# Low Power Quad Operational Amplifiers

- **Wide gain bandwidth: 1.3MHz**
- **Input common-mode voltage range includes ground**
- **Large voltage gain: 100dB**
- **Very low supply current/ampli: 375μA**
- **Low input bias current: 20nA**
- **Low input offset voltage: 5mV max. (for more accurate applications, use the equivalent parts LM124A-LM224A-LM324A which feature 3mV max.)**
- **Low input offset current: 2nA**
- **Wide power supply range:**
  Single supply: +3V to +30V
  Dual supplies: ±1.5V to ±15V

N
DIP14
(Plastic Package**)**

D
SO-14
(Plastic Micropackage**)**

P
TSSOP-14
(Thin Shrink Small Outline Package)

Description

These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Order Codes

Part Number	Temperature Range	Package	Packaging
LM124N	-55°C, +125°C	DIP	Tube
LM124D/DT		SO	Tube or Tape & Reel
LM224N	-40°C, +105°C	DIP	Tube
LM224D/DT		SO	Tube or Tape & Reel
LM224PT		TSSOP (Thin Shrink Outline Package)	Tape & Reel
LM324N	0°C, +70°C	DIP	Tube
LM324D/DT		SO	Tube or Tape & Reel
LM324PT		TSSOP (Thin Shrink Outline Package)	Tape & Reel
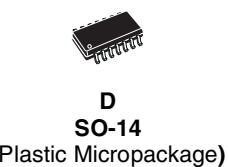
1   Pin & Schematic Diagram

**Figure 1: Pin connections (top view)**
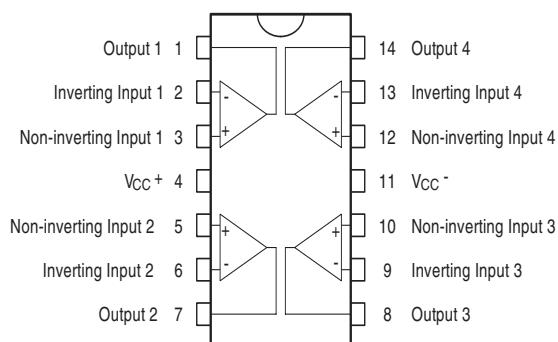
Figure 2: Schematic diagram (1/4 LM124)
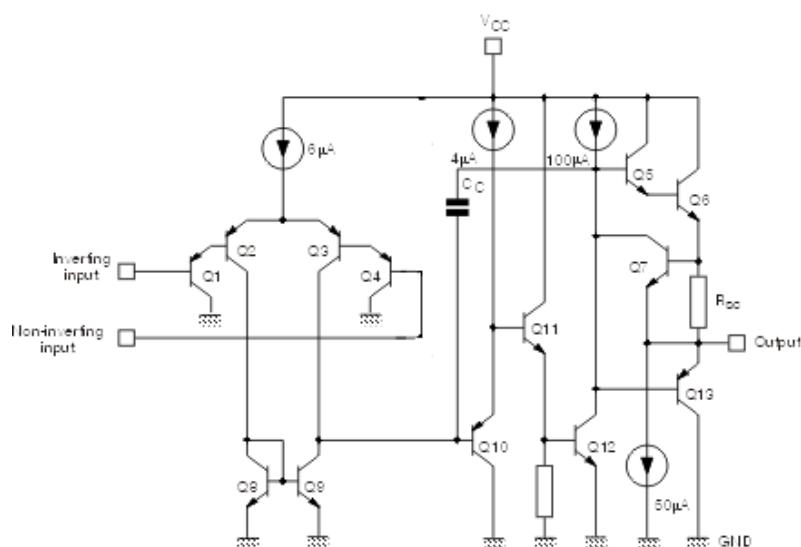
2   Absolute Maximum Ratings

Table 1: Key parameters and their absolute maximum ratings

Symbol	Parameter		LM124	LM224	LM324	Unit
VCC	Supply voltage		±16 or 32			V
V_i	Input Voltage		-0.3 to Vcc + 0.3			V
V_{id}	Differential Input Voltage [1]		-0.3 to Vcc + 0.3			V
P_{tot}	Power Dissipation	N Suffix D Suffix	500	500 400	500 400	mW mW
	Output Short-circuit Duration [2]		Infinite			
I_{in}	Input Current [3]		50	50	50	mA
T_{oper}	Operating Free-air Temperature Range		-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range		-65 to +150			°C
R_{thja}	Thermal Resistance Junction to Ambient SO14 TSSOP14 DIP14		103 100 66			°C/W

1) Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-.

2) Short-circuits from the output to VCC can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.

3) This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3V.

3 Electrical Characteristics

Table 2: V_{CC}^+ = +5V, V_{CC}^-= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - note [1] T_{amb} = +25°C LM324 $T_{min} \leq T_{amb} \leq T_{max}$ LM324		2	5 7 7 9	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		2	30 100	nA
I_{ib}	Input Bias Current - note [2] T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		20	150 300	nA
A_{vd}	Large Signal Voltage Gain V_{CC}^+ = +15V, R_L = 2kΩ, V_o = 1.4V to 11.4V T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \leq 10k\Omega$) V_{CC}^+ = 5V to 30V T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	65 65	110		dB
I_{CC}	Supply Current, all Amp, no load T_{amb} = +25°C V_{CC} = +5V V_{CC} = +30V $T_{min} \leq T_{amb} \leq T_{max}$ V_{CC} = +5V V_{CC} = +30V		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input Common Mode Voltage Range V_{CC} = +30V - note [3] T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common Mode Rejection Ratio ($R_s \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	70 60	80		dB
I_{source}	Output Current Source (V_{id} = +1V) V_{CC} = +15V, V_o = +2V	20	40	70	mA
I_{sink}	Output Sink Current (V_{id} = -1V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		mA µA
V_{OH}	High Level Output Voltage V_{CC} = +30V T_{amb} = +25°C R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$ V_{CC} = +5V, R_L = 2kΩ T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27 3.5 3	27 28		V

Table 2: V_{CC}^+ = +5V, V_{CC}^-= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit

V_{OL}	Low Level Output Voltage (R_L = 10kΩ)
	    T_{amb} = +25°C
	    $T_{min} \leq T_{amb} \leq T_{max}$
			5	20
				20
					mV

SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity Gain		0.4		V/μs
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF		1.3		MHz
THD	Total Harmonic Distortion f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = 2Vpp, C_L = 100pF, V_{CC} = 30V		0.015		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω, V_{CC} = 30V		40		$\dfrac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	30	μV/°C
DI_{lio}	Input Offset Current Drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel Separation - note [4] 1kHz $\leq$ f $\leq$ 20kHZ		120		dB

1) V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V

2)   The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

3)   The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.

4)   Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Table 3: V_{cc}^+ = +15V, V_{cc}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 2kΩ	100	V/mV
I_{cc}	No load, per amplifier	350	μA
V_{icm}		-15 to +13.5	V
V_{OH}	R_L = 2kΩ (V_{CC}^+=15V)	+13.5	V
V_{OL}	R_L = 10kΩ	5	mV
I_{os}	V_o = +2V, V_{CC} = +15V	+40	mA
GBP	R_L = 2kΩ, C_L = 100pF	1.3	MHz
SR	R_L = 2kΩ, C_L = 100pF	0.4	V/μs

Figure 3: Input bias current vs. ambient temperature

INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

Figure 6: Current limiting


Figure 4: Input voltage range
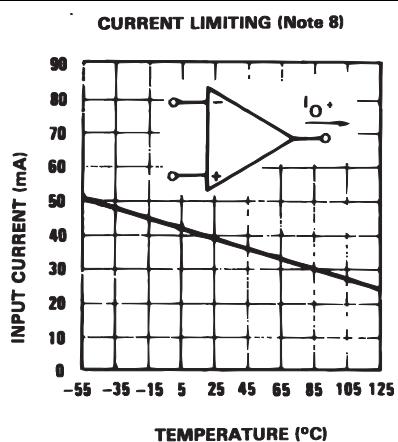

Figure 7: Supply current

Figure 5: Gain bandwidth product
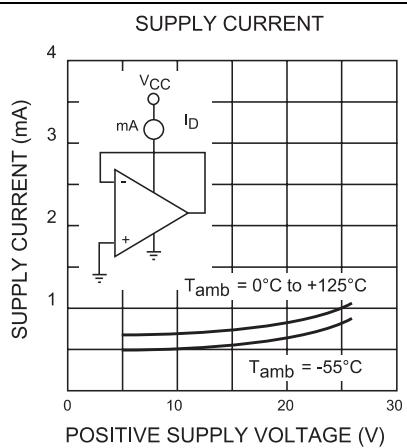
Figure 8: Common mode rejection ratio
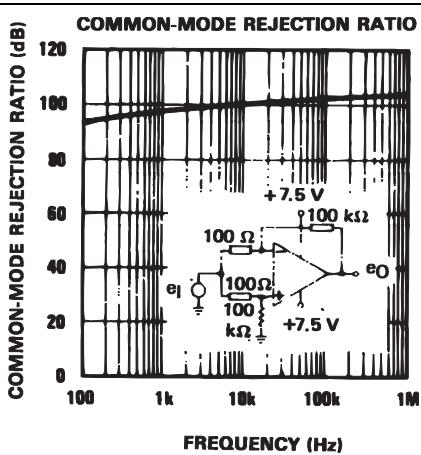
Figure 9: Electrical curves

OPEN LOOP FREQUENCY RESPONSE
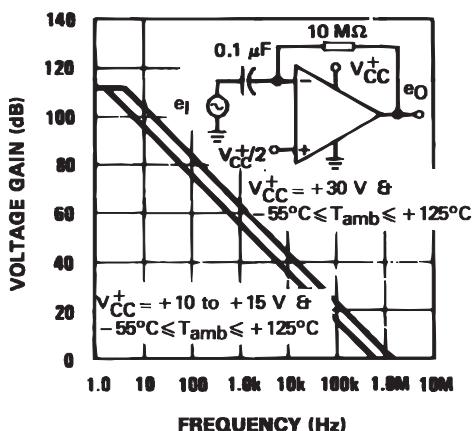
LARGE SIGNAL FREQUENCY RESPONSE
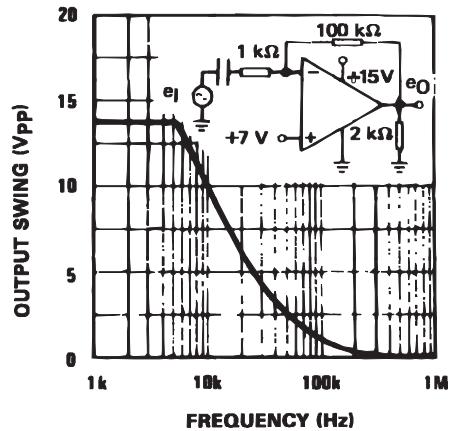
VOLTAGE FOLLOWER PULSE RESPONSE
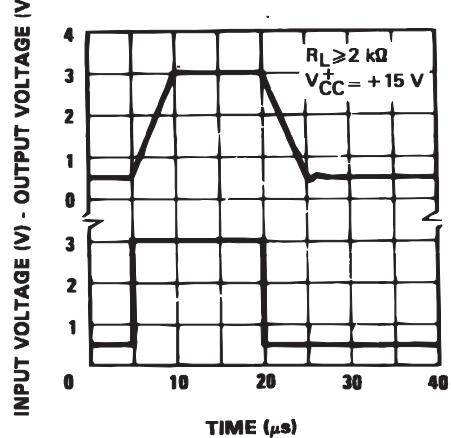
OUTPUT CHARACTERISTICS
(CURRENT SINKING)
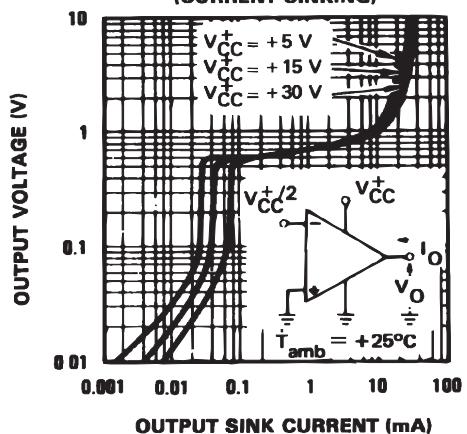
VOLTAGE FOLLOWER PULSE RESPONSE
(SMALL SIGNAL)
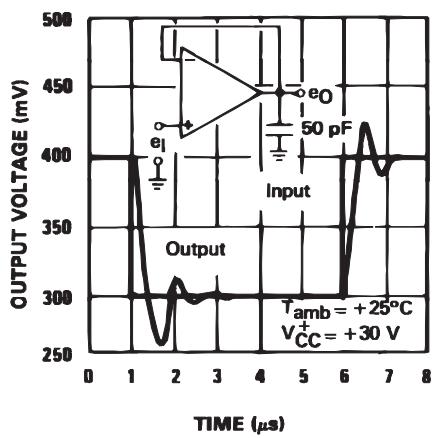
OUTPUT CHARACTERISTICS
(CURRENT SOURCING)
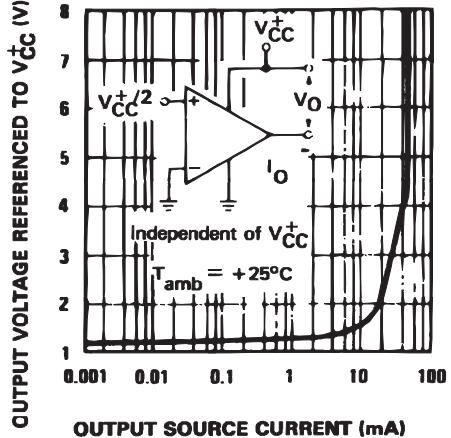
Figure 10: Input current

Figure 11: Power supply & common mode rejection ratio

Figure 12: Large signal voltage gain
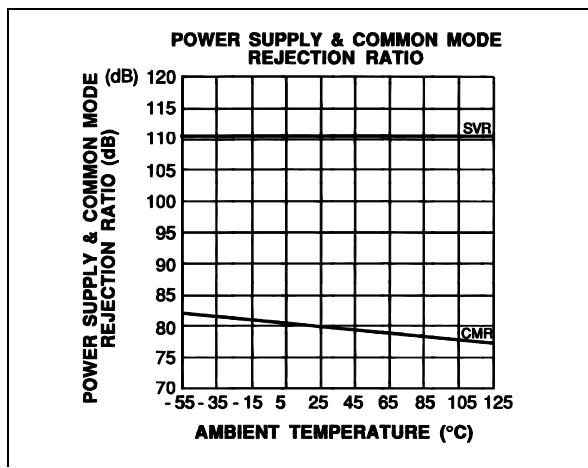
Figure 13: Voltage gain
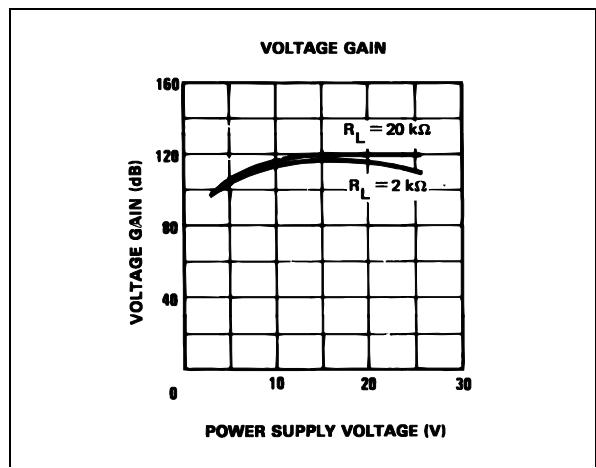
4   Typical Single - Supply Applications

Figure 14: AC coupled inverting amplifier

$$A_V = -\frac{R_f}{R1}$$

(as shown $A_V = -10$)
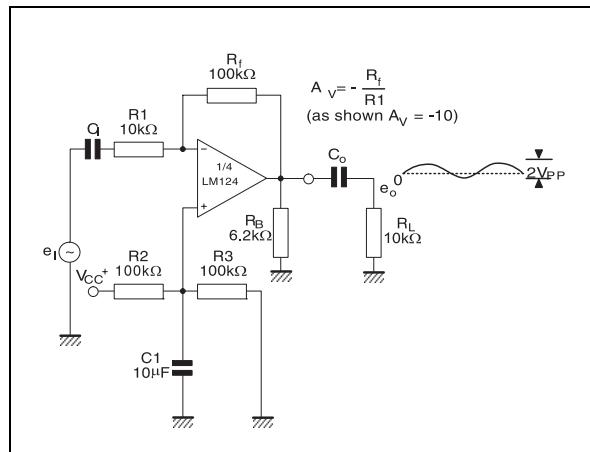
Figure 15: AC coupled non inverting amplifier

$$A_V = 1 + \frac{R2}{R1}$$

(as shown $A_V = 11$)
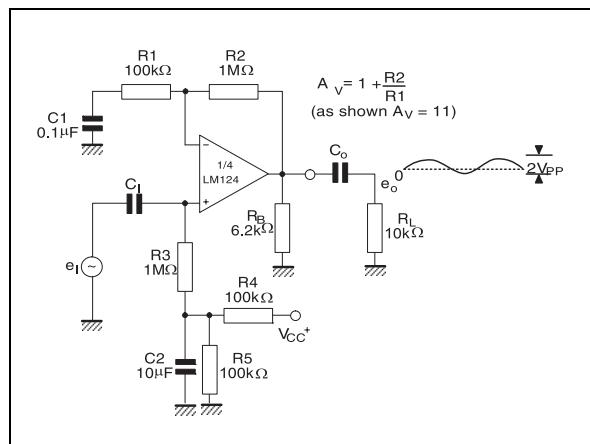
Figure 16: Non-inverting dc gain

$$A_V = 1 + \frac{R2}{R1}$$

(As shown $A_V = 101$)
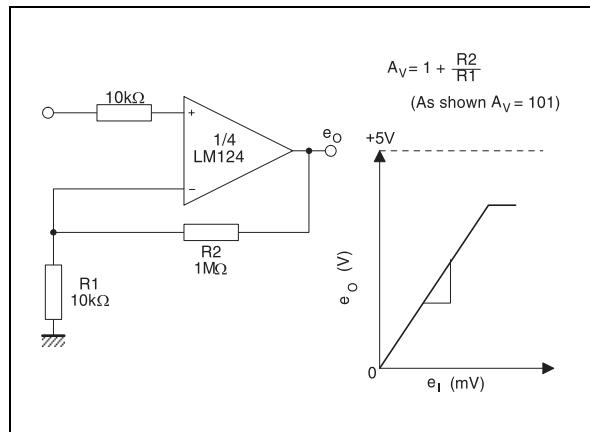
Figure 17: High input z adjustable gain DC instrumentation amplifier
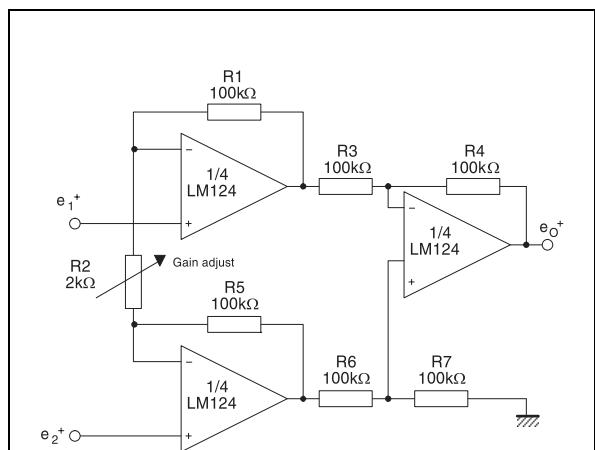
if $R1 = R5$ and $R3 = R4 = R6 = R7$

$$e_0 = \left[1 + \frac{2R_1}{R_2} \right] (e_2 - e_1)$$

As shown $e_0 = 101 (e_2 - e_1)$.

Figure 18: DC summing amplifier

$e_0 = e_1 + e_2 - e_3 - e_4$
Where $(e_1 + e_2) \geq (e_3 + e_4)$
to keep $e_0 \geq 0V$
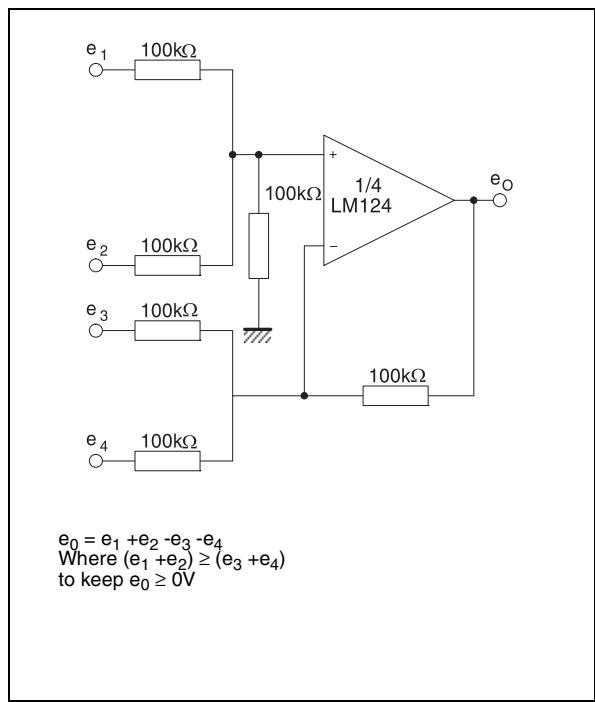
Figure 19: Low drift peak detector

* Polycarbonate or polyethylene

Figure 20: Activer bandpass filter

F_o = 1kHz

Q = 50

A_v = 100 (40dB)
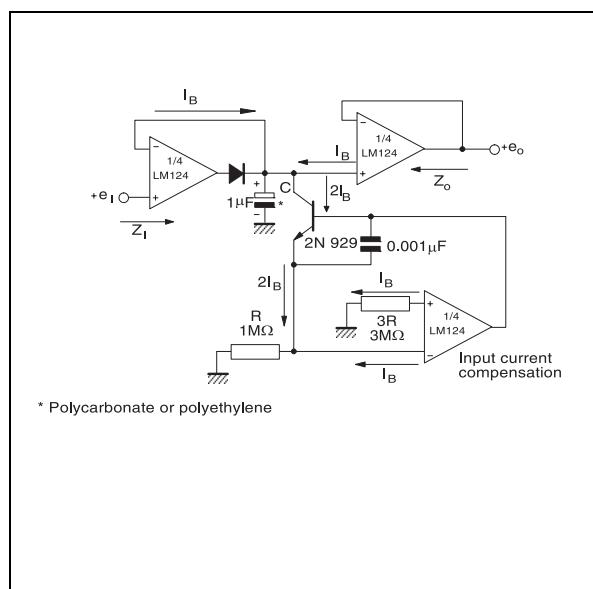
Figure 21: High input Z, DC differential amplifier

For $\dfrac{R_1}{R_2} = \dfrac{R_4}{R_3}$

(CMRR depends on this resistor ratio match)

$$e_0 \left(1 + \frac{R_4}{R_3} \right) \ (e_2 - e_1)$$

As shown $e_0 = (e_2 - e_1)$
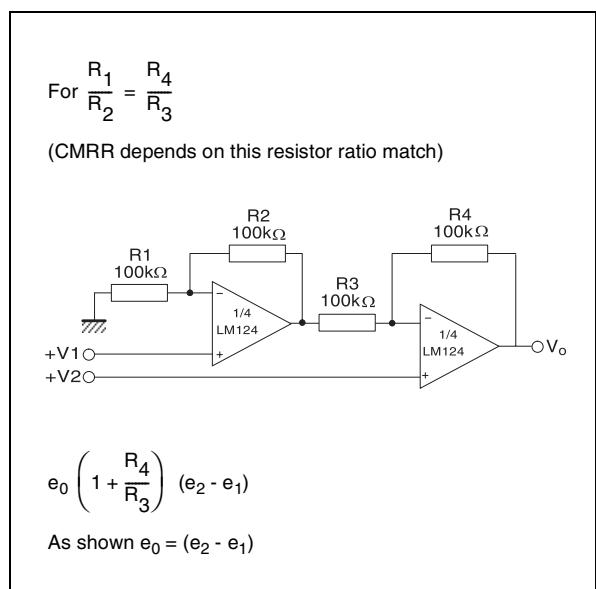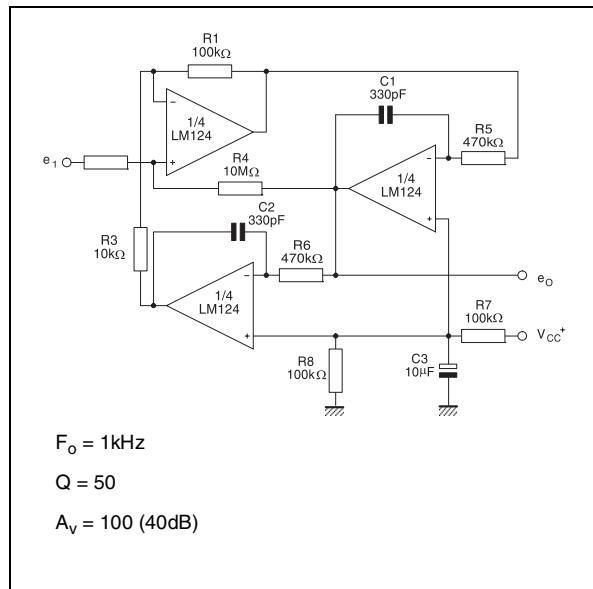
Figure 22: Using symetrical amplifiers to reduce input current (general concept)
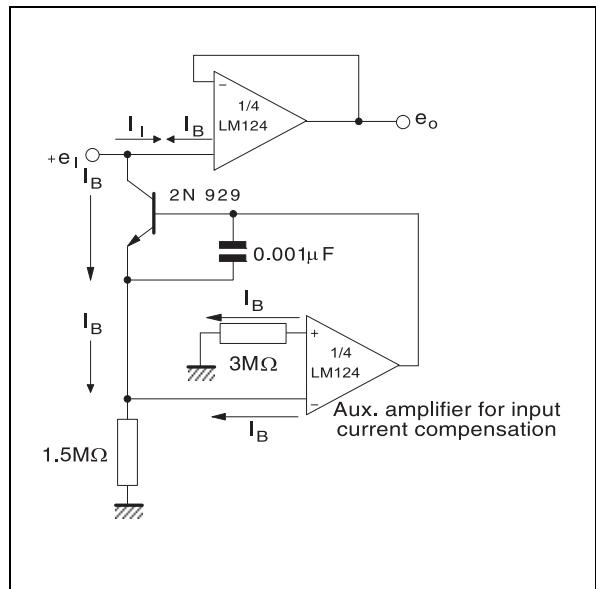
5   Macromodel

Warning: **Please consider following remarks before using this macromodel:**
All models are a trade-off between accuracy and complexity (i.e. simulation time).
Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach
and help to select surrounding component values.
A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING
CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as
the datasheet, its goal is to illustrate the main parameters of the product.
Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc) or even
worse: outside of the device operating conditions (Vcc, Vicm, etc) are not reliable in any way.

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** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT LM124 1 3 2 4 5 (analog)
********************************************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

6 Package Mechanical Data

6.1 DIP14 Package

	Plastic DIP-14 MECHANICAL DATA					
DIM.	**mm.**			**inch**		
	MIN.	**TYP**	**MAX.**	**MIN.**	**TYP.**	**MAX.**
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

P001A
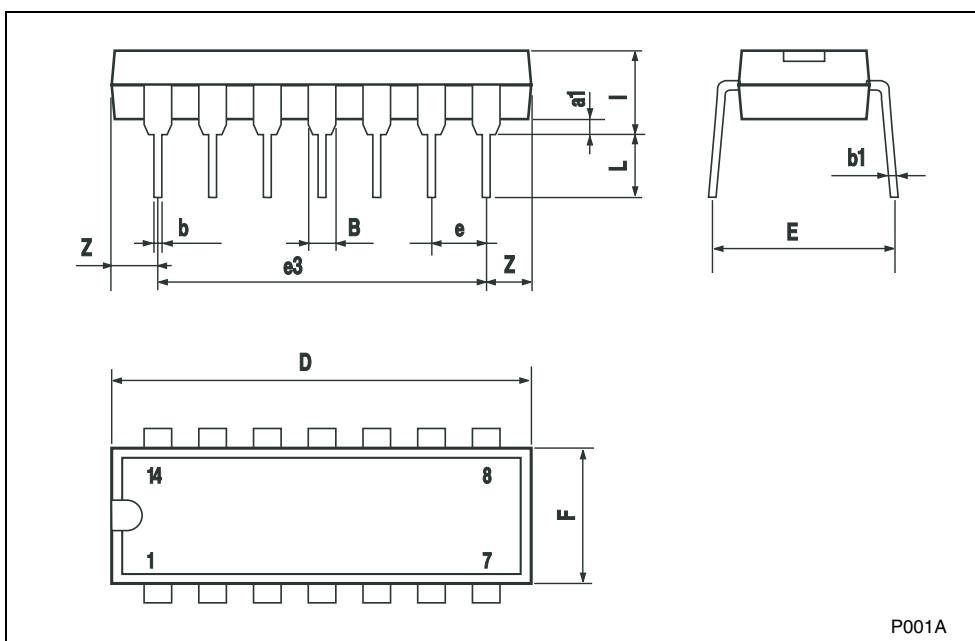
6.2 SO-14 Package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45˚ (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8˚ (max.)					

PO13G
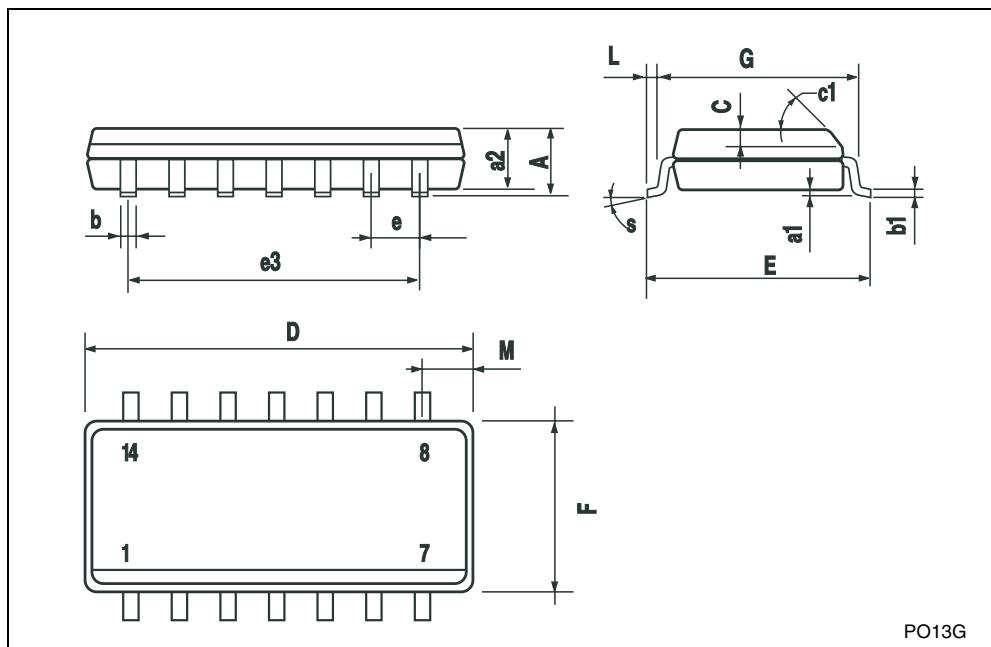
6.3 TSSOP14 Package

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0˚		8˚	0˚		8˚
L	0.45	0.60	0.75	0.018	0.024	0.030

TSSOP14 MECHANICAL DATA

0080337D
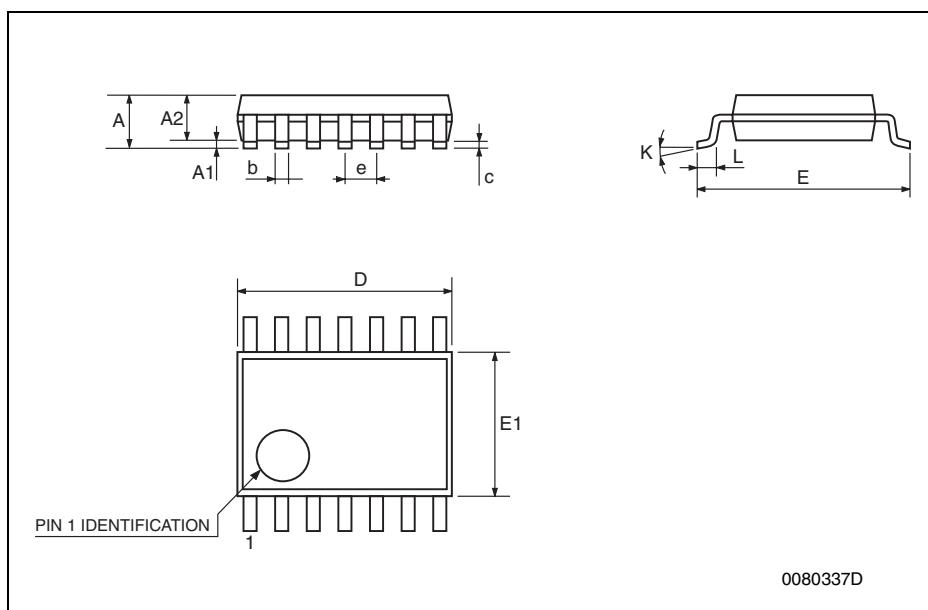
7   Summary of Changes

Date	Revision	Description of Changes
01 Oct. 2003	1	First Release
01 Jan. 2005	2	Modifications on AMR *Table 1 on page 3* (explanation of Vid and Vi limits)