



SBAS302A - DECEMBER 2003 - REVISED MARCH 2005

8-Bit, 8-Channel Sampling ANALOG-TO-DIGITAL CONVERTER with I²C[™] Interface

FEATURES

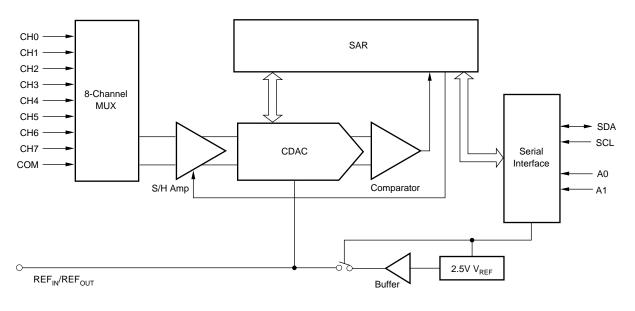
- 70kHz SAMPLING RATE
- ±0.5LSB INL/DNL
- 8 BITS NO MISSING CODES
- 4 DIFFERENTIAL/8 SINGLE-ENDED INPUTS
- 2.7V TO 5V OPERATION
- BUILT-IN 2.5V REFERENCE/BUFFER
- SUPPORTS ALL THREE I²C MODES: Standard, Fast, and High-Speed
- LOW POWER: 180μW (Standard Mode) 300μW (High-Speed Mode) 675μW (Fast Mode)
- DIRECT PIN COMPATIBLE WITH ADS7828
- TSSOP-16 PACKAGE

APPLICATIONS

- VOLTAGE-SUPPLY MONITORING
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY-OPERATED SYSTEMS
- REMOTE DATA ACQUISITION

DESCRIPTION

The ADS7830 is a single-supply, low-power, 8-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The Analog-to-Digital (A/D) converter features a sample-and-hold amplifier and internal, asynchronous clock. The combination of an I²C serial, 2-wire interface and micropower consumption makes the ADS7830 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7830 is available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I²C is a trademark of Koninklijke Philps Electronics N.V. All other trademarks are the property of their respective owners.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

+V _{DD} to GND	
Digital Input Voltage to GND	0.3 10 + v_{DD} + 0.3
Operating Temperature Range	40°C to +105°C
Storage Temperature Range	65°C to +150°C
Junction Temperature (T _J max)	+150°C
TSSOP Package	
Power Dissipation	$(T_J max - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION⁽¹⁾



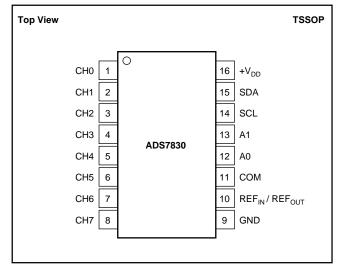
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7830I	±0.5	TSSOP-16	PW	–40°C to +85°C	ADS7830IPWT	Tape and Reel, 250
"	"	"	"	"	ADS7830IPWR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CH0	Analog Input Channel 0
2	CH1	Analog Input Channel 1
3	CH2	Analog Input Channel 2
4	CH3	Analog Input Channel 3
5	CH4	Analog Input Channel 4
6	CH5	Analog Input Channel 5
7	CH6	Analog Input Channel 6
8	CH7	Analog Input Channel 7
9	GND	Analog Ground
10	$\operatorname{REF}_{\operatorname{IN}}/\operatorname{REF}_{\operatorname{OUT}}$	Internal +2.5V Reference, External Reference Input
11	COM	Common to Analog Input Channel
12	A0	Slave Address Bit 0
13	A1	Slave Address Bit 1
14	SCL	Serial Clock
15	SDA	Serial Data
16	+V _{DD}	Power Supply, 3.3V Nominal



ELECTRICAL CHARACTERISTICS: +2.7V

At $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $+V_{DD} = +2.7V$, $V_{REF} = +2.5V$, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT Full-Scale Input Scan Absolute Input Range Capacitance	Positive Input - Negative Input Positive Input Negative Input	0 0.2 0.2	25	V _{REF} +V _{DD} + 0.2 +0.2	V V V pF
Leakage Current			±1		μΑ
SYSTEM PERFORMANCE No Missing Codes Integral Linearity Error Differential Linearity Error Offset Error Offset Error Match Gain Error Gain Error Match Noise Power-Supply Rejection		8	± 0.1 ± 0.1 ± 0.5 ± 0.05 ± 0.1 ± 0.05 100 72	± 0.5 ± 0.5 ± 1 ± 0.25 ± 0.5 ± 0.25	Bits LSB ⁽¹⁾ LSB LSB LSB LSB µVRMS dB
SAMPLING DYNAMICS Throughput Frequency	High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz			70 10 2.5	kSPS ⁽²⁾ kSPS kSPS
Conversion Time			5		μs
AC ACCURACY Total Harmonic Distortion Signal-to-Ratio Signal-to-(Noise+Distortion) Ratio Spurious-Free Dynamic Range Isolation Channel-to-Channel	$\begin{array}{l} V_{\text{IN}}=2.5V_{\text{PP}} \text{ at } 1\text{kHz} \\ V_{\text{IN}}=2.5V_{\text{PP}} \text{ at } 1\text{kHz} \\ V_{\text{IN}}=2.5V_{\text{PP}} \text{ at } 1\text{kHz} \\ V_{\text{IN}}=2.5V_{\text{PP}} \text{ at } 1\text{kHz} \end{array}$		-72 50 49 68 90		dB ⁽³⁾ dB dB dB dB
VOLTAGE REFERENCE OUTPUT Range Internal Reference Drift Output Impedance Quiescent Current	Internal Reference ON Internal Reference OFF Internal Reference ON, SCL and SDA pulled HIGH	2.475	2.5 15 110 1 850	2.525	V ppm/°C Ω GΩ μΑ
VOLTAGE REFERENCE INPUT Range Resistance Current Drain	High-Speed Mode: SCL= 3.4MHz	0.05	1 20	V _{DD}	V GΩ μA
DIGITAL INPUT/OUTPUT Logic Family Logic Levels: V _{IH} V _{IL} V _{OL} Input Leakage: I _{IH} I _{IL} Data Format	Minimum 3mA Sink Current $V_{IH} = +V_{DD} +0.5$ $V_{IL} = -0.3$	+V _{DD} • 0.7 -0.3 -10	CMOS Straight Binary	+V _{DD} + 0.5 +V _{DD} • 0.3 0.4 10	ν ν μΑ μΑ
ADS7830 HARDWARE ADDRESS			10010		Binary
POWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Quiescent Current Power Dissipation	Specified Performance High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz High-Speed Mode: SCL = 3.4MHz	2.7	225 100 60 675	3.6 320 1000	ν μΑ μΑ μW
Power-Down Mode w/Wrong Address Selected Full Power-Down	Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz SCL Pulled HIGH, SDA Pulled HIGH		300 180 70 25 6 400	3000	μW μW μA μA μA nA
				0000	10.1

NOTES: (1) LSB means least significant bit. When V_{REF} = 2.5V, 1LSB is 9.8mV.

(2) kSPS means kilo samples-per-second.

(3) THD measured out to the 9th-harmonic.





ELECTRICAL CHARACTERISTICS: +5V

At $T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $+V_{DD} = +5.0$ V, $V_{REF} =$ External +5.0V, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

ANALOG INPUT Positive Input - Negative Input Positive Input Absolute Input Range O -0.2 -0.2 -0.2 V +V _{REF} +V _{D0} + 0.2 +0.2 V V V V +0.2 Capacitance Leakage Current 25 y SYSTEM PERFORMANCE Negative Input 3 11 yA SYSTEM PERFORMANCE No Missing Codes Integral Linearity Error Offset Error Bain Error Bain Error Notes 8 10.1 10.5 LSB Offset Error Same Error Match Gain Error Noise Power-Supply Rejection 20.1 10.5 LSB SAMPLING DYNAMICS Throughput Frequency High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz 70 kSPS(2) kSPS(2) kSPS(2) kSPS Conversion Time V _N = 5V _{PP} at 1kHz Signal+to-Rhoise-Dilotrion Nine Symp at 1kHz -72 dB ⁽³⁾ dB dB Signal+to-Rhoise-Dilotrion Vin = 5V _{PP} at 1kHz 50 gB dB dB Signal+to-Rhoise-Dilotrion Vin = 5V _{PP} at 1kHz 50 gB dB dB Signal+to-Rhoise-Dilotrion Vin = 5V _{PP} at 1kHz 68 dB dB dB Signal+to-Rhoise-Dilotrion Range Internal Reference OFF 11 GQ Q QL Notac Reference Dift Output I				ADS7830E			
Line Scale Positive Input - Negative Input Positive Input - Negative Input Positive Input - Negative Input 0 -0.2 -0.2 V_{0PF} + V_{0P} + 0.2 V + V_{0P} + 0.2 V + 0.2 V + 0	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS	
Absolute Input Range Positive Input -0.2 $+V_{00} + 0.2$ V Capacitance Laskage Current -0.2 25 $+V_{00} + 0.2$ V SYSTEM PERFORMANCE Nesain Codes 8 -0.2 25 $+0.2$ V SWSTEM PERFORMANCE 8 -0.1 -0.5 1.5 LSBP Integral Linearity Error -0.2 40.1 -0.5 1.5 LSBP Offset Error Gain Error -0.0 -0.2.5 LSB 1.0.1 -0.0.5 LSBP Offset Error Match -0.0 -0.0.5 LSB -0.0.5 LSB -0.0.5 LSB Gain Error Match -0.0 -0.2.5 LSB -0.0.5 LSB -0.0.5 LSB Somethon Disorition Yes EVs at 1M4z -72 dBC -0.0.5 LSP -0.0	ANALOG INPUT						
Absolute Input Range Positive Input -0.2 $+V_{00} + 0.2$ V Capacitance Laskage Current -0.2 25 $+V_{00} + 0.2$ V SYSTEM PERFORMANCE Nesain Codes 8 -0.2 25 $+0.2$ V SWSTEM PERFORMANCE 8 -0.1 -0.5 1.5 LSBP Integral Linearity Error -0.2 40.1 -0.5 1.5 LSBP Offset Error Gain Error -0.0 -0.2.5 LSB 1.0.1 -0.0.5 LSBP Offset Error Match -0.0 -0.0.5 LSB -0.0.5 LSB -0.0.5 LSB Gain Error Match -0.0 -0.2.5 LSB -0.0.5 LSB -0.0.5 LSB Somethon Disorition Yes EVs at 1M4z -72 dBC -0.0.5 LSP -0.0	Full-Scale Input Scan	Positive Input - Negative Input	0		V	V	
Negative Input -0.2 -0.2 +0.2 V Leakage Current -0.2 25 -27 -2 No Masing Codes -1 -2.1 -2 -2 SYSTEM PERFORMANCE -2.1 -2.1 -2.1 -2.1 No Masing Codes -0.0 -3.0.5 LSBF -2.5 LSBF Offset Error Match -0.0.5 +0.0.5 +0.0.5 LSBF Gain Error Match -0.0.5 +0.0.5 LSBF Noise -0.0.5 +0.0.5 LSBF SameLinko DYNAMICS High-Speed Mode: SCL = 3.4MHz -7.0 kSPSF Conversion Time -2.5 kSPSF 2.5 kSPSF Conversion Time -2.4 -7.2 -4.6 4.9 Signation Chaine -2.4 -7.2 -4.6 4.9 Signation Chaine -2.4 -7.2 -4.6 4.9 -4.6 Signation Chaine -2.4 -7.2 -4.6 -4.6 -4.6 -4.6 -4.6 -4.6					+V _{PP} + 0.2		
Capacitance Leskage Current PF PF SYSTEM PERFORMANCE No Massing Codes Integral Lunearity Error Offset Error Master Gan Error Match 8 -0.1 -0.5 LSB Bits 10.0 Offset Error Mores Error Match -0.5 -1.1 -0.5 LSB Bits 10.0 -0.5 LSB Bits 20.1 -0.5 LSB Bits 10.0 -0.5 -0.5 -0.5 LSB Bits 10.0 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5 -0.5	i soorato inpat i tango				+0.2		
Lakage Current Image Lakage Current Image Linearity Image	Capacitance			25			
No Missing Codes Integral Linearity Error Offset Error Offset Error Offset Error Offset Error Offset Error Match Gain Error Gain Error Sam Funo Diffset Sam Funo Sam Funo Sam Funo Diffset Sam Funo Sam Funo	Leakage Current			±1			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	SYSTEM PERFORMANCE						
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			8				
Offset Error $+0.5$ $+1$ LSB Gain Error ± 0.05 ± 0.05 ± 0.05 ± 0.05 Gain Error ± 0.05 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
Offset Error Match ab. 2005 40.25 LSB Gain Error Match 10.05 40.25 LSB Noise 10.05 40.25 LSB Power-Supply Rejection 72 68 SAMPLING DYNAMICS 70 KSPS Conversion Time 70 KSPS Conversion Time 5 10 AC ACCURACY 2.5 KSP Signal-to-Roise-Distrotion V _M = 5V _{PP} at 1HHz 50 dB Signal-to-Roise-Distrotion V _M = 5V _{PP} at 1HHz 50 dB dB Signal-to-Roise-Distrotion V _M = 5V _{PP} at 1HHz 49 dB dB dB Signal-to-Roise-Distrotion V _M = 5V _{PP} at 1HHz 50 dB							
Gain Error Gain Error Match Noise Noise Noise Power-Supply Rejection 40.1 40.5 LSB LSB LSB LSB LSB LSB LSB LSB LSB LSB							
Gain Error Match Noise ±0.05 (1) ±0.05 (2) ±0.25 (2) LSB (μVRMB (2) SAMPLING DYNAMICS Throughput Frequency High-Speed Mode: SCL = 3.4MHz Fast Mode, SCL = 100kHz 70 kSP5 (2) kSP5 (2) Conversion Time Standard Mode, SCL = 100kHz 5 2.5 µpR AC ACCURACY Total Harmonic Distortion Signal-to-Ratio V _N = 5V _{PP} at 1kHz 50 68 68 Signal-to-Ratio V _N = 5V _{PP} at 1kHz 50 68 68 68 Soptious-Free Dynamic Range V _N = 5V _{PP} at 1kHz 68 68 68 68 Soptious-Free Dynamic Range V _N = 5V _{PP} at 1kHz 5 2.55 V_D 68 60 60 60 60 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
Noise Power-Supply Rejection 100 72 μμγRMS dB SAMPLING DYNAMICS Throughput Prequency High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400Hz Standard Mode, SCL = 100KHz 70 KSPS/30 Conversion Time 5 10 KSPS/30 Conversion Time 5 48 AC ACCURACY Total Harmonic Distortion Signal-to-(Noise-Distortion) Signal-to-(Noise-Distortion) Range V _M = 5V _{pp} at 1kHz Signal-to-(Noise-Distortion) V _M = 5V _{pp} at 1kHz -72 dB ⁽³⁾ Solution Channel-to-Channel V _M = 5V _{pp} at 1kHz 49 dB Spinato-(Noise-Distortion) Resolution Channel-to-Channel V _M = 5V _{pp} at 1kHz 49 dB VoltAGE REFERENCE OUTPUT Range Merisstance Internal Reference OFF 110 GD GD Ouisscent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 V _{pp} + 0.5 V Ouisscent Current High-Speed Mode: SCL = 3.4MHz -0.3 1 GD GD Current Drain High-Speed Mode: SCL = 3.4MHz -0.05 1 GD V _{DD} V Digit Levels: V _H V _{VL} Minimum 3mA Sink Current -0.3 -0.3 V <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
Power-Supply Rejection 72 dB SAMPLING DYNAMICS Throughput Frequency High-Speed Mode: SCL = 3.4MHz Fast Mode, SCL = 100kHz 70 kSPS/2 Conversion Time Standard Mode, SCL = 100kHz 5 70 kSPS/2 Ac ACCURACY Total Harmonic Distortion Signal-to-Ratio V _{III} = 5V _{ep} at 1HHz 5 400 ⁽¹⁾ 40 ⁽¹⁾ Signal-to-Ratio V _{III} = 5V _{ep} at 1HHz 50 48 49 48 Sources-to-Dynamic Range V _{III} = 5V _{ep} at 1HHz 50 48 49					±0.25	-	
SAMPLING DYNAMICS Throughput Frequency High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400KHz 70 10 kSPS(2) kSPS Conversion Time 70 kSPS(2) 10 kSPS(2) Conversion Time 5 µs 2.5 µs AC ACCURACY Total Harmonic Distortion Signal-to-Ratio Signal-to-Ratio Signal-to-Choise-Distortion) Ratio Signal-to-Choise-Distortion Ratio Subalano Channel-to-Channel V _M = 5V _{PP} at 1KHz 50 dB ⁽³⁾ Solution Channel-to-Channel V _M = 5V _{PP} at 1KHz 51 2.55 V Notack Reference Durput Range V _M = 5V _{PP} at 1KHz 68 dB dB VoltAGE REFERENCE OUTPUT Range Internal Reference ON Internal Reference OFF 110 0 µA Outascent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 µA DGIGTAL INPUTYOUTPUT Logic Family Logic Levels: V _M V _{UL} V _M = +V _{OD} + 0.5 V V 0.4 V Data Format V _M = +V _{OD} + 0.5 V 0.4 V V V Data Format V _M = +V _{OD} + 0.5 V 75 100 µA Dower Supply Voltage, +V _{OD}						•	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				12		ub	
Standard Mode, SCL = 400kHz 10 ksps Conversion Time 3tandard Mode, SCL = 400kHz 5 μ s AC ACURACY Total Harmonic Distortion $V_{M1} = SV_{PP}$ at 1kHz 50 μ s Signal-to-Ratio Signal-to-Ratio $V_{M1} = SV_{PP}$ at 1kHz 50 $dB^{(5)}$ Signal-to-Ratio Signal-to-Ratio $V_{M1} = SV_{PP}$ at 1kHz 50 dB Signal-to-Ratio Signal-to-Ratio $V_{M1} = SV_{PP}$ at 1kHz 50 dB Signal-to-Roise-Distortion Ratio $V_{M1} = SV_{PP}$ at 1kHz 50 dB dB Solation Channel-to-Channel V $V_{M1} = SV_{PP}$ at 1kHz 50 dB VoltAGE REFERENCE OUTPUT Internal Reference ON 110 $G\Omega$ μ Quiescent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 μ μ Range Corrent Drain High-Speed Mode: SCL = 3.4MHz 20 μ μ Logic Family V _{M1} = +V_{D0} + 0.5 -0.3 1 ν ν Logic Family V _{M1} = +V_{D0} +		High-Speed Mode: SCL = 3 4MHz			70	kSPS ⁽²⁾	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	······································	5 1			-		
Conversion Time 5 μ s AC ACCURACY Total Harmonic Distortion Signal-to-Ratio Signal-to-Ratio Signal-to-Ratio Signal-to-Ratio Signal-to-Ratio Signal-to-Roise+Distortion) Ratio Spurious-Free Dynamic Range Solution Channel-to-Channel $V_{N} = SV_{pp}$ at 1kHz -72 $B^{[3]}$ $B^{[3]}$ Signal-to-Ratio Signal-to-Ratio Signal-to-Ratio Signal-to-Ratio Solution Channel-to-Channel $V_{N} = SV_{pp}$ at 1kHz 50 $dB^{[3]}$ VOLTAGE REFERENCE OUTPUT Range Internal Reference ON Internal Reference OFF 1 GG Quiescent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 μ A VOLTAGE REFERENCE INPUT Range Int. Ref. ON, SCL and SDA pulled HIGH 1300 μ A Digrid LineVUT/OUTPUT Logic Family Logic Levels: V _H $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ Digrid LineVUT/OUTPUT Logic Family Logic Levels: V _H $V_{IL} = +0.3$ -100 $W_{DD} + 0.5$ $V_{DD} + 0.5$ Data Format $V_{IL} = +0.3$ $V_{IL} = -0.3$ 0.05 $V_{DD} + 0.5$ $V_{DD} + 0.5$ Power-Dupply Voltage, + $V_{DD} + 0.5$ $V_{IL} = -0.3$ $V_{IL} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ Diglic Levels: V _H $V_{IL} = -0.3$ <							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Conversion Time	,		5		μs	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	AC ACCURACY						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Total Harmonic Distortion			-72		dB ⁽³⁾	
Spurious-Free Dynamic Range Isolation Channel-to-Channel $V_{\rm N} = 5V_{\rm pp}$ at 1kHz68 90dB dBIsolation Channel-to-Channel90dBRange Internal Reference Drift Output Impedance1.10 Internal Reference OFF Internal Reference OFF2.4752.5 1.52.525VQuiescent CurrentInternal Reference OFF Internal Reference OFF110 1.00 Ω Ω VOLTAGE REFERENCE INPUT Range Resistance Current DrainHigh-Speed Mode: SCL = 3.4MHz0.05V QMinimum 3mA Sink Current V V V V V V V V V V V V V V V Q U Updet Leakage: 1,H H Internal Reference Mode: SCL = 3.4MHz0.05V V V V V V V V V V V V V V V QCMOS V V V V V V V V V V V V V V V QMinimum 3mA Sink Current V V V V V V V V V QCMOS V V V V V V V V V V V QSpecified Performance High-Speed Mode: SCL = 3.4MHz T5010010BinaryADS7830 HARDWARE ADDRESS10010Binary Fast Mode: SCL = 400kHz Standard Mode, SCL = 400kHz4.7555.25V M MO MAPower DissipationHigh-Speed Mode: SCL = 3.4MHz High-Speed Mode: SCL = 400kHz10010Binary BinaryPower-Down Mode W/Wrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz1000 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
Isolation Channel - Channel 90 dB VOLTAGE REFERENCE OUTPUT Range Range 2.475 2.5 2.525 V Internal Reference Drift Output Impedance Internal Reference OFF 110 GQ Q Quiescent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 μA VOLTAGE REFERENCE INPUT Range Resistance No.05 V V Q Current Drain High-Speed Mode: SCL = 3.4MHz 20 V Q Digit L INPUT/OUTPUT Logic Levels: V _H V _L V _L CMOS +V _{DD} • 0.7 -0.3 V V _L Minimum 3mA Sink Current I _L V _L 0.4 V V Data Format V _L V _L 0.4 V 4/2 ADS7830 HARDWARE ADDRESS 10010 Binary Binary Ma Power-Supply Voltage, +V _{DD} Specified Performance High-Speed Mode: SCL = 3.4MHz 3.75 5 V Quiescent Current High-Speed Mode: SCL = 3.4MHz 3.00 µA µA Data Format 10010 Binary <t< td=""><td>o (</td><td></td><td></td><td></td><td></td><td></td></t<>	o (
VOLTAGE REFERENCE OUTPUT Range Internal Reference Drift Output Impedance2.4752.52 V 15 Quiescent CurrentInternal Reference ON Internal Reference OFF Int. Ref. ON, SCL and SDA pulled HIGH1300 A VOLTAGE REFERENCE INPUT Range Resistance Current Drain1300 V_{DD} V_{DD} V_{DD} DIGITAL INPUT/OUTPUT Logic Family Logic Levels: V _H V_{L} Law Quiescent CurrentHigh-Speed Mode: SCL = 3.4MHz0.05 V_{DD} V_{DD} V_{DD} DIGITAL INPUT/OUTPUT Logic Family Logic Levels: V _H V_{L} Minimum 3mA Sink Current $V_{H} = +V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{DD} + 0.5$ $V_{DD} + 0.5$ $V_{L} = -0.3$ $V_{$		V _{IN} = 5V _{PP} at 1kHz					
Range Internal Reference Drift Output Impedance 2.475 2.5 2.525 V ppm/°C Output Impedance Internal Reference ON Internal Reference OFF 110 Ω Ω Quiescent Current Int. Ref. ON, SCL and SDA pulled HIGH 1300 µA VOLTAGE REFERENCE INPUT Range 0.05 1 0.05 1 Ω Current Drain High-Speed Mode: SCL = 3.4MHz 20 µA GΩ µA DigitAL INPUT/OUTPUT Logic Levels: Vi _H Vi _L 0.05 1 CMOS +Vo _D + 0.5 V VL Vi _L 0.4 V µA Vo _D + 0.5 V Logic Levels: Vi _H Vi _L = +V _{DD} + 0.5 V +Vo _D + 0.5 V V Logic Levels: Vi _H Vi _H = +V _{DD} + 0.5 V V µA Data Format Vi _H = +V _{DD} + 0.5 V V µA Data Format Specified Performance 4.75 5 5.25 V Power-Supply Votage, +V _{DD} Specified Performance 4.75 5 5.25 V	Isolation Channel-to-Channel			90		dB	
Internal Reference Drift Output ImpedanceInternal Reference ON Internal Reference OFF15 110ppm/*C Ω Quiescent CurrentInt. Ref. ON, SCL and SDA pulled HIGH1300 μ A VOLTAGE REFERENCE INPUT Range ResistanceInt. Ref. ON, SCL and SDA pulled HIGH0.051 1 $G\Omega$ $G\Omega$ DiGITAL INPUT/OUTPUT Logic Family Logic Levels: V _H UL Logic FamilyHigh-Speed Mode: SCL = 3.4MHz0.051 0.05 V_{DD} V V_{DD} DiGITAL INPUT/OUTPUT Logic Family Logic Levels: V _H UL Logic Levels: V _H UL Logic FamilyMinimum 3mA Sink Current $V_{IL} = 0.3$ CMOS $+V_{DD} + 0.5$ $V_{L} = 0.3$ V 0.4 V V $V_{L} = 0.3$ V $V_{DD} + 0.5$ $V_{U} = 0.3$ V $V_{DD} + 0.5$ V $V_{U} = 0.3$ ADS7830 HARDWARE ADDRESSInternal Reference $V_{U} = 0.5$ Internal Reference $V_{U} = 0.3$ <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td></td<>							
Output ImpedanceInternal Reference ON Internal Reference OFF110 1 GΩQuiescent CurrentInt. Ref. ON, SCL and SDA pulled HIGH1300μAVOLTAGE REFERENCE INPUT Range Resistance Current DrainNo.SCL and SDA pulled HIGH0.051 U GΩV U DDIGITAL INPUT/OUTPUT Logic Family Logic Levels: V _{IH} V _{IL} High-Speed Mode: SCL = 3.4MHz0.051 CMOSV U U UDigitationHigh-Speed Mode: SCL = 3.4MHzCMOS+V U <td></td> <td></td> <td>2.475</td> <td></td> <td>2.525</td> <td>-</td>			2.475		2.525	-	
Internal Reference OFF Quiescent Current1GΩ IQuiescent CurrentInt. Ref. ON, SCL and SDA pulled HIGH1300 μA VolTAGE REFERENCE INPUT Range 				-			
Quiescent CurrentInt. Ref. ON, SCL and SDA pulled HIGH1300 μ AVOLTAGE REFERENCE INPUT Range Resistance Current DrainHigh-Speed Mode: SCL = 3.4MHz0.051 V_{DD} V GQDIGITAL INPUT/OUTPUT Logic Family Logic Levels: V _H V _{LL} High-Speed Mode: SCL = 3.4MHz 0.05 1 μ ADIGITAL INPUT/OUTPUT Logic Family Logic ArmingMinimum 3mA Sink Current V_{IL} $+V_{DD} \bullet 0.7$ -0.3 $+V_{DD} \bullet 0.5$ $+V_{DD} \bullet 0.7$ -0.3 $+V_{DD} \bullet 0.5$ $+V_{DD} \bullet 0.5$ 0.4 V V V_{UL} Input Leakage: I _H I _{LL} QuieMinimum 3mA Sink Current $V_{IL} = -0.3$ -10 0.4 V V -10 V V V Data FormatStraight Binary 0.4 V V μ AADS7830 HARDWARE ADDRESS 0.000 0.000 μ A V_{IL} Power-Supply Voltage, +V _{DD} V GauseSpecified Performance $High-Speed Mode: SCL = 3.4MHz$ $Fast Mode: SCL = 400kHz10010BinaryPower DissipationHigh-Speed Mode: SCL = 4.00kHzHigh-Speed Mode: SCL = 4.00kHz1.5mW0.75Power-Down Modew/Wrong Address SelectedHigh-Speed Mode: SCL = 1.00kHzFast Mode: SCL = 4.00kHz3.755Full Power-DownSCL Pulled HIGH, SDA Pulled HIGH400030000nATEMPERATURE RANGESCL Pulled HIGH, SDA Pulled HIGH40003000nA$	Output Impedance			-			
VolTAGE REFERENCE INPUT Range Resistance Current DrainHigh-Speed Mode: SCL = 3.4MHz 0.05 V_{DD} V_{DD} DIGITAL INPUT/OUTPUT Logic Family Logic Levels: V_{H} V_{UL} Input Leakage: I_{H} Data FormatMinimum 3mA Sink Current $V_{IL} = -0.3$ $V_{DD} \bullet 0.7$ -0.3 $+V_{DD} \bullet 0.5$ $V_{UD} \bullet 0.3$ V $V_{DD} \bullet 0.5$ $V_{VD} \bullet 0.5$ V_{UL} $V_{UL} = -0.3$ $+V_{DD} \bullet 0.7$ -0.3 $+V_{DD} \bullet 0.5$ $V_{UD} \bullet 0.4$ $V_{UL} = -0.3$ $V_{UL} = -0.3$ Data FormatMinimum 3mA Sink Current I_{IL} 10010 BinaryADS7830 HARDWARE ADDRESS10010BinaryPower-Supply Voltage, $+V_{DD}$ Quiescent Current High-Speed Mode: SCL = 3.4MHz Standard Mode, SCL = 100KHz Fast Mode: SCL = 3.4MHz Standard Mode, SCL = 100KHz 4.75 5 Power DissipationHigh-Speed Mode: SCL = 3.4MHz Standard Mode, SCL = 100KHz Fast Mode: SCL = 400KHz Standard Mode, SCL = 100KHz 1.5 1.5 mW mW mW mW Standard Mode, SCL = 100KHz 1.5 μ_A Power-Down Mode wWrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz $Fast Mode: SCL = 400KHzFast Mode: SCL = 400KHzFast Mode: SCL = 100KHzFast Mode: SCL = 400KHzSCL = 100KHz35003535\mu_APower-DownSCL Pulled HIGH, SDA Pulled HIGH40004003000A\mu_A$	Quiescent Current						
Range Resistance Current Drain $High-Speed Mode: SCL = 3.4MHz$ 0.05 V_{DD} V_{DD} V GQ GQDIGITAL INPUT/OUTPUT Logic Family Logic Levels: V_{HH} V_{UL} High-Speed Mode: SCL = 3.4MHz $CMOS$ $+V_{DD} + 0.5$ V_{L} $+V_{DD} + 0.5$ V_{L} $+V_{DD} + 0.5$ V_{L} V_{U} V_{0L} 0.4 V Input Leakage: I_{HI} I_{L} $V_{HI} = +V_{DD} + 0.5$ $V_{L} = -0.3$ -10 N V_{DD} 0.4 V Data Format $V_{IL} = -0.3$ -10 $Straight$ $BinaryMMPOWER-SUPPLY REQUIREMENTSPower-Supply Voltage, +V_{DD}Specified PerformanceHigh-Speed Mode: SCL = 3.4MHz4.7555.25VQuiescent CurrentStraidf Mode, SCL = 100KHzStandard Mode, SCL = 100KHz1000\mu APower-Down ModewWrong Address SelectedHigh-Speed Mode: SCL = 3.4MHzFast Mode: SCL = 100KHz1.5MWmWPower-Down ModewWrong Address SelectedFast Mode: SCL = 100KHzFast Mode: SCL = 100KHz1.5MWmWPower-DownSCL Pulled HIGH, SDA Pulled HIGH40003000\mu AFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH40003000\Lambda$						μ.	
Resistance Current DrainHigh-Speed Mode: SCL = 3.4 MHz1 U $G\Omega$ μ DG17L INPUT/OUTPUT Logic Family Logic Levels: V_{H} V_{UL} Minimum 3mA Sink Current V_{UL} $CMOS$ $+V_{DD} + 0.5$ $+V_{DD} + 0.3$ $+V_{DD} + 0.5$ $V + V_{DD} + 0.3$ V $V_{UL} + V_{DD} + 0.5$ $V_{UL} = -0.3$ -0.3 $+V_{DD} + 0.5$ $V_{UL} + V_{DD} + 0.5$ 10 -10 0.4 V μ μ Data Format $V_{IL} = -0.3$ -10 Straight Binary 0.4 V μ μ ADS7830 HARDWARE ADDRESS 10010 BinaryPower-Supply Voltage, $+V_{DD}$ Specified Performance High-Speed Mode: SCL = 3.4 MHz 4.75 5 5.25 V μ Power DissipationHigh-Speed Mode: SCL = 3.4 MHz 3.00 μ A μ μ A $Standard Mode, SCL = 100KHz1000\muA\muPower-Down ModewWrong Address SelectedHigh-Speed Mode: SCL = 400KHz1.5mW\piat Mode, SCL = 400KHz1.5mW\piat Mode, SCL = 100KHzPower-DownScl L = 400$ KHz 3.5 μ A 400 μ A μ AFull Power-DownScl L = 100KHz 35 μ A 400 μ A 400 Full Power-DownScl L = Ulled HIGH, SDA Pulled HIGH 400 3000 μ A 400			0.05		Vpp	V	
Current DrainHigh-Speed Mode: $SCL = 3.4MHz$ 20 μ ADIGITAL INPUT/OUTPUT Logic Family Logic Levels: V_{H} V_{L} $V_{U_{L}}$ $V_{U_{D}} + V_{DD} + 0.5$ V_{L} $V_{V_{DD} + 0.5$ $V_{U_{L}} = -0.3$ $V_{V_{DD} + 0.5$ $V_{U_{L}} = -0.3$ $V_{U_{D}} + V_{DD} + 0.5$ $V_{U_{L}} = -0.3$ $V_{U_{D}} + V_{DD} + 0.5$ $V_{U_{L}} = -0.3$ 0.4 $V_{U_{L}} = -0.3$ V ADS7830 HARDWARE ADDRESS $V_{H_{L}} = -V_{DD} + 0.5$ $V_{U_{L}} = -0.3$ -10 $Straight$ $BinaryBinaryPOWER-SUPPLY REQUIREMENTSPower-Supply Voltage, +V_{DD}Specified PerformanceHigh-Speed Mode: SCL = 3.4MHzFast Mode: SCL = 400KHz4.7555.25VV\muAPower DissipationHigh-Speed Mode: SCL = 100KHz3.7550.75mWMWFast Mode: SCL = 400KHz1.50.75mWMWFast Mode: SCL = 100KHz0.750.75mWMWPower-Down ModeHigh-Speed Mode: SCL = 100KHz1.50.75mWMWmWFast Mode: SCL = 100KHz1.50.75mWMWPower-Down ModeHigh-Speed Mode: SCL = 100KHz1.500.75\muAPower-DownStandard Mode, SCL = 100KHz3.50.50\muAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nA$			0.00	1	• 00		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Current Drain	High-Speed Mode: SCL = 3.4MHz					
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	DIGITAL INPUT/OUTPUT						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Logic Family			CMOS			
V_{OL} Input Leakage: I_{HH} I_{LL} Minimum 3mA Sink Current $V_{HH} = +V_{DD} + 0.5$ $V_{IL} = -0.3$ 0.4VData Format $V_{HH} = +V_{DD} + 0.5$ $V_{IL} = -0.3$ -10Straight Binary μA μA ADS7830 HARDWARE ADDRESS10010BinaryPOWER-SUPPLY REQUIREMENTS Power-Supply Voltage, $+V_{DD}$ Quiescent CurrentSpecified Performance4.7555.25VPower-Supply Voltage, $+V_{DD}$ Quiescent CurrentSpecified Performance4.7555.25VPower DissipationHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz150 μA Power-Down Mode w/Wrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz1.5mWFast Mode: SCL = 400kHz Fast Mode: SCL = 100kHz1.5mWFull Power-DownStandard Mode, SCL = 100kHz Fast Mode: SCL = 100kHz35 μA Full Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nA	Logic Levels: V _{IH}						
$\begin{array}{ c c c c c c } \mbox{Input Leakage: I_{IH}} & V_{IH} = +V_{DD} + 0.5 \\ V_{IL} = -0.3 & V_{IL} = -0.3 & 10 & \mu A \\ \mbox{potencial} & Straight \\ \mbox{Binary} & Straight \\ Bi$			-0.3				
IIL Data FormatVIL = -0.3-10μAData FormatVIL = -0.3-10Straight BinaryμAADS7830 HARDWARE ADDRESS10010BinaryPOWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Quiescent CurrentSpecified Performance High-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400KHz4.7555.25VPower DissipationStandard Mode, SCL = 100KHz High-Speed Mode: SCL = 3.4MHz300 150μA μAPower-Down Mode w/Wrong Address SelectedFast Mode: SCL = 400KHz Fast Mode, SCL = 100KHz1.5 1.5mW mWPower-DownStandard Mode, SCL = 100KHz High-Speed Mode: SCL = 3.4MHz Standard Mode, SCL = 100KHz1.5 1.5mW mWPower-Down Mode w/Wrong Address SelectedFast Mode: SCL = 100KHz Standard Mode, SCL = 100KHz355 35μA μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nATEMPERATURE RANGEIIIII	V _{OL}						
Data FormatStraight BinaryADS7830 HARDWARE ADDRESS10010BinaryPOWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Specified Performance4.7555.25VQuiescent CurrentHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz7501000µAPower DissipationKatandard Mode, SCL = 100kHz150µAPower-Down ModeHigh-Speed Mode: SCL = 400kHz3.755mWPower-Down ModeHigh-Speed Mode: SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 100kHz0.75mWFast Mode: SCL = 100kHz1.5mWStandard Mode, SCL = 100kHz0.75mWStandard Mode, SCL = 100kHz0.75mWStandard Mode, SCL = 100kHz0.75mWStandard Mode, SCL = 100kHz35µAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000TEMPERATURE RANGEISOIA		$V_{IH} = +V_{DD} + 0.5$	10		10		
ADS7830 HARDWARE ADDRESSBinaryPOWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Specified Performance4.7555.25VQuiescent CurrentHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz7501000μAPower DissipationHigh-Speed Mode: SCL = 100kHz150μAPower-Down Mode w/Wrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz3.755mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz1.5mWFast Mode: SCL = 400kHz1.5mWFast Mode: SCL = 400kHz1.5mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz0.75mWStandard Mode, SCL = 100kHz35μAFull Power-DownScL Pulled HIGH, SDA Pulled HIGH4003000TEMPERATURE RANGEISOMA		$V_{IL} = -0.3$	-10	Ctroight		μΑ	
ADS7830 HARDWARE ADDRESS10010BinaryPOWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Quiescent CurrentSpecified Performance4.7555.25VQuiescent CurrentHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz7501000μAPower DissipationHigh-Speed Mode: SCL = 100kHz Fast Mode: SCL = 400kHz300μAPower DissipationHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz3.755mWPower-Down Mode w/Wrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz0.75 MWmWFast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz0.75 MOmWPower-DownKithode: SCL = 400kHz Fast Mode: SCL = 100kHz150 MOμAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nATEMPERATURE RANGEISOMOMA	Data Format						
POWER-SUPPLY REQUIREMENTS Power-Supply Voltage, +V _{DD} Quiescent CurrentSpecified Performance4.7555.25VQuiescent CurrentHigh-Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz7501000μAPower DissipationHigh-Speed Mode: SCL = 100kHz150μAPower-Down Mode w/Wrong Address SelectedHigh-Speed Mode: SCL = 3.4MHz3.755mWPower-DownStandard Mode, SCL = 400kHz1.5mWFast Mode: SCL = 400kHz0.75mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz0.75mWFast Mode: SCL = 400kHz150μAWorong Address SelectedFast Mode: SCL = 100kHz35μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nATEMPERATURE RANGEISOISOISOISO	ADS7830 HARDWARE ADDRESS		1	-		Binary	
Power-Supply Voltage, +VDDSpecified Performance4.7555.25VQuiescent CurrentHigh-Speed Mode: SCL = 3.4MHz7501000μAFast Mode: SCL = 400kHz300μAStandard Mode, SCL = 100kHz150μAPower DissipationHigh-Speed Mode: SCL = 3.4MHz3.755Fast Mode: SCL = 400kHz1.5mWFast Mode: SCL = 400kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 100kHz400μAw/Wrong Address SelectedFast Mode: SCL = 400kHz150μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nATEMPERATURE RANGEImage: SelectedImage: SelectedImage: SelectedImage: Selected		1	1				
Quiescent CurrentHigh-Speed Mode: SCL = 3.4 MHz7501000 μ AFast Mode: SCL = 400 kHz300 μ AStandard Mode, SCL = 100 kHz150 μ APower DissipationHigh-Speed Mode: SCL = 3.4 MHz 3.75 5Fast Mode: SCL = 400 kHz1.5mWFast Mode: SCL = 400 kHz1.5mWPower-Down ModeHigh-Speed Mode: SCL = 3.4 MHz 0.75 mWPower-Down ModeHigh-Speed Mode: SCL = 400 kHz 0.75 mWFast Mode: SCL = 400 kHz 150 μ Aw/Wrong Address SelectedFast Mode: SCL = 400 kHz 150 μ AFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH 400 3000 nATEMPERATURE RANGEImage: Standard Mode, SCL = 100 kHzImage: Standard Mode, SCL = 100 kHz <t< td=""><td></td><td>Specified Performance</td><td>4.75</td><td>5</td><td>5.25</td><td>V</td></t<>		Specified Performance	4.75	5	5.25	V	
Fast Mode: SCL = 400kHz300μAPower DissipationHigh-Speed Mode; SCL = 100kHz150μAPower-Down ModeHigh-Speed Mode: SCL = 3.4MHz3.755mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 3.4MHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 400kHz0.75mWFast Mode: SCL = 400kHz150μAw/Wrong Address SelectedFast Mode: SCL = 400kHz150μAStandard Mode, SCL = 100kHz35μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000TEMPERATURE RANGEImage: Standard Mode, SCL = 100kHzImage: Standard Mode, SCL = 100kHzImage: Standard Mode, SCL = 100kHz						-	
Standard Mode, SCL = 100kHz150µAPower DissipationHigh-Speed Mode: SCL = 3.4MHz3.755mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 100kHz0.75mWw/Wrong Address SelectedFast Mode: SCL = 400kHz150µAFull Power-DownSCL = 400kHz150µAStandard Mode, SCL = 100kHz35µATemperAture RANGESCL Pulled HIGH, SDA Pulled HIGH4003000							
Power DissipationHigh-Speed Mode: SCL = 3.4MHz3.755mWFast Mode: SCL = 400kHz1.5mWStandard Mode, SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 3.4MHz400μAw/Wrong Address SelectedFast Mode: SCL = 400kHz150μAStandard Mode, SCL = 100kHz35μAStandard Mode, SCL = 100kHz35μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000TEMPERATURE RANGEImage: Standard Mode, SDA Pulled HIGHImage: Standard Mode, SDA Pulled HIGHImage: Standard Mode, SDA Pulled HIGH							
Standard Mode, SCL = 100kHz0.75mWPower-Down ModeHigh-Speed Mode: SCL = 3.4MHz400μAw/Wrong Address SelectedFast Mode: SCL = 400kHz150μAStandard Mode, SCL = 100kHz35μAStandard Mode, SCL = 100kHz35μAFull Power-DownSCL Pulled HIGH, SDA Pulled HIGH4003000nATEMPERATURE RANGEImage: Comparison of the second seco	Power Dissipation			3.75	5	mW	
Power-Down Mode High-Speed Mode: SCL = 3.4MHz 400 μA w/Wrong Address Selected Fast Mode: SCL = 400kHz 150 μA Standard Mode, SCL = 100kHz 35 μA Full Power-Down SCL Pulled HIGH, SDA Pulled HIGH 400 3000 nA TEMPERATURE RANGE							
w/Wrong Address Selected Fast Mode: SCL = 400kHz 150 μA Standard Mode, SCL = 100kHz 35 μA Full Power-Down SCL Pulled HIGH, SDA Pulled HIGH 400 3000 nA TEMPERATURE RANGE Image: Comparison of the second sec							
Standard Mode, SCL = 100kHz 35 µA Full Power-Down SCL Pulled HIGH, SDA Pulled HIGH 400 3000 nA TEMPERATURE RANGE Image: Comparison of the second s							
Full Power-Down SCL Pulled HIGH, SDA Pulled HIGH 400 3000 nA TEMPERATURE RANGE	w/Wrong Address Selected						
TEMPERATURE RANGE	Full Power Down				2000		
				400	3000	na	
			40		05		

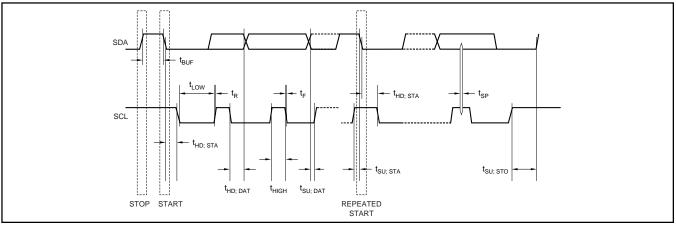
NOTES: (1) LSB means Least Significant Bit. When $V_{REF} = 5.0V$, 1LSB is 19.5mV.

(2) kSPS means kilo samples-per-second.

(3) THD measured out to the 9th-harmonic.



TIMING DIAGRAM



TIMING CHARACTERISTICS⁽¹⁾

At T_{A} = –40°C to +85°C, +V_{\text{DD}} = +2.7V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f _{SCL}	Standard Mode Fast Mode High-Speed Mode, C _B = 100pF max High-Speed Mode, C _B = 400pF max		100 400 3.4 1.7	kHz kHz MHz MHz
Bus Free Time Between a STOP and START Condition	t _{BUF}	Standard Mode Fast Mode	4.7 1.3		μs μs
Hold Time (Repeated) START Condition	t _{HD} ; _{STA}	Standard Mode Fast Mode High-Speed Mode	4.0 600 160		μs ns ns
LOW Period of the SCL Clock	t _{LOW}	$\begin{array}{l} {\rm Standard\ Mode}\\ {\rm Fast\ Mode}\\ {\rm High-Speed\ Mode,\ C_B}=100 {\rm pF\ max^{(2)}}\\ {\rm High-Speed\ Mode,\ C_B}=400 {\rm pF\ max^{(2)}} \end{array}$	4.7 1.3 160 320		μs μs ns ns
HIGH Period of the SCL Clock	t _{ніGн}	$\begin{array}{l} {\rm Standard\ Mode}\\ {\rm Fast\ Mode}\\ {\rm High-Speed\ Mode,\ C_B}=100 {\rm pF\ max^{(2)}}\\ {\rm High-Speed\ Mode,\ C_B}=400 {\rm pF\ max^{(2)}} \end{array}$	4.0 600 60 120		μs ns ns ns
Setup Time for a Repeated START Condition	t _{SU} ; _{STA}	Standard Mode Fast Mode High-Speed Mode	4.7 600 160		μs ns ns
Data Setup Time	t _{SU} ; _{DAT}	Standard Mode Fast Mode High-Speed Mode	250 100 10		ns ns ns
Data Hold Time	t _{hd} ; _{dat}	$\begin{array}{l} \mbox{Standard Mode} \\ \mbox{Fast Mode} \\ \mbox{High-Speed Mode, C}_{\rm B} = 100 \mbox{pF max}^{(2)} \\ \mbox{High-Speed Mode, C}_{\rm B} = 400 \mbox{pF max}^{(2)} \end{array}$	0 0 0 ⁽³⁾ 0 ⁽³⁾	3.45 0.9 70 150	μs μs ns ns
Rise Time of SCL Signal t _{RCL}		$\begin{array}{l} \mbox{Standard Mode} \\ \mbox{Fast Mode} \\ \mbox{High-Speed Mode, C}_{\rm B} = 100 \mbox{pF max}^{(2)} \\ \mbox{High-Speed Mode, C}_{\rm B} = 400 \mbox{pF max}^{(2)} \end{array}$	20 + 0.1C _B 10 20	1000 300 40 80	ns ns ns ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t _{RCL1}	$\begin{array}{l} {\rm Standard\ Mode}\\ {\rm Fast\ Mode}\\ {\rm High-Speed\ Mode,\ C_B}=100 {\rm pF\ max^{(2)}}\\ {\rm High-Speed\ Mode,\ C_B}=400 {\rm pF\ max^{(2)}} \end{array}$	20 + 0.1C _B 10 20	1000 300 80 160	ns ns ns ns
Fall Time of SCL Signal t _{FCL}		$\begin{array}{l} {\rm Standard\ Mode} \\ {\rm Fast\ Mode} \\ {\rm High-Speed\ Mode,\ C_B} = 100 {\rm pF\ max^{(2)}} \\ {\rm High-Speed\ Mode,\ C_B} = 400 {\rm pF\ max^{(2)}} \end{array}$	20 + 0.1C _B 10 20	300 300 40 80	ns ns ns ns

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.

(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated. (3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.





TIMING CHARACTERISTICS⁽¹⁾ (Cont.)

At $T_A = -40^{\circ}C$ to +85°C, +V_{DD} = +2.7V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Rise Time of SDA Signal	t _{RDA}	Standard Mode		1000	ns
-		Fast Mode	20 + 0.1C _B	300	ns
		High-Speed Mode, C _B = 100pF max ⁽²⁾	10	80	ns
		High-Speed Mode, $C_B = 400 pF max^{(2)}$	20	160	ns
Fall Time of SDA Signal	t _{FDA}	Standard Mode		300	ns
		Fast Mode	20 + 0.1C _B	300	ns
		High-Speed Mode, C _B = 100pF max ⁽²⁾	10	80	ns
		High-Speed Mode, $C_B = 400 pF max^{(2)}$	20	160	ns
Setup Time for STOP Condition	t _{su} ; _{sтo}	Standard Mode	4.0		μs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Capacitive Load for SDA and SCL Line	C _B			400	pF
Pulse Width of Spike Suppressed	t _{SP}	Fast Mode		50	ns
	0.	High-Speed Mode		10	ns
Noise Margin at the HIGH Level for		Standard Mode			
Each Connected Device (Including	V _{NH}	Fast Mode	0.2V _{DD}		V
Hysteresis)		High-Speed Mode			
Noise Margin at the LOW Level for		Standard Mode			
Each Connected Device (Including	V _{NL}	Fast Mode	0.1V _{DD}		V
Hysteresis)		High-Speed Mode			

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.

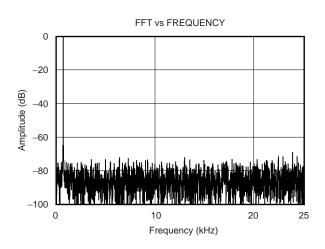
(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated.

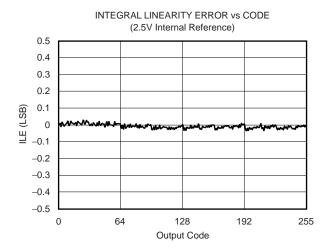
(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

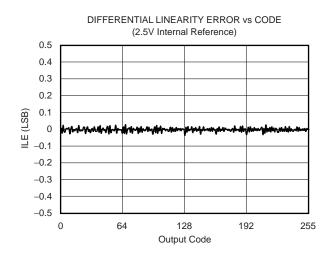


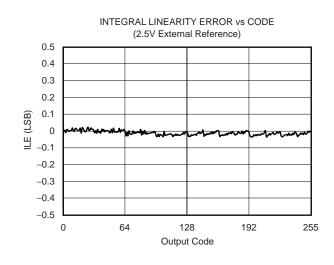
TYPICAL CHARACTERISTICS

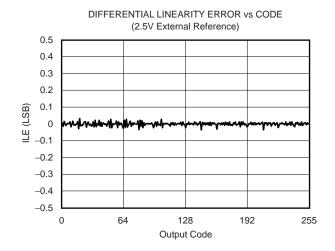
 T_{A} = +25°C, V_{DD} = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.

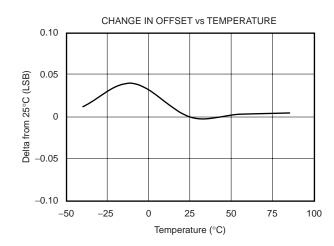










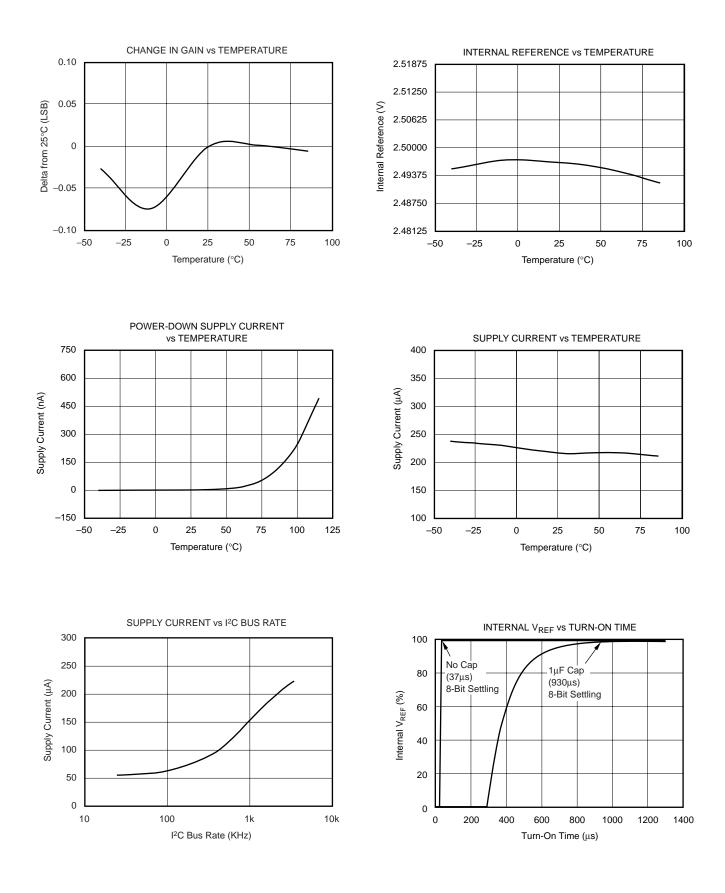






TYPICAL CHARACTERISTICS (Cont.)

 $T_{A} = +25^{\circ}C, V_{DD} = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.$





THEORY OF OPERATION

The ADS7830 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sampleand-hold function. The converter is fabricated on a 0.6μ CMOS process.

The ADS7830 core is controlled by an internally generated free-running clock. When the ADS7830 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The simplified diagram of input and output for the ADS7830 is shown in Figure 1.

ANALOG INPUT

When the converter enters the hold mode, the voltage on the selected CHx pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

REFERENCE

The ADS7830 can operate with an internal 2.5V reference or an external reference. If a +5V supply is used, an external +5V reference is required in order to provide full dynamic range for a 0V to $+V_{DD}$ analog input. This external reference can be as low as 50mV. When using a +2.7V supply, the internal +2.5V reference will provide full dynamic range for a 0V to $+V_{DD}$ analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 256. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.02LSB peak-topeak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—1LSB. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

DIGITAL INTERFACE

The ADS7830 supports the I²C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The ADS7830 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

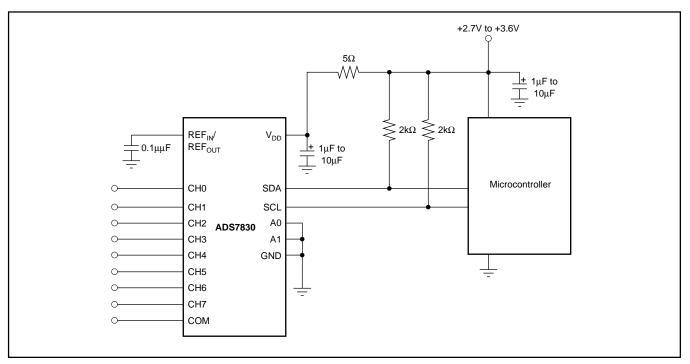


FIGURE 1. Simplified I/O of the ADS7830.



The following bus protocol has been defined (as shown in Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid: The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

Within the I²C bus specifications a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The ADS7830 works in all three modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/\overline{W} bit, two types of data transfer are possible:

- 1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- 2. Data transfer from a slave transmitter to a master receiver. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7830 may operate in the following two modes:

- Slave Receiver Mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave Transmitter Mode: The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7830 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

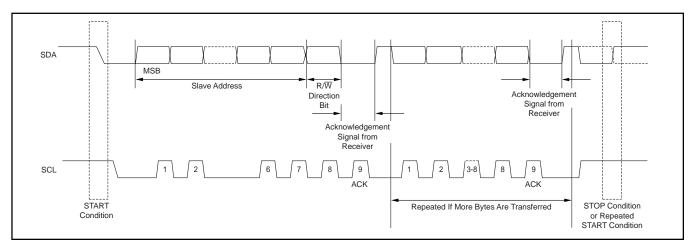


FIGURE 2. Basic Operation of the ADS7830.





Address Byte

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/W

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7830 determine these two bits of the device address for a particular ADS7830. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

The A1-A0 Address Inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up of the ADS7830.

The last bit of the address byte (R/\overline{W}) defines the operation to be performed. When set to a '1' a read operation is selected; when set to a '0' a write operation is selected. Following the START condition the ADS7830 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/\overline{W} bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	х	х

The ADS7830 operating mode is determined by a command byte which is illustrated above.

- SD: Single-Ended/Differential Inputs
 - 0: Differential Inputs
 - 1: Single-Ended Inputs
- C2 C0: Channel Selections
- PD1 0: Power-Down Selection
 - X: Unused

See Table I for a power-down selection summary.

See Table II for a channel selection control summary.

PD1	PD0	DESCRIPTION				
0	0	Power Down Between A/D Converter Conversions				
0	1	ternal Reference OFF and A/D Converter ON				
1	0	Internal Reference ON and A/D Converter OFF				
1	1	Internal Reference ON and A/D Converter ON				

TABLE I. Power-Down Selection

					CHANNEL	SELECTIO	N CONTRO	L				
SD	C2	C1	C0	CH0	CH1	CH2	СНЗ	CH4	CH5	CH6	CH7	СОМ
0	0	0	0	+IN	–IN	—	—	—	—	—	—	_
0	0	0	1	_	—	+IN	–IN	_	-	—	—	—
0	0	1	0		—	—	—	+IN	–IN	—	—	—
0	0	1	1		—	—	—	_	_	+IN	-IN	—
0	1	0	0	-IN	+IN	—	—	_	_	—	—	—
0	1	0	1	—	—	–IN	+IN	-	-	—	—	—
0	1	1	0	—	—	_	—	–IN	+IN	—	-	—
0	1	1	1	—	—	_	—	-	-	–IN	+IN	—
1	0	0	0	+IN	—	—	—	-	_	_	—	–IN
1	0	0	1	—	—	+IN	—	-	-	—	—	–IN
1	0	1	0	—	—	_	—	+IN	-	—	-	–IN
1	0	1	1	—			—	1		+IN	-	–IN
1	1	0	0	—	+IN	-	—				_	–IN
1	1	0	1	—	-		+IN	1	Ι		-	–IN
1	1	1	0	—			—	1	+IN		-	–IN
1	1	1	1	—	_	_	_	_	_	—	+IN	–IN

TABLE II. Channel Selection Control Addressed by Command BYTE.

INITIATING CONVERSION

Provided the master has write-addressed it, the ADS7830 turns on the A/D converter section and begins conversions when it receives BIT 4 of the command byte shown in the Command Byte. If the command byte is correct, the ADS7830 will return an ACK condition.

READING DATA

Data can be read from the ADS7830 by read-addressing the part (LSB of address byte set to '1') and receiving the transmitted byte. Converted data can only be read from the ADS7830 once a conversion has been initiated as described in the preceding section.

Each 8-bit data word is returned in one byte, as shown below, where D7 is the MSB of the data word, and D0 is the LSB.

	MSB	6	5	4	3	2	1	LSB
DATA	D7	D6	D5	D4	D3	D2	D1	D0

READING IN F/S MODE

Figure 3 describes the interaction between the master and the slave ADS7830 in Fast or Standard (F/S) mode. At the end of reading conversion data the ADS7830 can be issued a repeated START condition by the master to secure bus operation for subsequent conversions of the A/D converter. This would be the most efficient way to perform continuous conversions.

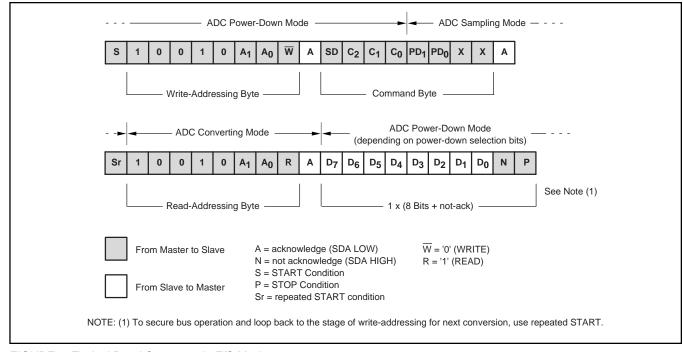


FIGURE 3. Typical Read Sequence in F/S Mode.

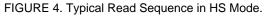




READING IN HS MODE

High Speed (HS) mode is fast enough that codes can be read out one at a time. In HS mode, there is not enough time for a single conversion to complete between the reception of a repeated START condition and the read-addressing byte, so the ADS7830 stretches the clock after the read-addressing byte has been fully received, holding it LOW until the conversion is complete. See Figure 4 for a typical read sequence for HS mode. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a conversion; to do this, issue a repeated START instead of a STOP at the end of the read sequence, since a STOP causes the part to return to F/S mode.

F/S Mode	-
S 0 0 0 0 1 X	XXN
HS Mode Master Co	de
HS Mode Enabled -	ver-Down Mode ————————————————————————————————————
Sr 1 0 0 1 0 A ₁	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$
Write-Addressing By	te Command Byte
ADC Converting N	Iode
Sr 1 0 0 1 0 A ₁	A0 R A SCLH ⁽²⁾ is stretched LOW waiting for data conversion
HS Mode Enabled	Return to F/S Mode ⁽¹⁾
(depending on power-down s D7 D6 D5 D4 D3 D2 D1	
1 x (8 Bits + not-acl	<)
From Master to Slave	A = acknowledge (SDA LOW) \overline{W} = '0' (WRITE)N = not acknowledge (SDA HIGH)R = '1' (READ)S = STABT Condition
From Slave to Master	S = START Condition P = STOP Condition Sr = repeated START condition
NOTES: (1) To remain in HS mode, (2) SCLH is SCL in HS mo	use repeated START instead of STOP.







READING WITH REFERENCE ON/OFF

The internal reference defaults to off when the ADS7830 power is on. To turn the internal reference on or off, see Table I. If the reference (internal or external) is constantly turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the configuration.

See Figure 5 for an example of the proper internal reference turn-on sequence before issuing the typical read sequences required for the F/S mode when an internal reference is used.

When using an internal reference, there are three things that must be done:

- In order to use the internal reference, the PD1 bit of Command Byte must always be set to logic '1' for each sample conversion that is issued by the sequence, as shown in Figure 3.
- In order to achieve 8-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered, as shown in the

Internal V_{REF} vs Turn-On Time Typical Characteristic plot. If the PD1 bit has been set to logic '0' while using the ADS7830, then the settling time must be reconsidered after PD1 is set to logic '1'. In other words, whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 8-bit accuracy conversion.

3) When the internal reference is off, it is not turned on until both the first Command Byte with PD1 = '1' is sent and then a STOP condition or repeated START condition is issued. (The actual turn-on time occurs once the STOP or repeated START condition is issued.) Any Command Byte with PD1 = '1' issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any Command Byte with PD1 = '0'.

The example in Figure 5 can be generalized for a HS mode conversion cycle by simply swapping the timing of the conversion cycle.

If using an external reference, PD1 must be set to '0', and the external reference must be settled. The typical sequence in Figure 3 or Figure 4 can then be used.

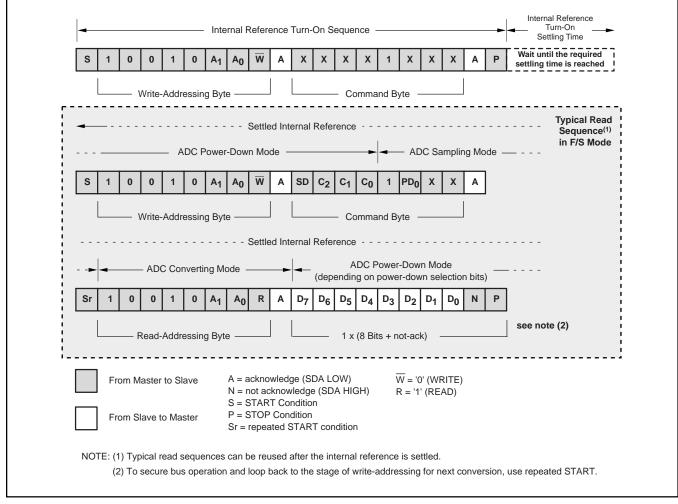


FIGURE 5. Internal Reference Turn-On Sequence and Typical Read Sequence (F/S mode shown).



LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7830 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an "n-bit" SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7830 should be clean and well-bypassed. A 0.1μ F ceramic bypass capacitor should be placed as close to the device as possible. A 1μ F to 10μ F capacitor may also be needed if the impedance of the connection between +V_{DD} and the power supply is high.

The ADS7830 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS7830IPWR	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7830IPWRG4	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7830IPWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7830IPWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address:

Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated