

Document Title

32Kx8 bit Low Power CMOS Static RAM

Revision History

Revision No	History	Draft Data	Remark
0.0	Initial draft	May 18th 1997	Design target
0.1	First revision - KM62256DL/DLI I _{SB1} = 100 → 50μA KM62256DL-L I _{SB1} = 20 → 10μA KM62256DLI-L I _{SB1} = 50 → 15μA - C _{IN} = 6 → 8pF, C _{IO} = 8 → 10pF - KM62256D-4/5/7 Family t _{OH} = 5 → 10ns - KM62256DL/DLI I _{DR} = 50→30μA KM62256DL-L/DLI-L I _{DR} = 30 → 15μA	April 1st 1997	Preliminily
1.0	Finalize - Remove I _{CC} write value - Improved operating current I _{CC2} = 70 → 60mA - Improved standby current KM62256DL/DLI I _{SB1} = 50 → 30μA KM62256DL-L I _{SB1} = 10 → 5μA KM62256DLI-L I _{SB1} = 15 → 5μA - Improved data retention current KM62256DL/DLI I _{DR} = 30 → 5μA KM62256DL-L/DLI-L I _{DR} = 15 → 3μA - Remove 45ns part from commercial product and 100ns part from industrial product. Replace test load 100pF to 50pF for 55ns part	November 11th 1997	Final

The attached datasheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserves the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

KM62256D Family

CMOS SRAM

32Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 28-DIP-600B, 28-SOP-450
28-TSOP1-0813.4F, 28-TSOP1-0813.4R

GENERAL DESCRIPTION

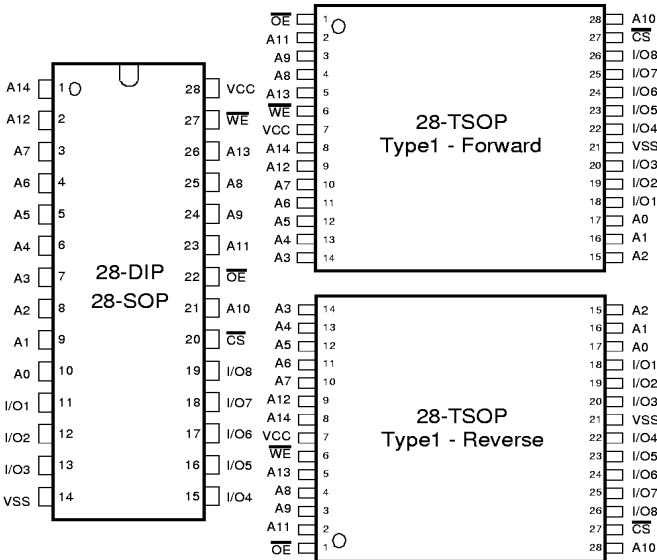
The KM62256D family is fabricated by SAMSUNG's advanced CMOS process technology. The family support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature.	Speed (ns)	PKG Type	Power Dissipation	
				Standby (Isb1, Max)	Operating (Icc2, Max)
KM62256DL KM62256DL-L	Commercial (0~70°C)	55 ¹⁾ /70ns	28-DIP,28-SOP 28-TSOP1-F/R	30μA 5μA	60mA
KM62256DLI KM62256DLI-L	Industrial (-40~85°C)	70ns	28-SOP 28-TSOP1-F/R	30μA 5μA	

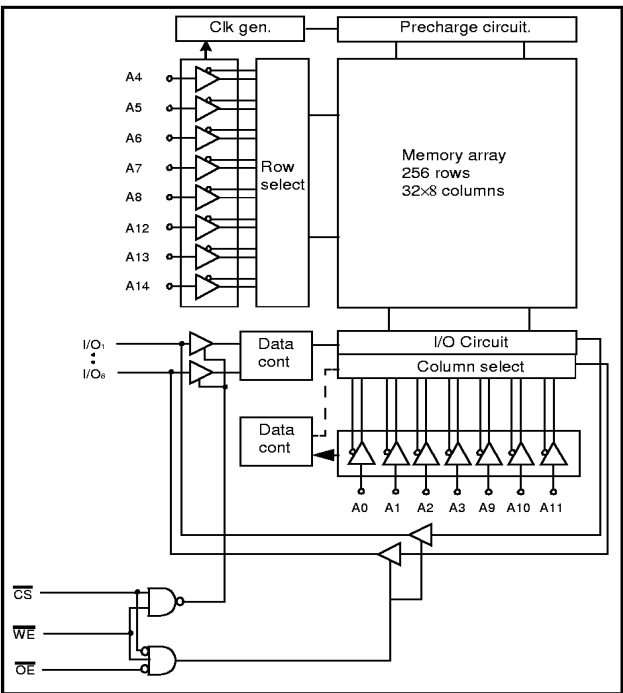
1. The parameter is tested with 50pF test load.

PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
A0~A14	Address Inputs	I/O1~I/O8	Data Inputs/Outputs
WE	Write Enable Input	Vcc	Power
CS	Chip Select Input	Vss	Ground
OE	Output Enable Input	NC	No connect

FUNCTIONAL BLOCK DIAGRAM



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KM62256D Family

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PRODUCT LIST

Commercial Temp Product (0~70°C)		Industrial Temp Products (-40~85°C)	
Part Name	Function	Part Name	Function
KM62256DLP-5	28-DIP, 55ns, L-pwr	KM62256DLGI-7	28-SOP, 70ns, L-pwr
KM62256DLP-5L	28-DIP, 55ns, LL-pwr	KM62256DLGI-7L	28-SOP, 70ns, LL-pwr
KM62256DLP-7	28-DIP, 70ns, L-pwr	KM62256DLTGI-7	28-TSOP F, 70ns, L-pwr
KM62256DLP-7L	28-DIP, 70ns, LL-pwr	KM62256DLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256DLG-5	28-SOP, 50ns, L-pwr	KM62256DLRGI-7	28-TSOP R, 70ns, L-pwr
KM62256DLG-5L	28-SOP, 50ns, LL-pwr	KM62256DLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256DLG-7	28-SOP, 70ns, L-pwr		
KM62256DLG-7L	28-SOP, 70ns, LL-pwr		
KM62256DLTG-5	28-TSOP F, 55ns, L-pwr		
KM62256DLTG-5L	28-TSOP F, 55ns, LL-pwr		
KM62256DLTG-7	28-TSOP F, 70ns, L-pwr		
KM62256DLTG-7L	28-TSOP F, 70ns, LL-pwr		
KM62256DLRG-5	28-TSOP R, 55ns, L-pwr		
KM62256DLRG-5L	28-TSOP R, 55ns, LL-pwr		
KM62256DLRG-7	28-TSOP R, 70ns, L-pwr		
KM62256DLRG-7L	28-TSOP R, 70ns, LL-pwr		

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS ¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM62256DL
		-40 to 85	°C	KM62256DLI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V _{IH}	2.2	-	Vcc+0.5V ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

- Note:
- 1. Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
 - 2. Overshoot : V_{CC}+3.0V in case of pulse width≤30ns
 - 3. Undershoot : -3.0V in case of pulse width≤30ns
 - 4. Overshoot and undershoot is sampled, not 100% tested

CAPACITANCE ¹⁾ (f=1 MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled not, 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{ss} to V _{cc}		-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}$ =V _{IH} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{ss} to V _{cc}		-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}$ =V _{IL} , V _{IN} =V _{IH} or V _{IL} , Read		-	5	10	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA	Read	-	2	5	mA
		$\overline{CS}$ ≤0.2V, V _{IN} ≤0.2V, V _{IN} ≥V _{cc} -0.2V	Write		-	20	
	I _{CC2}	Cycle time=Min,100% duty, I _{IO} =0mA, $\overline{CS}$ =V _{IL} , V _{IN} =V _{IH} or V _{IL}		-	45	60	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA		-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}$ =V _{IH} , Other inputs=V _{IH} or V _{IL}		-	-	1	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}$ ≥V _{cc} -0.2V, Other inputs=0~V _{cc}	Low Power	-	1	30	μA
			Low Low Power	-	0.2	5	μA

KM62256D Family

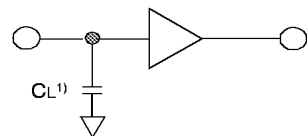
CMOS SRAM

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V
Input rising and falling time : 5ns
input and output reference voltage : 1.5V
Output load (See right) :CL=100pF+1TTL
CL=50¹⁾pF+1TTL

1. Refer to AC characteristics.



1. Including scope and jig capacitance

AC CHARACTERISTICS (Vcc=4.5~5.5V, KM62256D Family : TA=0 to 70°C, KM62256DI Family : TA=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55 ¹⁾ ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	ns
	Address access time	tAA	-	55	-	70	ns
	Chip select to output	tCO	-	55	-	70	ns
	Output enable to valid output	tOE	-	25	-	35	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	30	ns
	Output hold from address change	tOH	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	ns
	Chip select to end of write	tCW	45	-	60	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	ns
	Write pulse width	tWP	40	-	50	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	ns
	Data to write time overlap	tDW	25	-	30	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

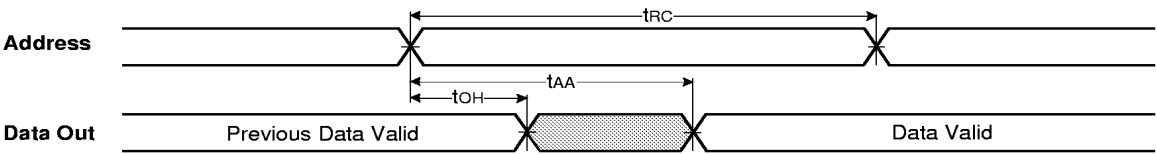
1. The parameter is tested with 50pF test load.

DATA RETENTION CHARACTERISTICS

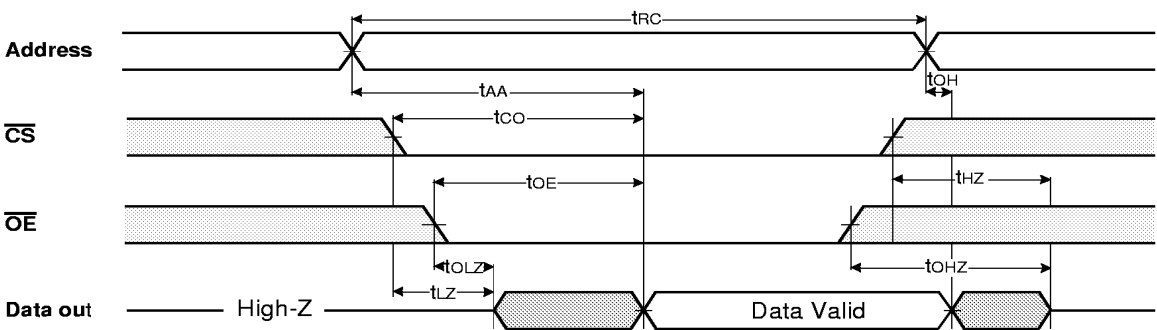
Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_i \wedge V_{cc}-0.2V$		2.0	-	5.5	V
Data retention current	IDR	$V_{cc}=3.0V, \overline{CS}_i \wedge V_{cc}-0.2V$	L-Ver	-	1	15	S _i
			LL-Ver	-	0.2	3	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ms
Recovery time	tRDR			5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)

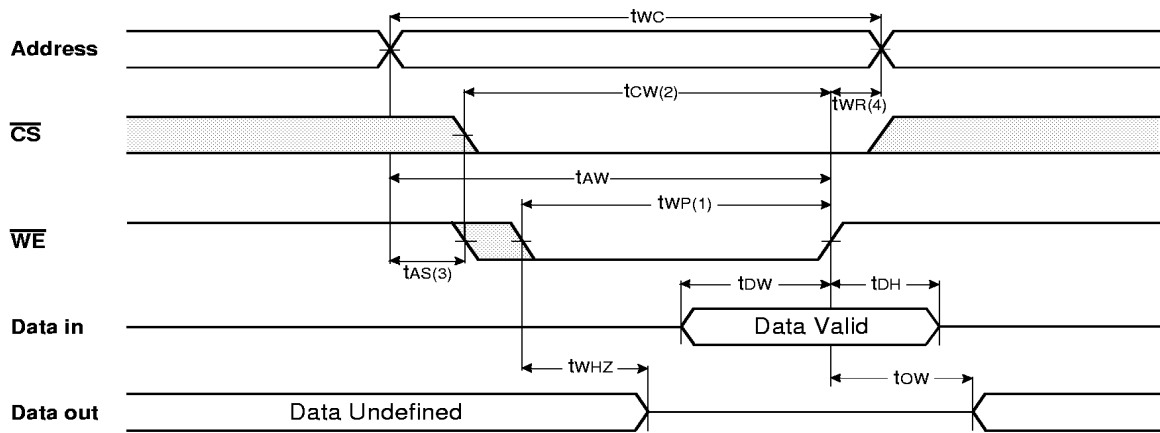


TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

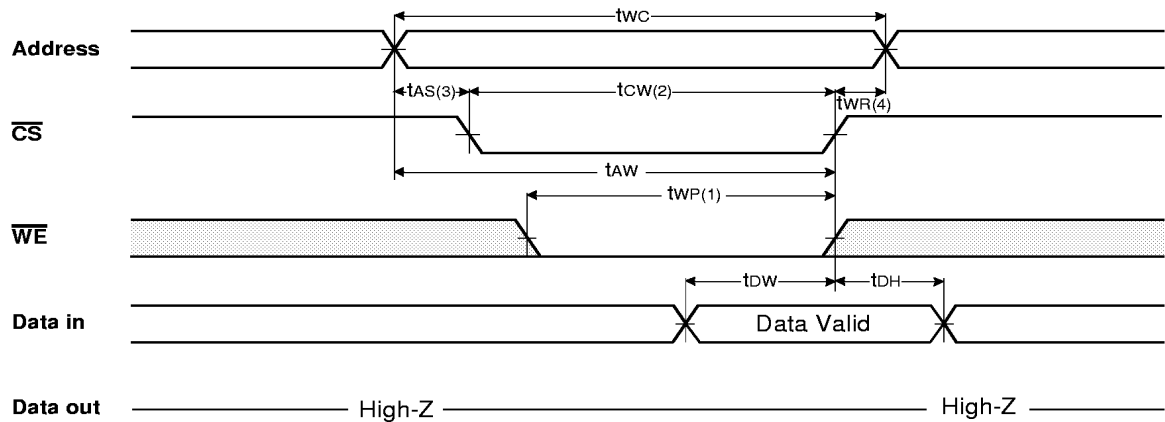


- NOTES (READ CYCLE)
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
 2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)

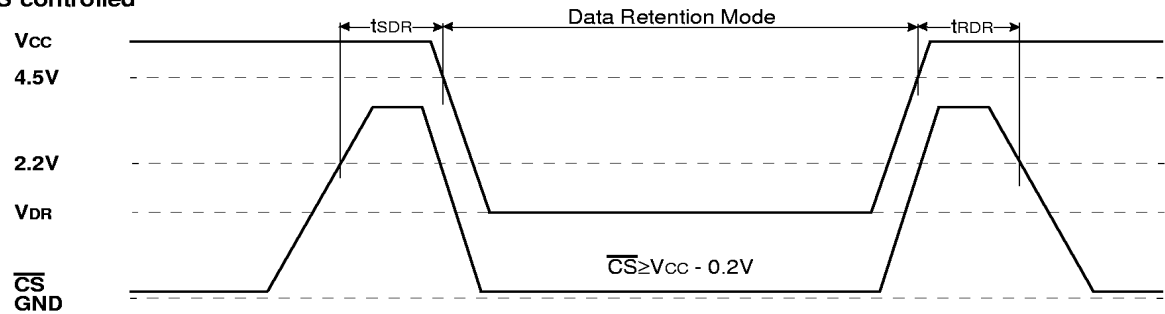


NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
- 2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
- 3. t_{AS} is measured from the address valid to the beginning of write.
- 4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

CS controlled



CMOS SRAM

Units :mm(inch)

28 PIN DUAL IN LINE PACKAGE(600mil)

The drawing illustrates the mechanical specifications of a 28-pin DIP package. Key dimensions include:

- Top View:** Shows the package footprint with pin locations #1, #14, #15, and #28. The width is 13.60 ± 0.20 mm (0.535 ± 0.008 in).
- Side View:** Shows the package height as 15.24 ± 0.600 mm. The pin height is 0.25 ± 0.10 mm (0.010 ± 0.004 in) with a tolerance of -0.05 to -0.002 mm.
- End View:** Shows the pin pitch and individual pin dimensions. The overall length is 36.72 ± 1.446 mm MAX. The distance between the center of the package and the center of the pins is 36.32 ± 0.20 mm (1.430 ± 0.008 in). The pin pitch is 1.65 ± 0.065 mm. Individual pin dimensions include a width of 0.46 ± 0.10 mm (0.018 ± 0.004 in), a thickness of 1.52 ± 0.10 mm (0.060 ± 0.004 in), and a base width of 2.54 ± 0.100 mm. The distance from the package body to the pin base is 3.81 ± 0.20 mm (0.150 ± 0.008 in). The maximum pin height is 5.08 ± 0.200 mm MAX. The distance from the package body to the pin tip is 3.30 ± 0.30 mm (0.130 ± 0.012 in). The minimum distance from the package body to the pin base is 0.38 ± 0.015 mm MIN.

Technical drawing of a 28-pin DIP package showing top, side, and end views with dimensions in inches and millimeters.

Top View:

- Pin numbers: #1 to #28.
- Overall width: 11.81 ± 0.30 in, 0.465 ± 0.012 mm.
- Overall height: 8.38 ± 0.20 in, 0.330 ± 0.008 mm.
- Distance from pin center to top edge: 11.43 ± 0.450 in.

Side View:

- Pin height: 0.15 ± 0.10 in, -0.05 mm.
- Pin thickness: 0.006 ± 0.004 in, -0.002 mm.
- Distance from pin center to bottom edge: 1.02 ± 0.20 in, 0.040 ± 0.008 mm.

End View:

- Pin pitch: 0.89 ± 0.035 in.
- Pin width: 0.41 ± 0.10 in, 0.016 ± 0.004 mm.
- Pin thickness: 1.27 ± 0.050 in.
- Distance from pin center to bottom edge: 0.05 ± 0.002 in.
- Distance from pin center to top edge: 18.69 ± 0.736 MAX in.
- Distance from pin center to bottom edge: 18.29 ± 0.720 in, 0.20 ± 0.008 mm.
- Distance from pin center to top edge: 2.59 ± 0.102 in, 0.20 ± 0.008 mm.
- Distance from pin center to bottom edge: 3.00 ± 0.118 MAX in.

Notes:

- 0~8, 1~4
- 0.10 MAX, 0.004 MAX

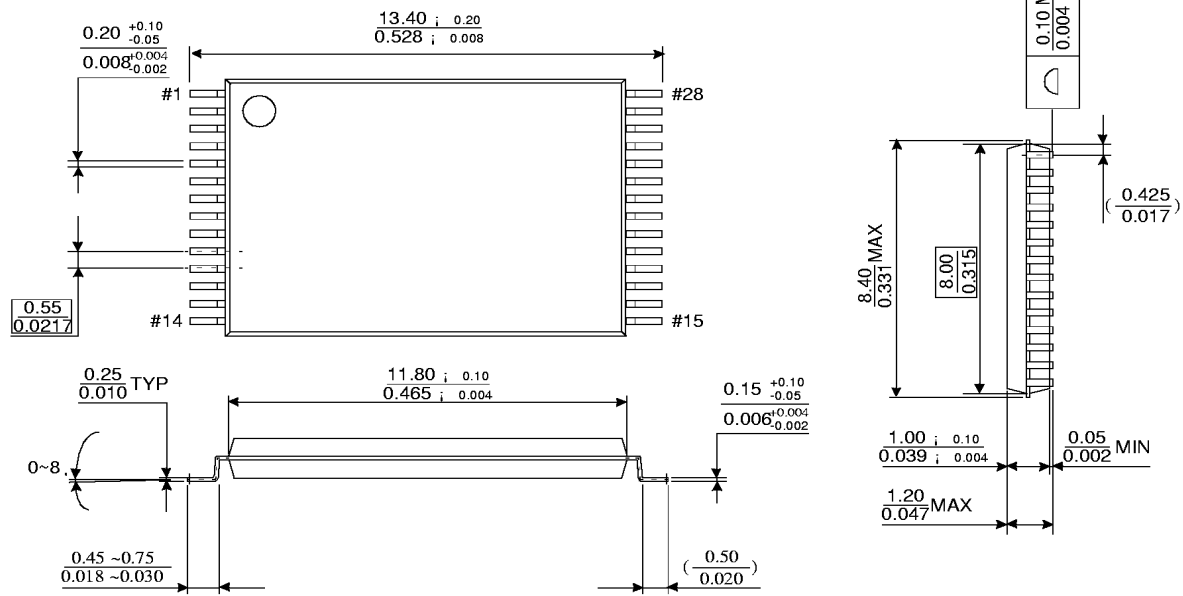
KM62256D Family

CMOS SRAM

PACKAGE DIMENSIONS

Units :mm(Inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)

