BUZ11

Data Sheet June 1999 File Number 2253.2

30A, 50V, 0.040 Ohm, N-Channel Power MOSFET

This is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Formerly developmental type TA9771.

Ordering Information

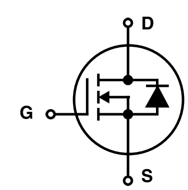
PART NUMBER	PACKAGE	BRAND
BUZ11	TO-220AB	BUZ11

NOTE: When ordering, use the entire part number.

Features

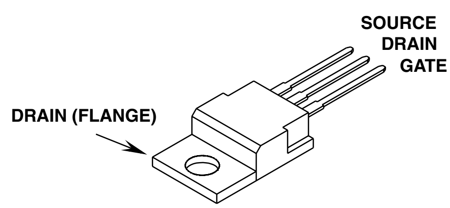
- 30A, 50V
- $r_{DS(ON)} = 0.040\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		BUZ11	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	50	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	50	V
Continuous Drain Current $T_C = 30^oC$	I_D	30	A
Pulsed Drain Current (Note 3)	I_{DM}	120	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	75	W
Linear Derating Factor		0.6	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V	50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA (Figure 9)	2.1	3	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$T_J = 25^oC$, V_{DS} = 50V, V_{GS} = 0V	-	20	250	µA
		$T_J = 125^oC$, V_{DS} = 50V, V_{GS} = 0V	-	100	1000	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 20V, V_{DS} = 0V	-	10	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 15A, V_{GS} = 10V (Figure 8)	-	0.03	0.04	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 25V, I_D = 15A (Figure 11)	4	8	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{CC} = 30V, I_D ≈ 3A, V_{GS} = 10V, R_{GS} = 50Ω, R_L = 10Ω	-	30	45	ns
Rise Time	t_r		-	70	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	180	230	ns
Fall Time	t_f		-	130	170	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 10)	-	1500	2000	pF
Output Capacitance	C_{OSS}		-	750	1100	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	400	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			≤ 1.67		^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			≤ 75		^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	$T_C = 25^oC$	-	-	30	A
Pulsed Source to Drain Current	I_{SDM}	$T_C = 25^oC$	-	-	120	A
Source to Drain Diode Voltage	V_{SD}	$T_J = 25^oC$, I_{SD} = 60A, V_{GS} = 0V	-	1.7	2.6	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 30A, dI_{SD}/dt = 100A/µs, V_R = 30V	-	200	-	ns
Reverse Recovery Charge	Q_{RR}		-	0.25	-	µC

NOTES:

2. Pulse Test: Pulse width ≤ 300ms, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

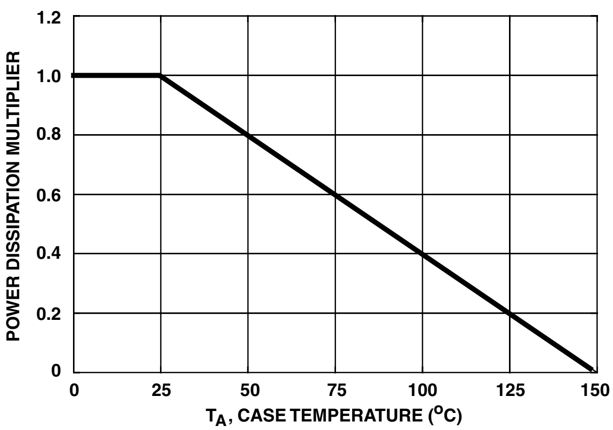


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

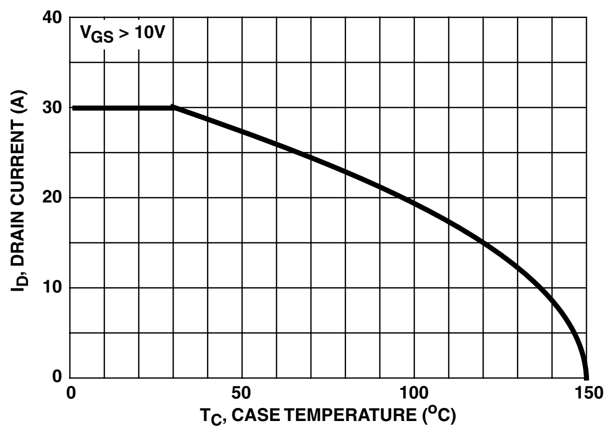


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

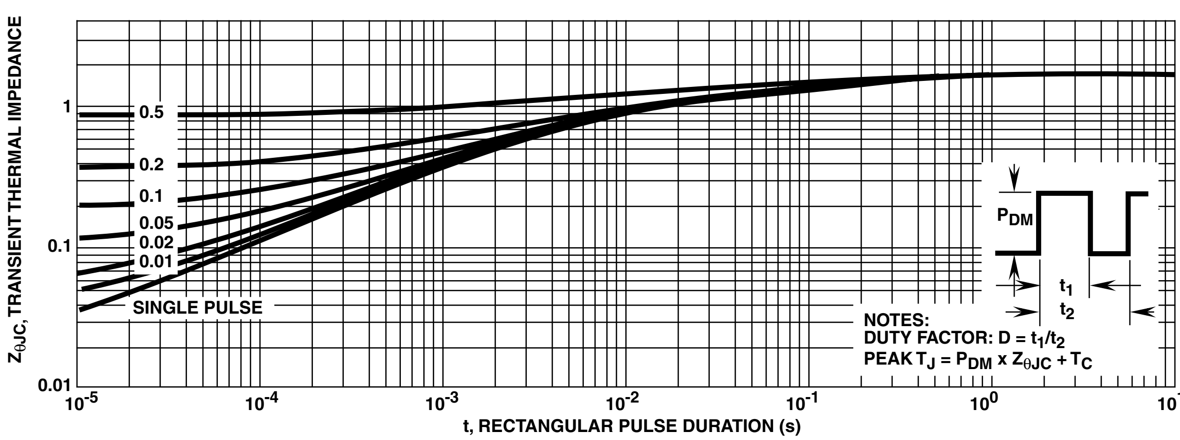


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

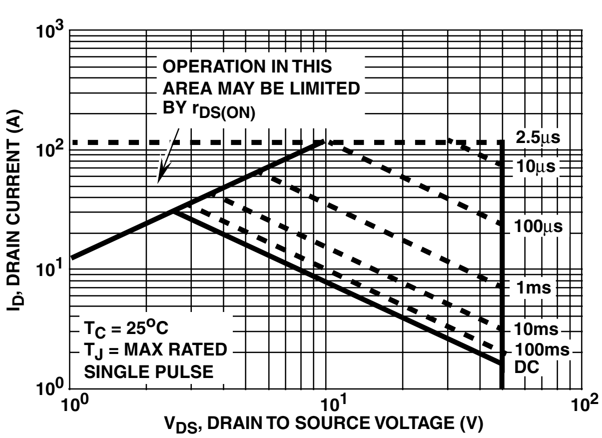


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

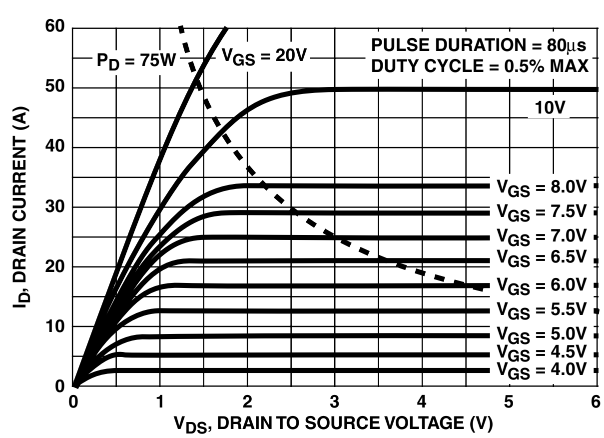


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

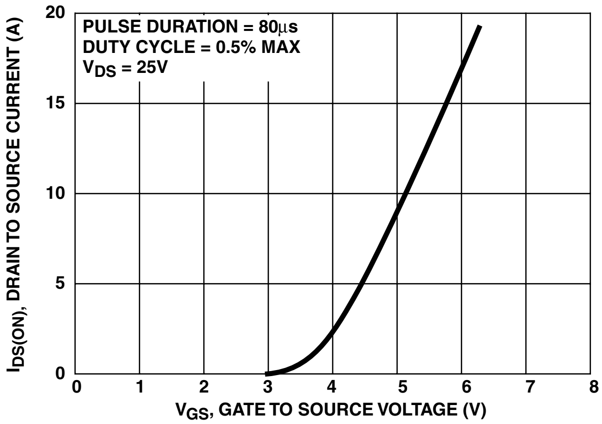


FIGURE 6. TRANSFER CHARACTERISTICS

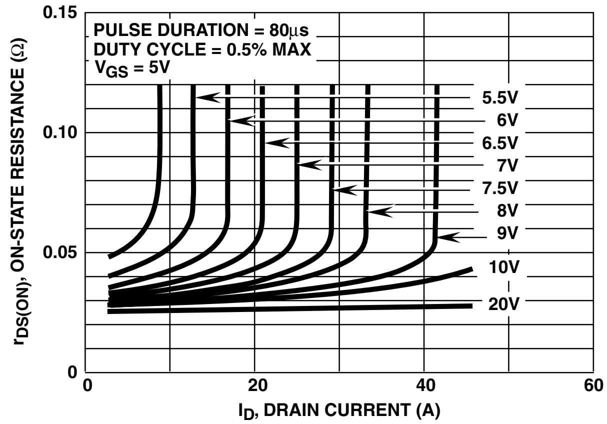


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

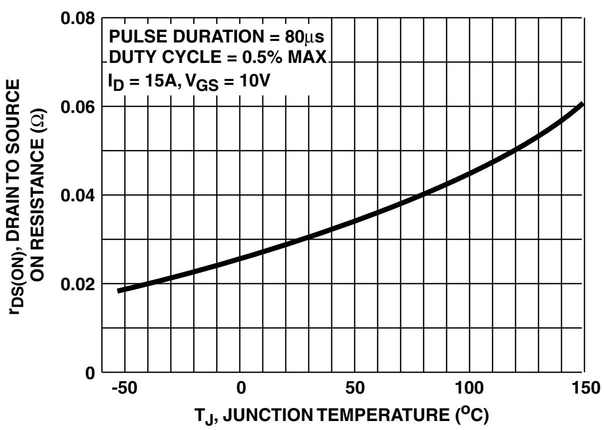


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

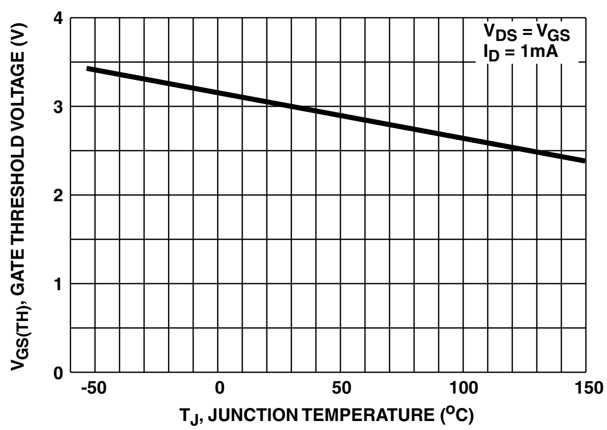


FIGURE 9. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

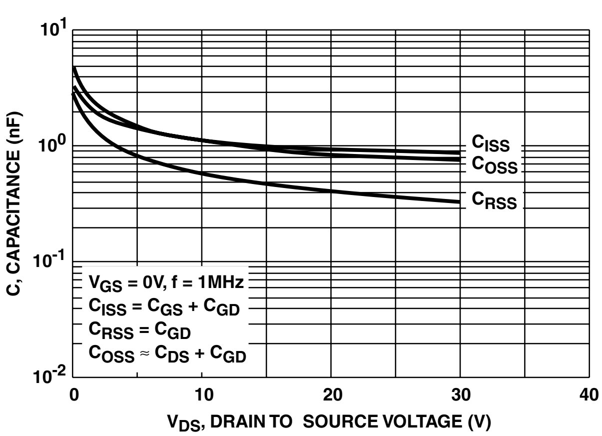


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

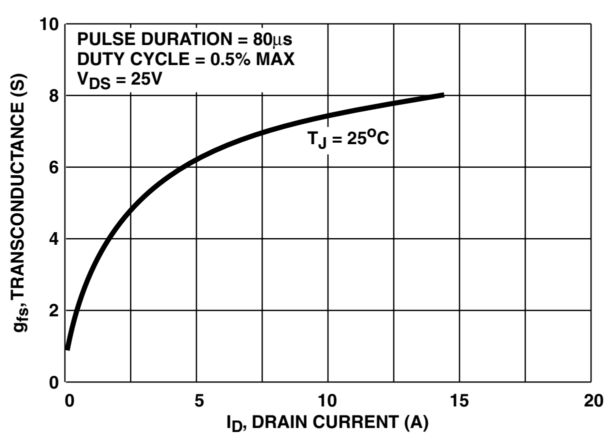


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

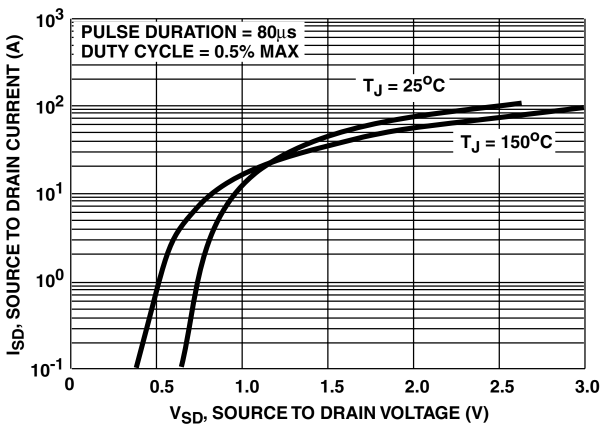


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

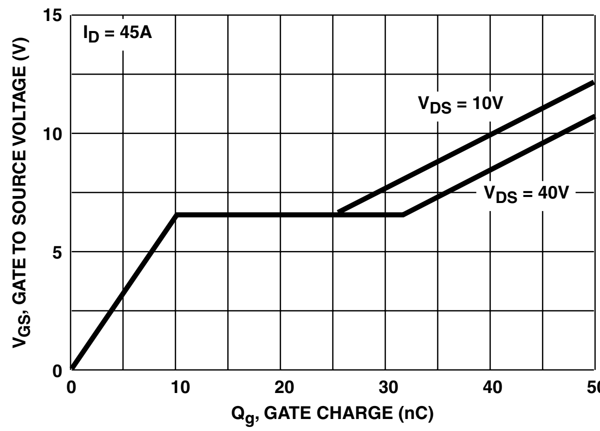


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

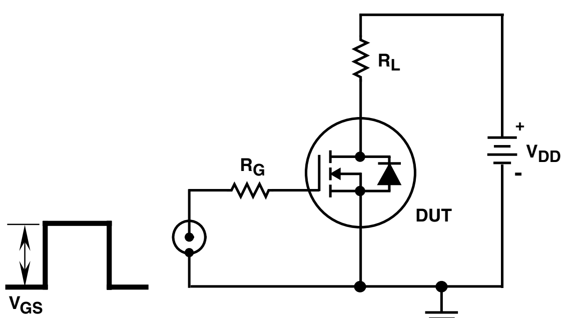


FIGURE 14. SWITCHING TIME TEST CIRCUIT

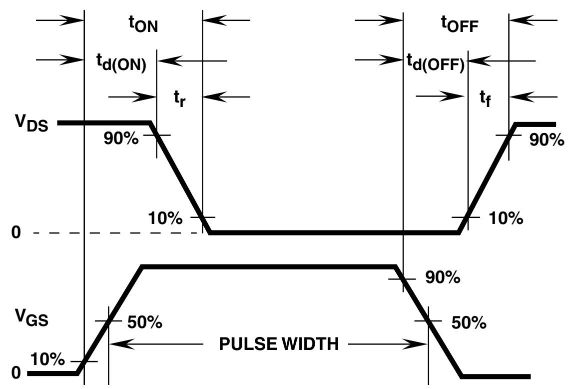


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

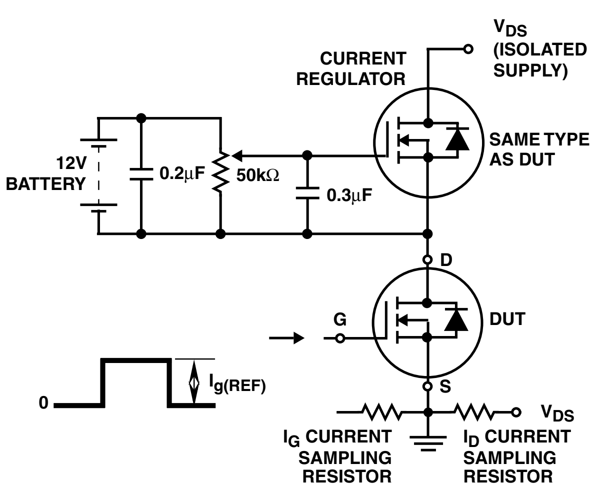


FIGURE 16. GATE CHARGE TEST CIRCUIT

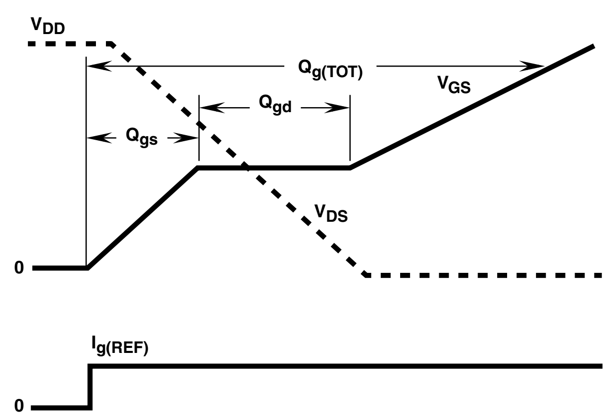


FIGURE 17. GATE CHARGE WAVEFORMS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	PACMAN™	SuperSOT™-3
Bottomless™	FASTr™	POP™	SuperSOT™-6
CoolFET™	GlobalOptoisolator™	PowerTrench ®	SuperSOT™-8
CROSSVOLT™	GTO™	QFET™	SyncFET™
DenseTrench™	HiSeC™	QS™	TinyLogic™
DOME™	ISOPLANAR™	QT Optoelectronics™	UHC™
EcoSPARK™	LittleFET™	Quiet Series™	UltraFET™
E^2CMOS™	MicroFET™	SILENT SWITCHER ®	VCX™
EnSigna™	MICROWIRE™	SMART START™	
FACT™	OPTOLOGIC™	Star* Power™	
FACT Quiet Series™	OPTOPLANAR™	Stealth™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.