

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

High-Speed CMOS Logic Octal Inverting Transparent Latch, Three-State Outputs

Features

- Common Latch-Enable Control
- Common Three-State Output Enable Control
- Buffered Inputs
- Three-State Outputs
- Bus Line Driving Capacity
- Typical Propagation Delay = 13ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$ (Data to Output)
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC533, 'HCT533, 'HC563, and CD74HCT563 are high-speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the three-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent of the state of the output enable.

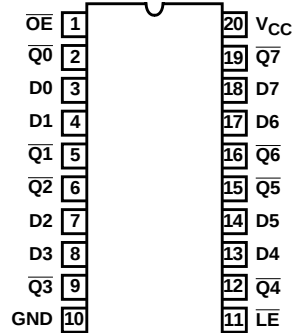
The 'HC533 and 'HCT533 are identical in function to the 'HC563 and CD74HCT563 but have different pinouts. The 'HC533 and 'HCT533 are similar to the 'HC373 and 'HCT373; the latter are non-inverting types.

Ordering Information

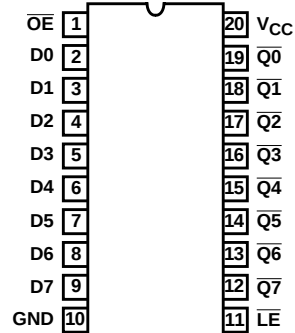
PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE
CD54HC533F3A	-55 to 125	20 Ld CERDIP
CD54HC563F3A	-55 to 125	20 Ld CERDIP
CD54HCT533F3A	-55 to 125	20 Ld CERDIP
CD74HC533E	-55 to 125	20 Ld PDIP
CD74HC563E	-55 to 125	20 Ld PDIP
CD74HC563M	-55 to 125	20 Ld SOIC
CD74HCT533E	-55 to 125	20 Ld PDIP
CD74HCT563E	-55 to 125	20 Ld PDIP
CD74HCT563M	-55 to 125	20 Ld SOIC

Pinouts

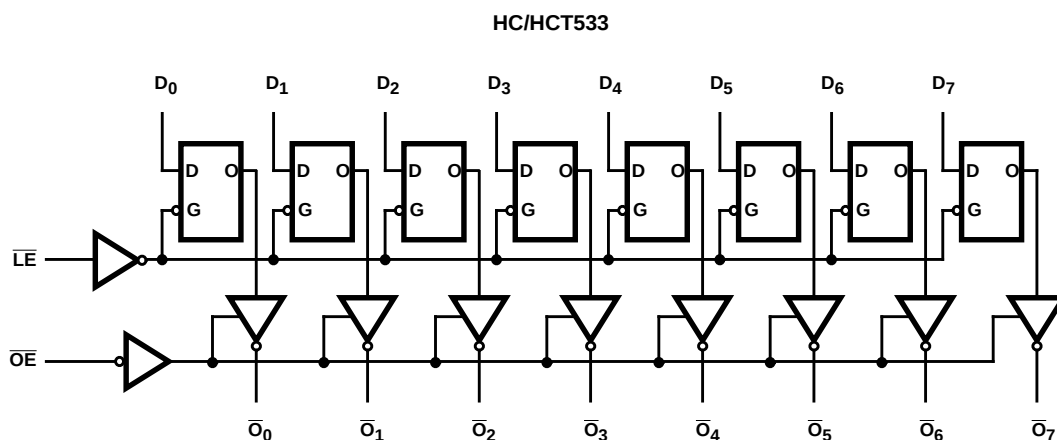
CD54HC533, CD54HCT533
(CERDIP)
CD74HC533, CD74HCT533
(PDIP)
TOP VIEW



CD54HC563
(CERDIP)
CD74HC563, CD74HCT563
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE

OUTPUT ENABLE	LATCH ENABLE	DATA	Q OUTPUT
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance State, l = Low voltage level one set-up time prior to the high to low latch enable transition, h = High voltage level one set-up time prior to the high to low latch enable transition.

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Drain Current, per Output, I_O
 For $-0.5V < V_O < V_{CC} + 0.5V$ $\pm 35mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} $\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^{\circ}C/W$)
 E (PDIP) Package 69
 M (SOIC) Package 58
 Maximum Junction Temperature $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$
 (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC}
 HC Types 2V to 6V
 HCT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 1000ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
HC TYPES														
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V		
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V		
			7.8	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA		
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	µA		

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Leakage Current	-	V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	-	±0.5	-	±5	-	±10	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Three-State Leakage Current	-	V _{IL} or V _{IH}	V _O = V _{CC} or GND	5.5	-	-	±0.5	-	±5	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
D0 - D7	0.15
$\overline{\text{LE}}$	0.30
$\overline{\text{OE}}$	0.55

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
$\overline{\text{LE}}$ Pulse Width	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Set-up Time Data to $\overline{\text{LE}}$	t_{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Hold Time, Data to $\overline{\text{LE}}$ (533)	t_H	-	2	35	-	-	45	-	55	-	ns
			4.5	7	-	-	9	-	11	-	ns
			6	6	-	-	8	-	7	-	ns
Hold Time, Data to $\overline{\overline{\text{LE}}}$ (563)	t_H	-	2	4	-	-	4	-	4	-	ns
			4.5	4	-	-	4	-	4	-	ns
			6	4	-	-	4	-	4	-	ns
HCT TYPES											
$\overline{\text{LE}}$ Pulse Width	t_W	-	4.5	16	-	-	20	-	24	-	ns
Set-up Time Data to $\overline{\text{LE}}$	t_W	-	4.5	10	-	-	13	-	15	-	ns
Hold Time, Data to $\overline{\text{LE}}$ (533)	t_H	-	4.5	8	-	-	10	-	12	-	ns
Hold Time, Data to $\overline{\text{LE}}$ (563)	t_H	-	4.5	5	-	-	5	-	5	-	ns

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Data to Qn (HC533)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
			6	-	28	35	43	ns
		C _L = 15pF	5	13	-	-	-	ns
Propagation Delay, Data to Qn (HC563)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C _L = 15pF	5	12	-	-	-	ns
Propagation Delay, LE to Qn (HC533)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
		C _L = 15pF	5	14	-	-	-	ns
Propagation Delay, LE to Qn (HC563)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
			6	-	28	35	43	ns
		C _L = 15pF	5	13	-	-	-	ns

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

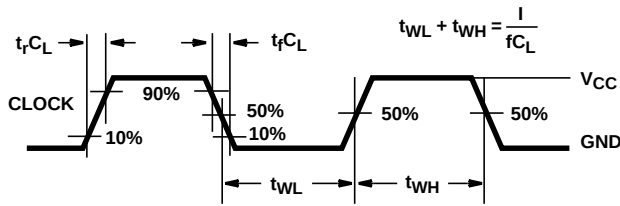
Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Enable Times (HC533)	t_{PZH}, t_{PZL}	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Disable Times (HC533)	t_{PHZ}, t_{PLZ}	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Enable and Disable Times (HC563)	$t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Output Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	42	-	-	-	pF
HCT TYPES								
Propagation Delay, Data to Qn (HC/HCT533)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	34	43	51	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Propagation Delay, Data to Qn (HC/HCT563)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Propagation Delay, LE to Qn (HC/HCT533)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	38	48	57	ns
		$C_L = 15\text{pF}$	5	16	-	-	-	ns
Propagation Delay, LE to Qn (HC/HCT563)	t_{PZL}, t_{PZH}	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Enable Times (HC/HCT533)	t_{PLZ}, t_{PZH}	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Disable Times (HC/HCT533)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Enable and Disable Times (HC/HCT563)	$t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	42	-	-	-	pF

NOTES:

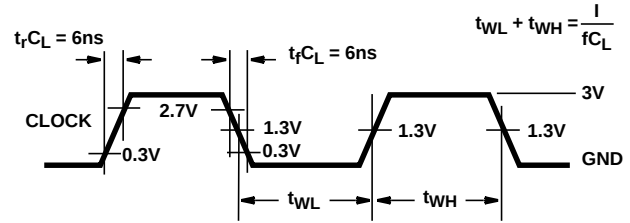
- C_{PD} is used to determine the no-load dynamic power consumption, per latch.
- P_D (total power per latch) = $C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

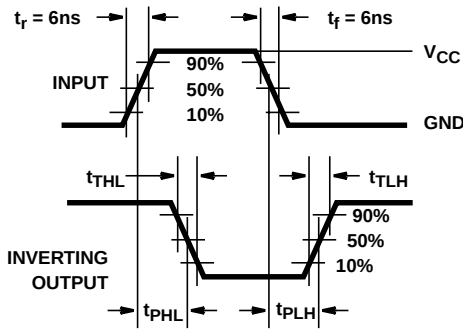


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

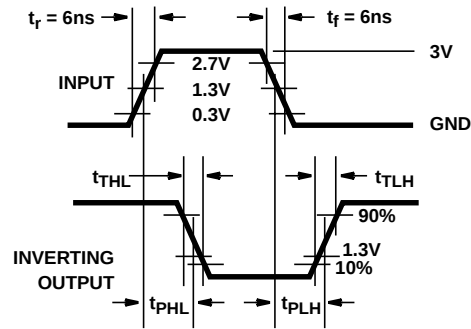


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

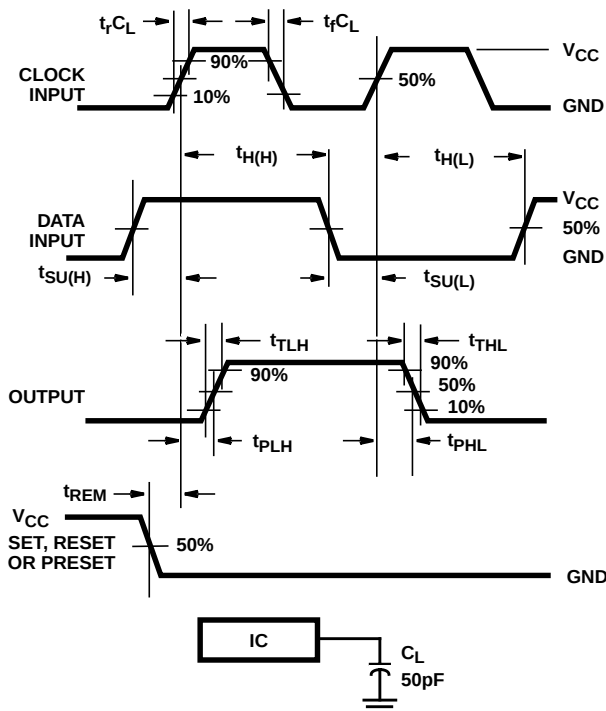


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

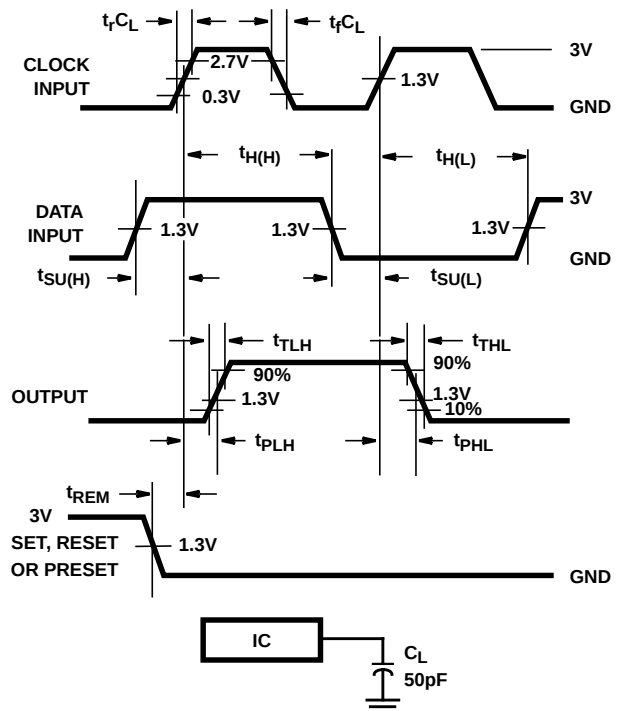


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

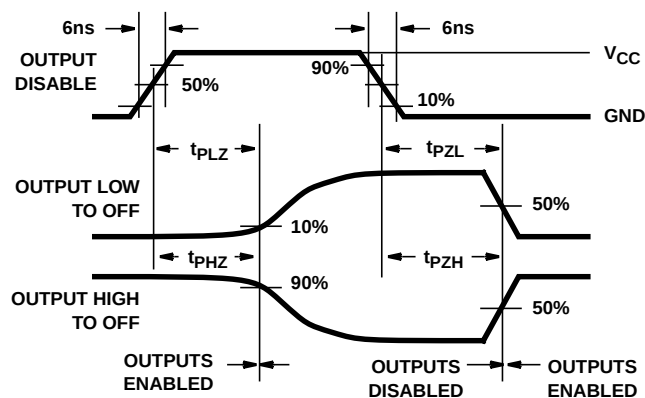


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

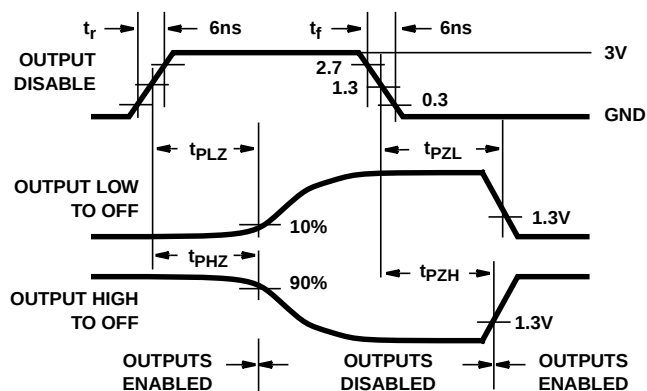
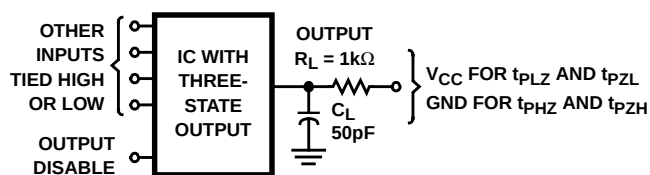


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



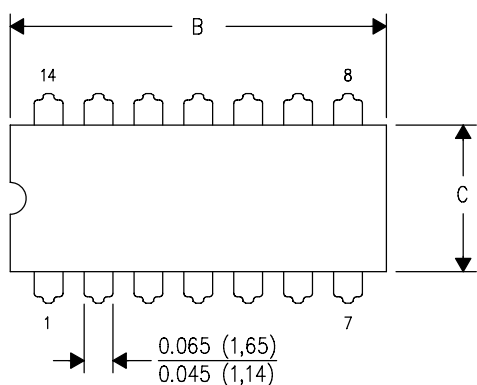
NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

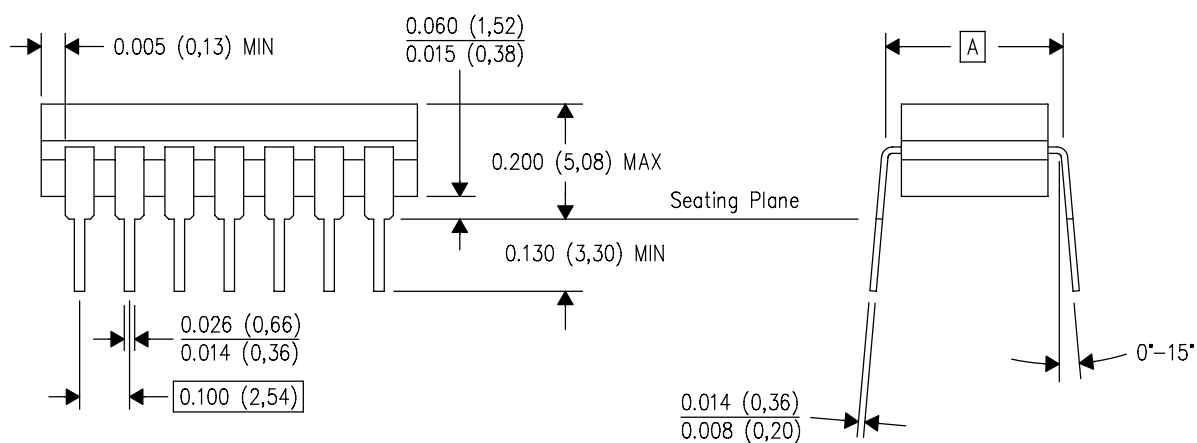
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



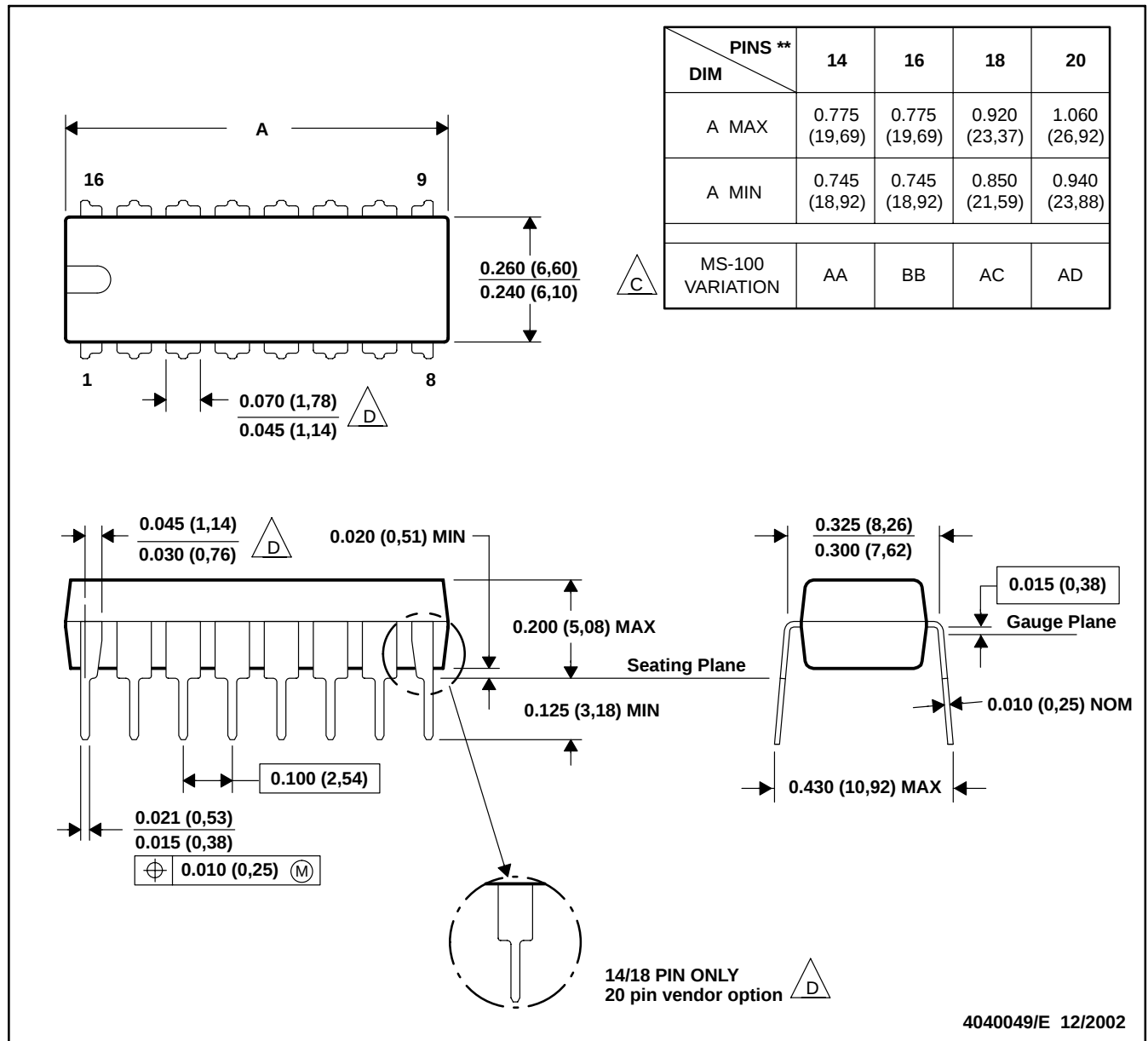
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

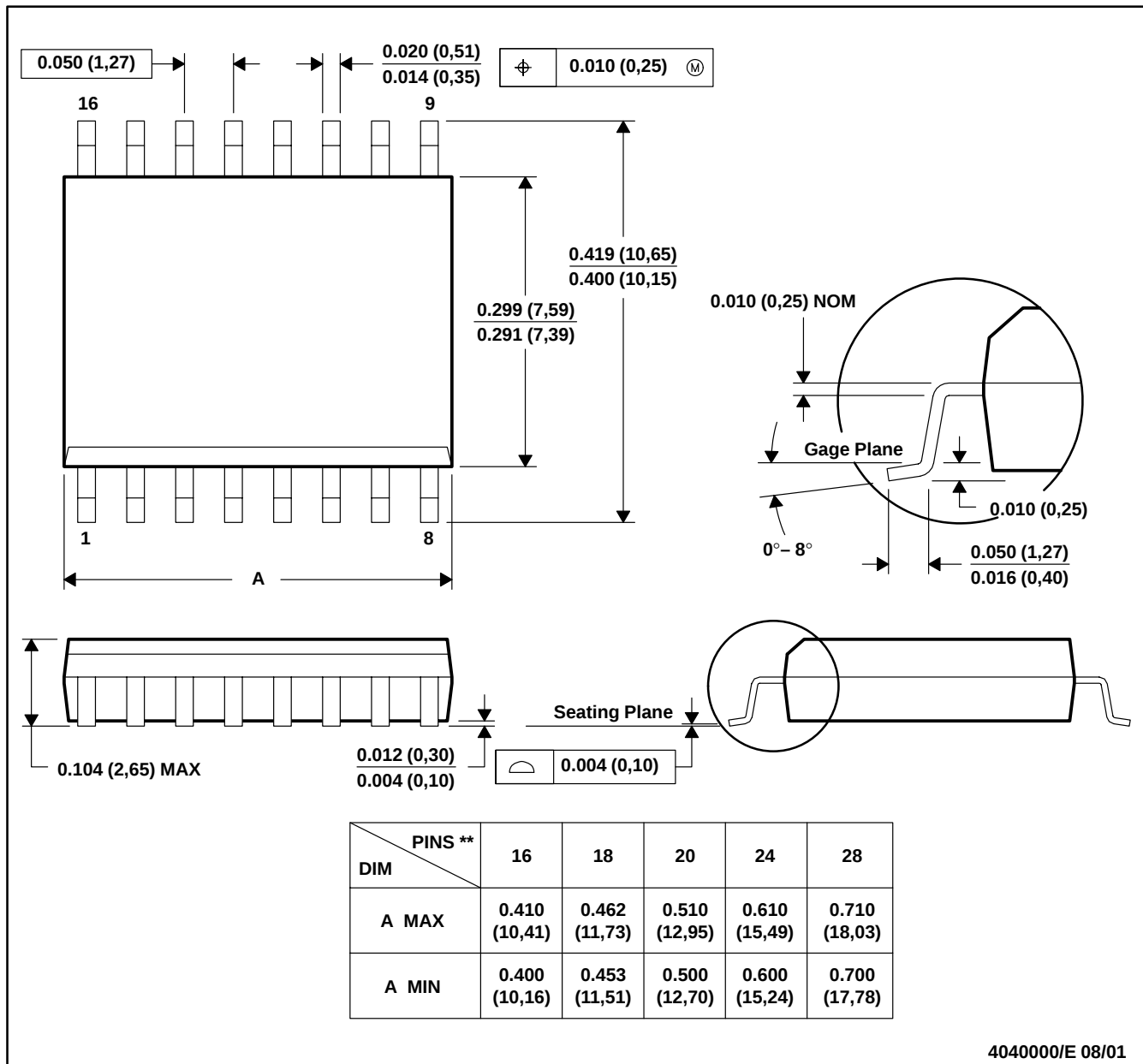
C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013