National Semiconductor

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LM26001
1.5A Switching Regulator with High Efficiency Sleep Mode

General Description

The LM26001 is a switching regulator designed for the high efficiency requirements of applications with stand-by modes. The device features a low-current sleep mode to maintain efficiency under light-load conditions and current-mode control for accurate regulation over a wide input voltage range. Quiescent current is reduced to 10 µA typically in shutdown mode and less than 40 µA in sleep mode. Forced PWM mode is also available to disable sleep mode.

The LM26001 can deliver up to 1.5A of continuous load current with a fixed current limit, through the internal N-channel switch. The part has a wide input voltage range of 4.0V to 38V and can operate with input voltages as low as 3V during line transients.

Operating frequency is adjustable from 150 kHz to 500 kHz with a single resistor and can be synchronized to an external clock.

Other features include Power good, adjustable soft-start, enable pin, input under-voltage protection, and an internal bootstrap diode for reduced component count.

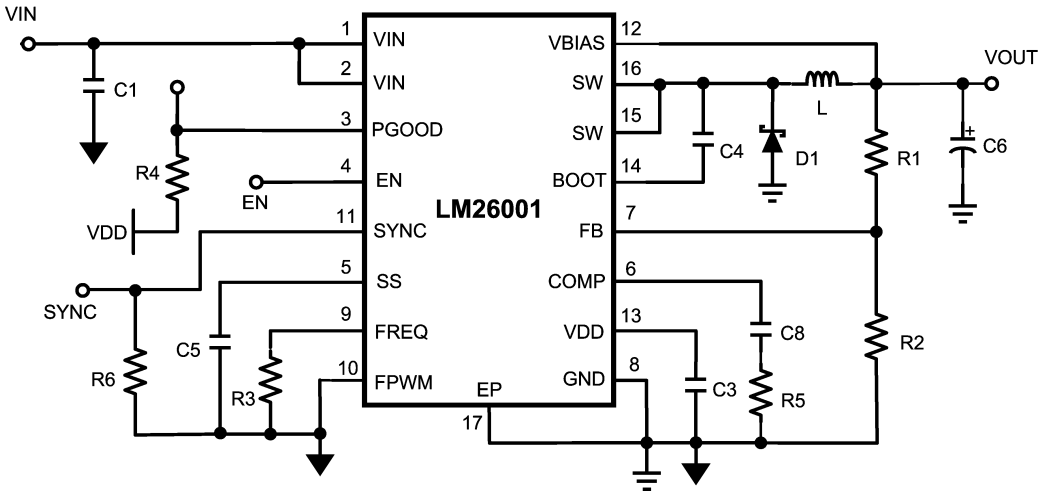
Features

- High efficiency sleep mode
- 40 µA typical Iq in sleep mode
- 10 µA typical Iq in shutdown mode
- 3.0V minimum input voltage
- 4.0V to 38V continuous input range
- 1.5% reference accuracy
- Cycle-by-cycle current limit
- Adjustable Frequency (150 kHz to 500 kHz)
- Synchronizable to an external clock
- Power Good Flag
- Forced PWM function
- Adjustable Soft-start
- TSSOP-16 exposed pad package
- Thermal Shut Down

Applications

- Automotive Telematics
- Navigation systems
- In-Dash Instrumentation
- Battery Powered Applications
- Stand-by power for home gateways/set-top boxes

Typical Application Circuit



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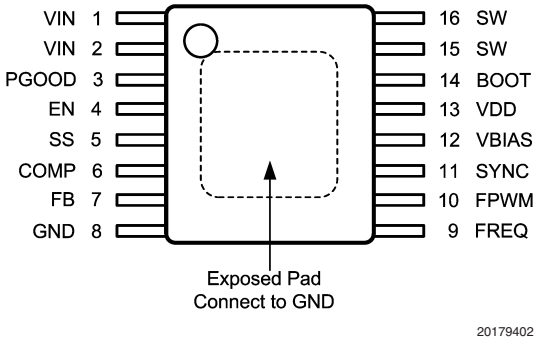
Connection Diagram



Top View
16-Lead Plastic TSSOP

Ordering Information

Order Number	Package Type	Package Drawing	Package Marking	Supplied As
LM26001MXA	TSSOP-16EXP	MXA16A	LM26001EM	92 Units of Rail
LM26001MXAX	TSSOP-16EXP	MXA16A	LM26001EM	2500 Units of Tape and Reel

Pin Descriptions

Pin #	Pin Name	Description
1	VIN	Power supply input
2	VIN	Power supply input
3	PGOOD	Power Good pin. An open drain output which goes high when the output voltage is greater than 92% of nominal.
4	EN	Enable is an analog level input pin. When pulled below 0.8V, the device enters shutdown mode.
5	SS	Soft-start pin. Connect a capacitor from this pin to GND to set the soft-start time.
6	COMP	Compensation pin. Connect to a resistor capacitor pair to compensate the control loop.
7	FB	Feedback pin. Connect to a resistor divider between Vout and GND to set output voltage.
8	GND	Ground
9	FREQ	Frequency adjust pin. Connect a resistor from this pin to GND to set the operating frequency.
10	FPWM	FPWM is a logic level input pin. For normal operation, connect to GND. When pulled high, sleep mode operation is disabled.
11	SYNC	Frequency synchronization pin. Connect to an external clock signal for synchronized operation. SYNC must be pulled low for non-synchronized operation.
12	VBIAS	Connect to an external 3V or greater supply to bypass the internal regulator for improved efficiency. If not used, VBIAS should be tied to GND.
13	VDD	The output of the internal regulator. Bypass with a minimum 1.0 µF capacitor.
14	BOOT	Bootstrap capacitor pin. Connect a 0.1µF minimum ceramic capacitor from this pin to SW to generate the gate drive bootstrap voltage.
15	SW	Switch pin. The source of the internal N-channel switch.
16	SW	Switch pin. The source of the internal N-channel switch.
EP	EP	Exposed Pad thermal connection. Connect to GND.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltages from the indicated pins to GND:	
VIN	-0.3V to 40V
SW (Note 7)	-0.5V to 40V
VDD	-0.3V to 7V
VBIAS	-0.3V to 10V
FB	-0.3V to 6V
BOOT	SW-0.3V to SW+7V
PGOOD	-0.3V to 7V
FREQ	-0.3V to 7V
SYNC	-0.3V to 7V
EN	-0.3V to 40V
FPWM	-0.3V to 7V
SS	-0.3V to 7V
Storage Temperature	-65˚C to +150˚C
Power Dissipation (Note 2)	2.6 W
Recommended Lead Temperature	
Vapor Phase (70s)	215˚C
Infrared (15s)	220˚C
ESD Susceptibility (Note 3)	
Machine Model	200V
Human Body Model	2KV
Charged Device Model	1kV

Operating Ratings (Note 1)

Operating Junction Temp.	–40˚C to 125˚C
Supply Voltage (Note 4)	3.0V to 38V

Electrical Characteristics

Specifications in standard type are for T_J = 25˚C only, and limits in boldface type apply over the junction temperature (T_J) range of -40˚C to +125˚C. Unless otherwise stated, Vin=12V. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25˚C, and are provided for reference purposes only. (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System						
I_{SD} (Note 6)	Shutdown Current	EN = 0V		9.5	**20**	µA
$Iq_{\_Sleep\_VB}$ (Note 6)	Quiescent Current	Sleep mode, VBIAS = 5V		38	**70**	µA
$Iq_{\_Sleep\_VDD}$	Quiescent Current	Sleep mode, VBIAS = GND		83	**150**	µA
$Iq_{\_PWM\_VB}$	Quiescent Current	PWM mode, VBIAS = 5V		150	230	µA
$Iq_{\_PWM\_VDD}$	Quiescent Current	PWM mode, VBIAS = GND		0.65	0.85	mA
I_{BIAS_Sleep} (Note 6)	Bias Current	Sleep mode, VBIAS = 5V		43	**105**	µA
I_{BIAS_PWM}	Bias Current	PWM mode, VBIAS = 5V		0.5	0.70	mA
V_{FB}	Feedback Voltage	5V < Vin < 38V	**1.2155**	1.234	**1.2525**	V
I_{FB}	FB Bias Current				±200	nA
$\Delta V_{OUT}/\Delta V_{IN}$	Vout line regulation	5V < Vin <38V		0.001		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Vout load regulation	0.8 < V_{COMP} < 1.15V		0.07		%
VDD	VDD output voltage	7 < Vin < 35V, I_{VDD}= 0 mA to 5 mA	**5.50**	5.95	**6.50**	V
I_{SS_Source}	Soft-start source current		**0.9**	2.3	**3.6**	µA
V_{bias_th}	VBIAS switchover threshold		**2.50**	2.7	**3.05**	V
Switching						
$R_{DS(ON)}$	Switch on Resistance	Isw = 1A	**0.12**	0.2	**0.42**	Ω
I_{sw_off}	Switch off state leakage current	Vin = 38V, VSW = 0V		0.002	**5.0**	µA
f_{sw}	Switching Frequency	RFREQ = 62k, 124k, 240k			**±10**	%
V_{FREQ}	FREQ voltage			1.0		V
f_{SW} range	Switching Frequency range		**150**		**500**	kHz
V_{SYNC}	Sync pin threshold	SYNC rising		1.2	**1.6**	V
		SYNC falling	**0.8**	1.1		
	Sync pin hysteresis			114		mV
I_{SYNC}	SYNC leakage current			6		nA
F_{SYNC_UP}	Upper frequency synchronization range	As compared to nominal f_{SW}			**+30**	%
F_{SYNC_DN}	Lower frequency synchronization range	As compared to nominal f_{SW}			**-20**	%

Electrical Characteristics Specifications in standard type are for T_J = 25˚C only, and limits in boldface type apply over the junction temperature (T_J) range of -40˚C to +125˚C. Unless otherwise stated, Vin=12V. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25˚C, and are provided for reference purposes only. (Note 5) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{OFFMIN}	Minimum Off-time			365		ns
T_{ONMIN}	Minimum On-time			155		ns
TH_{SLEEP_HYS}	Sleep mode threshold hysteresis	VFB rising, % of TH_{WAKE}		101.2		%
TH_{WAKE}	Wake up threshold	Measured at falling FB, COMP = 0.6V		1.234		V
I_{BOOT}	BOOT pin leakage current	BOOT = 16V, SW = 10V		0.0006	**5.0**	µA
Protection						
I_{LIMPK}	Peak Current Limit		**1.85**	2.5	**3.2**	A
V_{FB_SC}	Short circuit frequency foldback threshold	Measured at FB falling		0.87		V
F_min_sc	Min Frequency in foldback	VFB < 0.3V		71		kHz
V_{TH_PGOOD}	Power Good Threshold	Measured at FB, PGOOD rising	**89**	92	**95**	%
	PGOOD hysteresis		2	7	8	%
I_{PGOOD_HI}	PGOOD leakage current	PGOOD = 5V		0.2		nA
R_{DS_PGOOD}	PGOOD on resistance	PGOOD sink current = 500 µA		64		Ω
V_{UVLO}	Under-voltage Lock-Out Threshold	Vin falling , shutdown, VDD = VIN	**2.60**	2.9	**3.20**	V
		Vin rising, soft-start, VDD = VIN	**3.60**	3.9	**4.20**	
TSD	Thermal Shutdown Threshold			160		˚C
θ_{JA}	Thermal resistance	Power dissipation = 1W, 0 lfpm air flow		38		˚C/W
Logic						
Vth_{EN}	Enable Threshold voltage		**0.8**	1.1	**1.4**	V
	Enable hysteresis			164		mV
I_{EN_Source}	EN source current	EN = 0V		4.5		µA
V_{TH_FPWM}	FPWM threshold		**0.8**	1.2	**1.6**	V
I_{FPWM}	FPWM leakage current	FPWM = 5V		66		nA
EA						
gm	Error amp trans-conductance		**400**	670	**1000**	µmho
I_{COMP}	COMP source current	VCOMP = 0.9V		56		µA
	COMP sink current	VCOMP = 0.9V		39		µA
V_{COMP}	COMP pin voltage range		0.64		1.27	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\_MAX} = (T_{J\_MAX} - T_A) / \theta_{JA}$. The maximum power dissipation of 2.6W is determined using T_A = 25˚C, θ_{JA} = 38˚C/W, and T_{J_MAX} = 125˚C.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. The charged device model is per JESD22-C101-C.

Note 4: Below 4.0V input, power dissipation may increase due to increased $R_{DS(ON)}$. Therefore, a minimum input voltage of 4.0V is required to operate continuously within specification. A minimum of 3.9V (typical) is also required for startup.

Note 5: All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

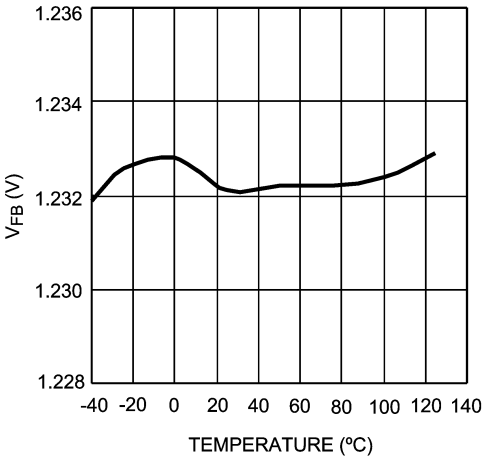
Note 6: Iq and ISD specify the current into the VIN pin. IBIAS is the current into the VBIAS pin when the VBIAS voltage is greater than 3V. All quiescent current specifications apply to non-switching operation.

Note 7: The absolute maximum specification applies to DC voltage. An extended negative voltage limit of -2V applies for a pulse of up to 1µs, and -1V for a pulse of up to 20µs.

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25˚C.

VFB vs Temperature



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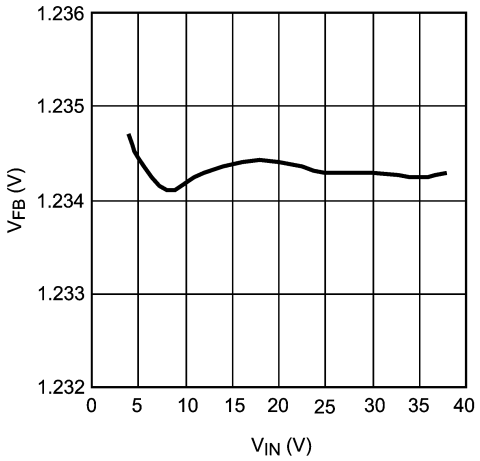
VFB vs Vin (IDC = 300 mA)



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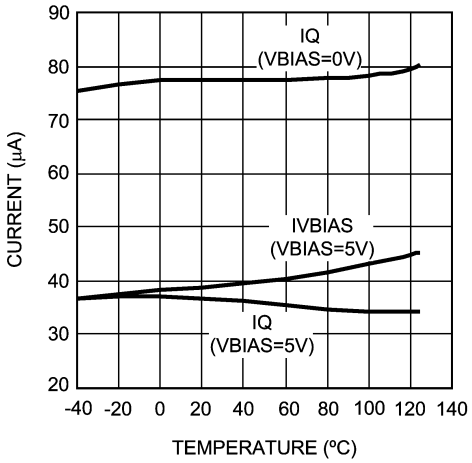
IQ and IVBIAS vs Temperature (Sleep Mode)



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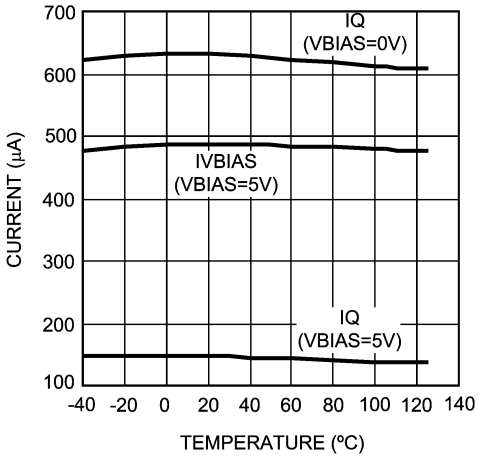
IQ and IVBIAS vs Temperature (PWM Mode)



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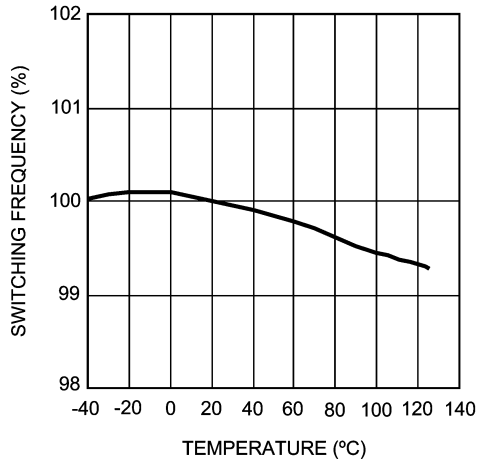
Normalized Switching Frequency vs Temperature (300kHz)



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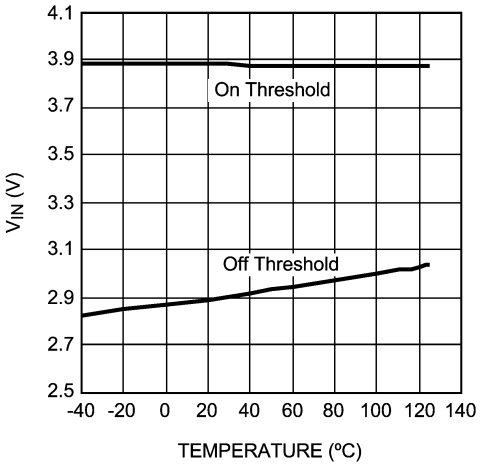
UVLO Threshold vs Temperature (VDD = VIN)



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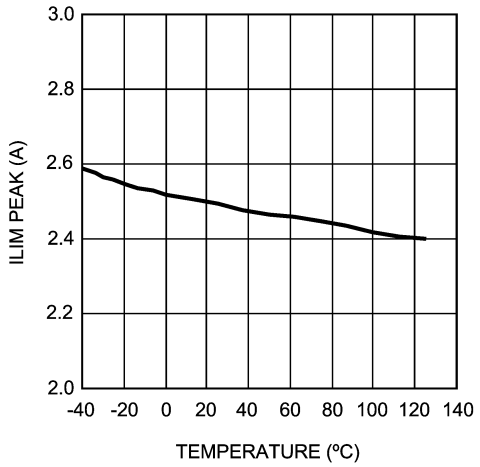
Typical Performance Characteristics Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25˚C. (Continued)

Peak Current Limit vs Temperature



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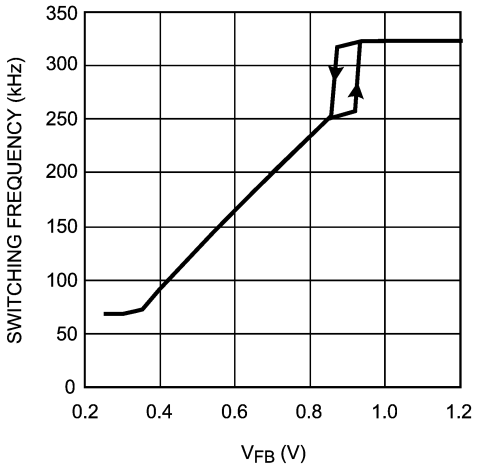
Short Circuit Foldback Frequency vs V_{FB} (325 kHz nominal)



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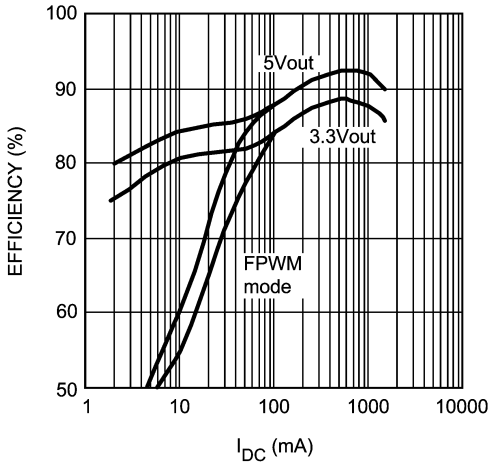
Efficiency vs Load Current (330kHz)



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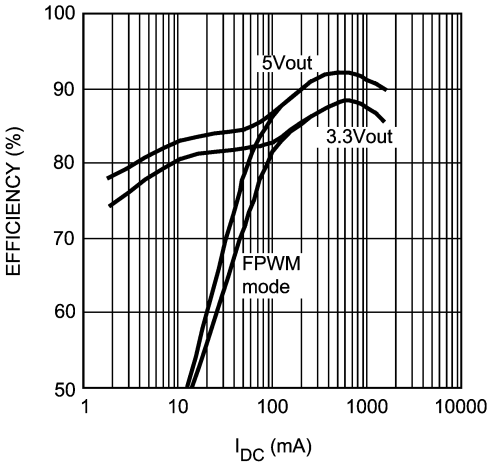
Efficiency vs Load Current (500kHz)



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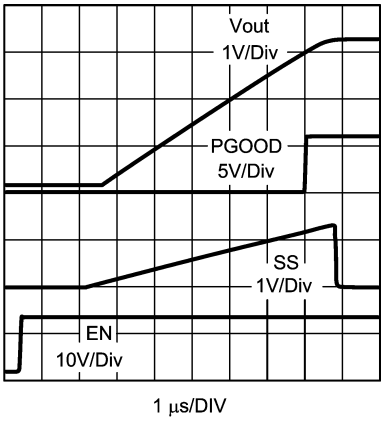
Startup Waveforms



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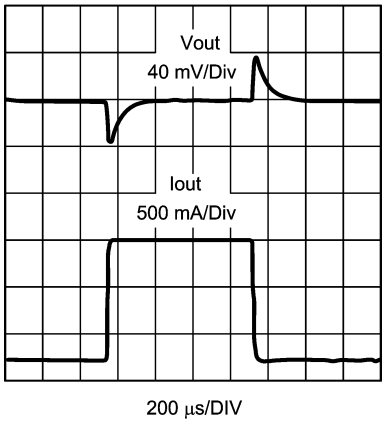
Load Transient Response



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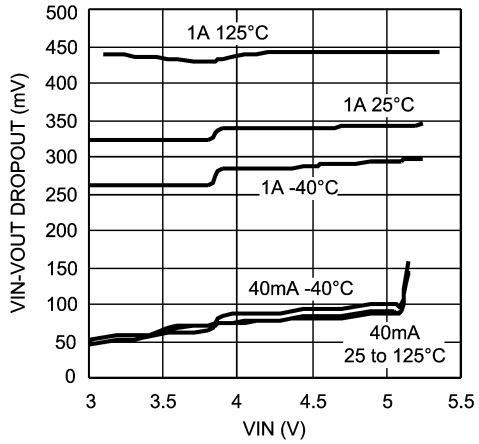
Typical Performance Characteristics Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25˚C. (Continued)

Low Input Voltage Dropout
Nominal VOUT = 5V



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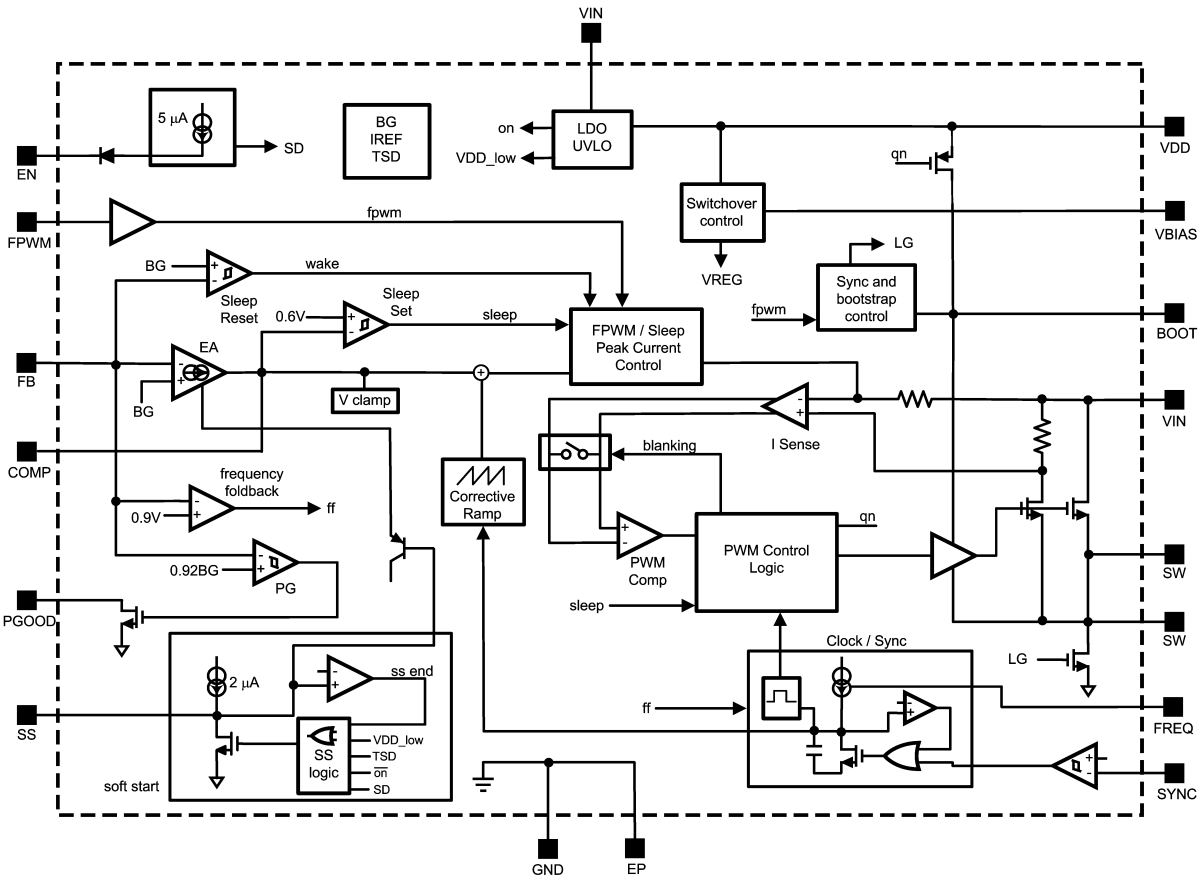
Block Diagram



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Operation Description

GENERAL

The LM26001 is a current mode PWM buck regulator. At the beginning of each clock cycle, the internal high-side switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. A control signal derived from the inductor current is compared to the voltage control signal at the COMP pin, derived from the feedback voltage. When the inductor current reaches the threshold, the high-side switch is turned off and inductor current ramps down. While the switch is off, inductor current is supplied through the catch diode. This cycle repeats at the next clock cycle. In this way, duty cycle and output voltage are controlled by regulating inductor current. Current mode control provides superior line and load regulation. Other benefits include cycle by cycle current limiting and a simplified compensation scheme. Typical PWM waveforms are shown in Figure 1.

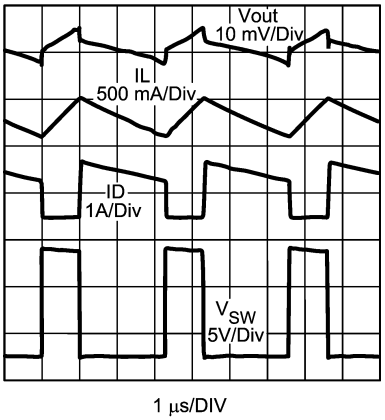

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FIGURE 1. PWM Waveforms
1A Load, Vin = 12V

SLEEP MODE

In light load conditions, the LM26001 automatically switches into sleep mode for improved efficiency. As loading decreases, the voltage at FB increases and the COMP voltage decreases. When the COMP voltage reaches the 0.6V (typical) clamp threshold, and the FB voltage rises 1% above nominal, sleep mode is enabled and switching stops. The regulator remains in sleep mode until the FB voltage falls to

Operation Description (Continued)

the reset threshold, at which point switching resumes. This 1% FB window limits the corresponding output ripple to approximately 1% of nominal output voltage. The sleep cycle will repeat until load current is increased. Figure 2 shows typical switching and output voltage waveforms in sleep mode.

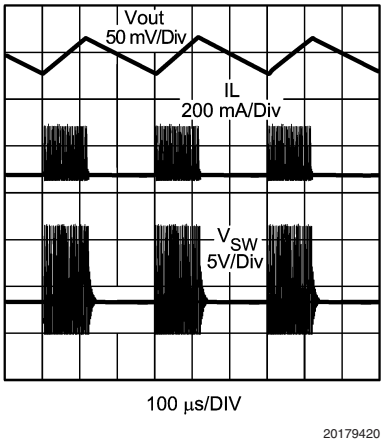


FIGURE 2. Sleep Mode Waveforms
25mA Load, Vin = 12V

In sleep mode, quiescent current is reduced to less than 40 µA when not switching. The DC sleep mode threshold can be calculated according to the equation below:

$$I_{Sleep} = \left[I_{min} + 0.13\,\mu \left[\frac{Vin - Vout}{L} \right] \right]^2 x \left[\frac{fsw \times L}{D \times 2 \times (Vin - Vout)} \right]$$

Where Imin=Ilim/16 (2.5A/16 typically) and D=duty cycle, defined as (Vout+Vdiode)/Vin.

When load current increases above this limit, the LM26001 is forced back into PWM operation. The sleep mode threshold varies with frequency, inductance, and duty cycle as shown in Figure 3.

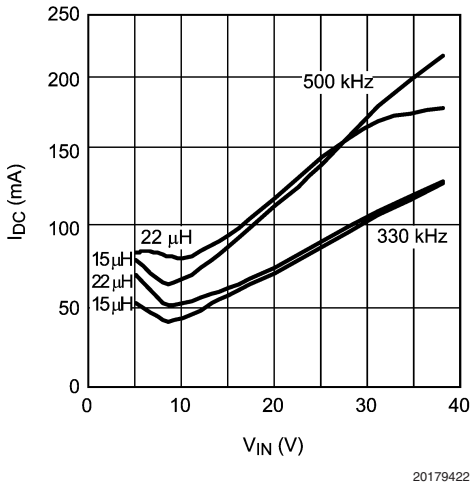


FIGURE 3. Sleep Mode Threshold vs Vin
Vout = 3.3V

FPWM

Pulling the FPWM pin high disables sleep mode and forces the LM26001 to always operate in PWM mode. Light load efficiency is reduced in PWM mode, but switching frequency remains stable. The FPWM pin can be connected to the VDD pin to pull it high. In FPWM mode, under light load conditions, the regulator operates in discontinuous conduction mode (DCM) . In discontinuous conduction mode, current through the inductor starts at zero and ramps up to its peak, then ramps down to zero again. Until the next cycle, the inductor current remains at zero. At nominal load currents, in FPWM mode, the device operates in continuous conduction mode, where positive current always flows in the inductor. Typical discontinuous operation waveforms are shown below.

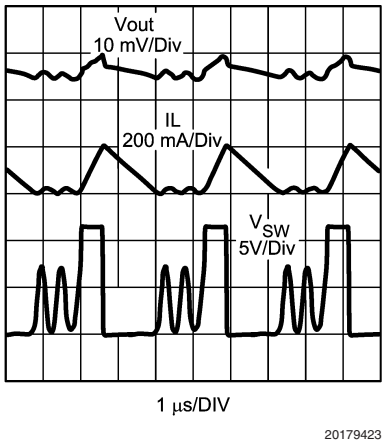


FIGURE 4. Discontinuous Mode Waveforms
75mA Load, Vin = 12V

At very light load, in FPWM mode, the LM26001 may enter sleep mode. This is to prevent an over-voltage condition from occurring. However, the FPWM sleep threshold is much lower than in normal operation.

ENABLE

The LM26001 provides a shutdown function via the EN pin to disable the device when the output voltage does not need to be maintained. EN is an analog level input with typically 164 mV of hysteresis. The device is active when the EN pin is above 1.1V (typical) and in shutdown mode when EN is below this threshold. When EN goes high, the internal VDD regulator turns on and charges the VDD capacitor. When VDD reaches 3.9V (typical), the soft-start pin begins to source current. In shutdown mode, the VDD regulator shuts down and total quiescent current is reduced to 10 µA (typical). Because the EN pin sources 4.5 µA (typical) of pull-up current, this pin can be left open for always-on operation. When open, EN will be pulled up to VIN.

If EN is connected to VIN, it must be connected through a 10 kΩ resistor to limit noise spikes. EN can also be driven externally with a maximum voltage of 38V or VIN + 15V, whichever is lower.

SOFT-START

The soft-start feature provides a controlled output voltage ramp up at startup. This reduces inrush current and eliminates output overshoot at turn-on. The soft-start pin, SS, must be connected to GND through a capacitor. At power-

Operation Description (Continued)

on, enable, or UVLO recovery, an internal 2.3 µA (typical) current charges the soft-start capacitor. During soft-start, the error amplifier output voltage is controlled by both the soft-start voltage and the feedback loop. As the SS pin voltage ramps up, the duty cycle increases proportional to the soft-start ramp, causing the output voltage to ramp up. The rate at which the duty cycle increases depends on the capacitance of the soft-start capacitor. The higher the capacitance, the slower the output voltage ramps up. The soft-start capacitor value can be calculated with the following equation:

$$Css = \frac{Iss \times tss}{1.234V}$$

Where tss is the desired soft-start time and Iss is the soft-start source current. During soft-start, current limit and synchronization remain in effect, while sleep mode and frequency foldback are disabled. Soft-start mode ends when the SS pin voltage reaches 1.23V typical. At this point, output voltage control is transferred to the FB pin and the SS pin is discharged.

CURRENT LIMIT

The peak current limit is set internally by directly measuring peak inductor current through the internal switch. To ensure accurate current sensing, VIN should be bypassed with a minimum 1µF ceramic capacitor placed directly at the pin.

When the inductor current reaches the current limit threshold, the internal FET turns off immediately allowing inductor current to ramp down until the next cycle. This reduction in duty cycle corresponds to a reduction in output voltage.

The current limit comparator is disabled for less than 100ns at the leading edge for increased immunity to switching noise.

Because the current limit monitors peak inductor current, the DC load current limit threshold varies with inductance and frequency. Assuming a minimum current limit of 1.85A, maximum load current can be calculated as follows:

$$Iload_{max} = 1.85A - \frac{Iripple}{2}$$

Where Iripple is the peak-to-peak inductor ripple current, calculated as shown below:

$$Iripple = \frac{(Vin - Vout) \times Vout}{fsw \times L \times Vin}$$

To find the worst case (lowest) current limit threshold, use the maximum input voltage and minimum current limit specification.

During high over-current conditions, such as output short circuit, the LM26001 employs frequency foldback as a second level of protection. If the feedback voltage falls below the short circuit threshold of 0.9V, operating frequency is reduced, thereby reducing average switch current. This is especially helpful in short circuit conditions, when inductor current can rise very high during the minimum on-time. Frequency reduction begins at 20% below the nominal frequency setting. The minimum operating frequency in foldback mode is 71 kHz typical.

If the FB voltage falls below the frequency foldback threshold during frequency synchronized operation, the SYNC function is disabled. Operating frequency versus FB voltage in short circuit conditions is shown in the typical performance characteristics section.

In conditions where the on time is close to minimum (less than 200nsec typically), such as high input voltage and high switching frequency, the current limit may not function properly. This is because the current limit circuit cannot reduce the on-time below minimum which prevents entry into frequency foldback mode. There are two ways to ensure proper current limit and foldback operation under high input voltage conditions. First, the operating frequency can be reduced to increase the nominal on time. Second, the inductor value can be increased to slow the current ramp and reduce the peak over-current.

FREQUENCY ADJUSTMENT AND SYNCHRONIZATION

The switching frequency of the LM26001 can be adjusted between 150 kHz and 500 kHz using a single external resistor. This resistor is connected from the FREQ pin to ground as shown in the typical application. The resistor value can be calculated with the following empirically derived equation:

$$R_{FREQ} = (6.25 \times 10^{10}) \times f_{SW}^{-1.042}$$

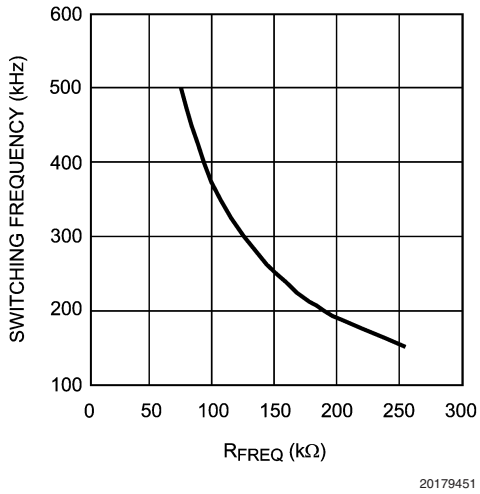


FIGURE 5. Swtiching Frequency vs R_{FREQ}

The switching frequency can also be synchronized to an external clock signal using the SYNC pin. The SYNC pin allows the operating frequency to be varied above and below the nominal frequency setting. The adjustment range is from 30% above nominal to 20% below nominal. External synchronization requires a 1.2V (typical) peak signal level at the SYNC pin. The FREQ resistor must always be connected to initialize the nominal operating frequency. The operating frequency is synchronized to the falling edge of the SYNC input. When SYNC goes low, the high-side switch turns on. This allows any duty cycle to be used for the sync signal when synchronizing to a frequency higher than nominal. When synchronizing to a lower frequency, however, there is a minimum duty cycle requirement for the SYNC signal, given in the equation below:

Operation Description (Continued)

$$\text{Sync\_Dmin} \geq 1 - \frac{f_{sync}}{fnom}$$

Where fnom is the nominal switching frequency set by the FREQ resistor, and fsync is a square wave. If the SYNC pin is not used, it must be pulled low for normal operation. A 10kΩ pull-down resistor is recommended to protect against a missing sync signal. Although the LM26001 is designed to operate at up to 500 kHz, maximum load current may be limited at higher frequencies due to increased temperature rise. See the Thermal Considerations section.

VBIAS

The VBIAS pin is used to bypass the internal regulator which provides the bias voltage to the LM26001. When the VBIAS pin is connected to a voltage greater than 3V, the internal regulator automatically switches over to the VBIAS input. This reduces the current into VIN (Iq) and increases system efficiency. Using the VBIAS pin has the added benefit of reducing power dissipation within the device.

For most applications where 3V < Vout < 10V, VBIAS can be connected to Vout. If not used, VBIAS should be tied to GND.

If VBIAS drops below 2.7V (typical), the device automatically switches over to supply the internal bias voltage from Vin.

Total device input current is the sum of Iq, gate drive current, and VBIAS current, plus some negligible current into the FB pin. Total minimum input supply current can be calculated as shown below:

$$Iinput = Iq + I_{QG} + \left(\frac{I_{BIAS} \times D}{eff}\right)$$

Where I_{QG} is the gate drive current, calculated as:

$$I_{QG} = (4.6 \times 10^{-9}) \times f_{SW}$$

Total supply input current varies according to load, system efficiency, and operating frequency. To calculate minimum input current during sleep mode, use $Iq_{\_Sleep\_VB}$, and I_{BIAS_SLEEP}.

For input current in PWM mode, use the same equation, with $Iq_{\_PWM\_VB}$, and I_{BIAS_PWM}.

If VBIAS is connected to ground, use the same equation with the Ibias term eliminated and either $I_{q\_Sleep\_VDD}$ or $Iq_{\_PWM\_VDD}$.

LOW VIN OPERATION AND UVLO

The LM26001 is designed to remain operational during short line transients when input voltage may drop as low as 3.0V. Minimum nominal operating input voltage is 4.0V. Below this voltage, switch $R_{DS(ON)}$ increases, due to the lower gate drive voltage from VDD. The minimum voltage required at VDD is approximately 3.5V for normal operation within specification.

VDD can also be used as a pull-up voltage for functions such as PGOOD and FPWM. Note that if VDD is used externally, the pin is not recommended for loads greater than 1 mA.

If the input voltage approaches the nominal output voltage, the duty cycle is maximized to hold up the output voltage. In this mode of operation, once the duty cycle reaches its maximum, the LM26001 can skip a maximum of seven off pulses, effectively increasing the duty cycle and thus minimizing the dropout from input to output. Typical off-pulse skipping waveforms are shown below.

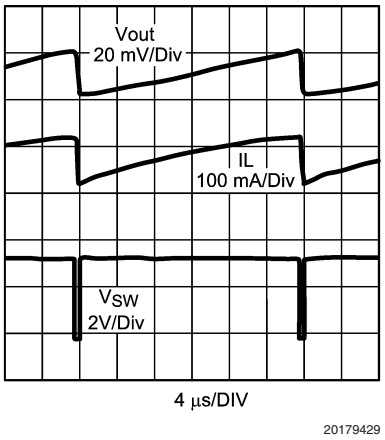


FIGURE 6. Off-pulse Skipping Waveforms
Vin = 3.5V, Vnom = 3.3V, fnom = 305kHz

UVLO is sensed at both VIN and VDD, and is activated when either voltage falls below 2.9V (typical). Although VDD is typically less than 200mV below VIN, it will not discharge through VIN. Therefore when the VIN voltage drops rapidly, VDD may remain high, especially in sleep mode. For fast line voltage transients, using a larger capacitor at the VDD pin can help to hold off a UVLO shutdown by extending the VDD discharge time. By holding up VDD, a larger cap can also reduce the $R_{DS(ON)}$ (and dropout voltage) in low VIN conditions. Alternately, under heavy loading the VDD voltage can fall several hundred mV below VIN. In this case, UVLO may be triggered by VDD even though the VIN voltage is above the UVLO threshold.

When UVLO is activated the LM26001 enters a standby state in which VDD remains charged. As input voltage and VDD voltage rise above 3.9V (typical) the device will restart from softstart mode.

PGOOD

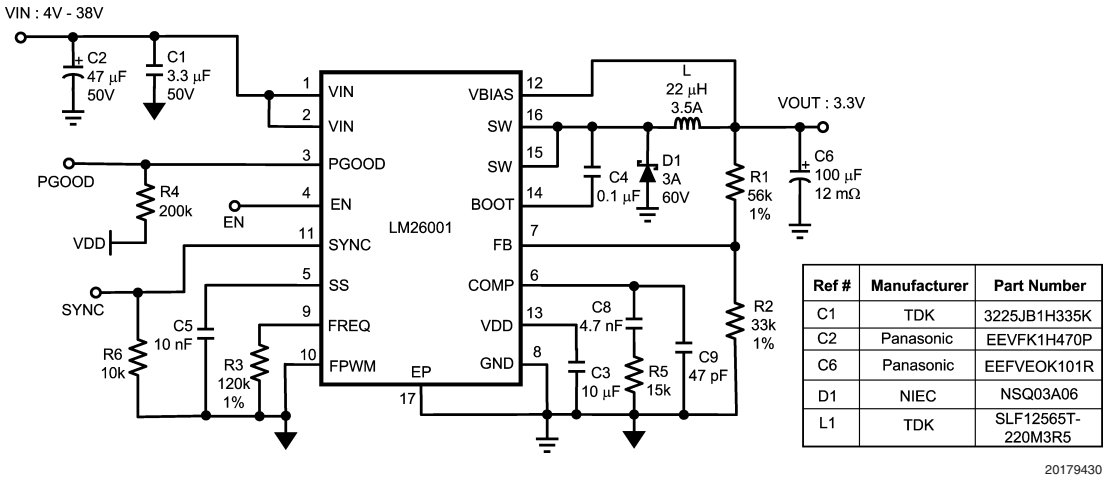
A power good pin, PGOOD, is available to monitor the output voltage status. The pin is internally connected to an open drain MOSFET, which remains open while the output voltage is within operating range. PGOOD goes low (low impedance to ground) when the output falls below 85% of nominal or EN is pulled low. When the output voltage returns to within 92% of nominal, as measured at the FB pin, PGOOD returns to a high state. For improved noise immunity, there is a 5us delay between the PGOOD threshold and the PGOOD pin going low.

Design Information

EXAMPLE CIRCUIT

Figure 7 shows a complete typical application schematic. The components have been selected based on the design criteria given in the following sections.

Design Information (Continued)



Ref #	Manufacturer	Part Number
C1	TDK	3225JB1H335K
C2	Panasonic	EEVFK1H470P
C6	Panasonic	EEFVEOK101R
D1	NIEC	NSQ03A06
L1	TDK	SLF12565T-220M3R5

FIGURE 7. Example Circuit
1.5A Max, 305 kHz

SETTING OUTPUT VOLTAGE

The output voltage is set by the ratio of a voltage divider at the FB pin as shown in the typical application. The resistor values can be determined by the following equation:

$$R2 = \frac{R1}{\left(\frac{Vout}{Vfb} - 1\right)}$$

Where Vfb = 1.234V typically.

A maximum value of 150kΩ is recommended for the sum of R1 and R2.

As input voltage decreases towards the nominal output voltage, the LM26001 can skip up to seven off-pulses as described in the Low Vin Operation section. In low output voltage applications, if the on-time reaches Ton_{MIN}, the device will skip on-pulses to maintain regulation. There is no limit to the number of pulses that are skipped. In this mode of operation, however, output ripple voltage may increase slightly.

INDUCTOR

The output inductor should be selected based on inductor ripple current. The amount of inductor ripple current compared to load current, or ripple content, is defined as Iripple/Iload. Ripple content should be less than 40%. Inductor ripple current, Iripple, can be calculated as shown below:

$$Iripple = \frac{(Vin - Vout) \times Vout}{fsw \times L \times Vin}$$

Larger ripple content increases losses in the inductor and reduces the effective current limit.

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold.

Remember that inductor value also affects the sleep mode threshold as shown in Figure 3.

When choosing the inductor, the saturation current rating must be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current. Peak inductor current, Ipeak, is calculated as:

$$Ipeak = Iload + \frac{Iripple}{2}$$

For example, at a maximum load of 1.5A and a ripple content of 40%, peak inductor current is equal to 1.8A which is safely below the minimum current limit of 1.85A. By increasing the inductor size, ripple content and peak inductor current are lowered, which increases the current limit margin.

The size of the output inductor can also be determined using the desired output ripple voltage, Vrip. The equation to determine the minimum inductance value based on Vrip is as follows:

$$L_{MIN} = \frac{(Vin - Vout) \times Vout \times Re}{Vin \times fsw \times Vrip}$$

Where Re is the ESR of the output capacitors, and Vrip is a peak-to-peak value. This equation assumes that the output capacitors have some amount of ESR. It does not apply to ceramic output capacitors.

If this method is used, ripple content should still be verified to be less than 40%.

OUTPUT CAPACITOR

The primary criterion for selecting an output capacitor is equivalent series resistance, or ESR.

ESR (Re) can be selected based on the requirements for output ripple voltage and transient response. Once an inductor value has been selected, ripple voltage can be calculated for a given Re using the equation above for Lmin. Lower ESR values result in lower output ripple.

Design Information (Continued)

Re can also be calculated from the following equation:

$$Re_{MAX} = \frac{\Delta Vt}{\Delta It}$$

Where ΔVt is the allowed voltage excursion during a load transient, and ΔIt is the maximum expected load transient.

If the total ESR is too high, the load transient requirement cannot be met, no matter how large the output capacitance.

If the ESR criteria for ripple voltage and transient excursion cannot be met, more capacitors should be used in parallel.

For non-ceramic capacitors, the minimum output capacitance is of secondary importance, and is determined only by the load transient requirement.

If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The minimum capacitance is calculated as follows:

$$C_{MIN} = \frac{L \times \left(\Delta Vt - \sqrt{(\Delta Vt)^2 - (\Delta It \times R_e)^2}\right)}{V_{out} \times R_e^2}$$

It is assumed the total ESR, Re, is no greater than Re_{MAX}. Also, it is assumed that L has already been selected.

Generally speaking, the output capacitance requirement decreases with Re, ΔIt, and L. A typical value greater than 100 µF works well for most applications.

INPUT CAPACITOR

In a switching converter, very fast switching pulse currents are drawn from the input rail. Therefore, input capacitors are required to reduce noise, EMI, and ripple at the input to the LM26001. Capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. The equation for calculating the RMS input ripple current is shown below:

$$Irms = \frac{Iload \times \sqrt{Vout \times (Vin - Vout)}}{Vin}$$

For noise suppression, a ceramic capacitor in the range of 1.0 µF to 10 µF should be placed as close as possible to the VIN pin.

A larger, high ESR input capacitor should also be used. This capacitor is recommended for damping input voltage spikes during power on and for holding up the input voltage during transients. In low input voltage applications, line transients may fall below the UVLO threshold if there is not enough input capacitance. Both tantalum and electrolytic type capacitors are suitable for the bulk capacitor. However, large tantalums may not be available for high input voltages and their working voltage must be derated by at least 2X.

BOOTSTRAP

The drive voltage for the internal switch is supplied via the BOOT pin. This pin must be connected to a ceramic capacitor, Cboot, from the switch node, shown as C4 in the typical application. The LM26001 provides the VDD voltage internally, so no external diode is needed. A minimum value of 0.1 uF is recommended for Cboot. Smaller values may result in insufficient hold up time for the drive voltage and increased power dissipation.

During low Vin operation, when the on-time is extended, the bootstrap capacitor is at risk of discharging. If the Cboot capacitor is discharged below approximately 2.5V, the LM26001 enters a high frequency re-charge mode. The Cboot cap is re-charged via the LG synchronous FET shown in the block diagram. Switching returns to normal when the Cboot cap has been recharged.

CATCH DIODE

When the internal switch is off, output current flows through the catch diode. Alternately, when the switch is on, the diode sees a reverse voltage equal to Vin. Therefore, the important parameters for selecting the catch diode are peak current and peak inverse voltage. The average current through the diode is given by:

$$ID_{AVE} = Iload \times (1-D)$$

Where D is the duty cycle, defined as Vout/Vin. The catch diode conducts the largest currents during the lowest duty cycle. Therefore ID_{AVE} should be calculated assuming maximum input voltage. The diode should be rated to handle this current continuously. For over-current or short circuit conditions, the catch diode should be rated to handle peak currents equal to the peak current limit.

The peak inverse voltage rating of the diode must be greater than maximum input voltage.

A Schottky diode must be used. It's low forward voltage maximizes efficiency and BOOT voltage, while also protecting the SW pin against large negative voltage spikes

COMPENSATION

The purpose of loop compensation is to ensure stable operation while maximizing dynamic performance. Stability can be analyzed with loop gain measurements, while dynamic performance is analyzed with both loop gain and load transient response. Loop gain is equal to the product of control-output transfer function (power stage) and the feedback transfer function (the compensation network).

For stability purposes, our target is to have a loop gain slope that is -20dB /decade from a very low frequency to beyond the crossover frequency. Also, the crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60 kHz in the case of 300 kHz switching frequency.

For dynamic purposes, the higher the bandwidth, the faster the load transient response. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). To achieve this loop gain, the compensation components should be set according to the shape of the control-output bode plot. A typical plot is shown in Figure 8 below.

Design Information (Continued)

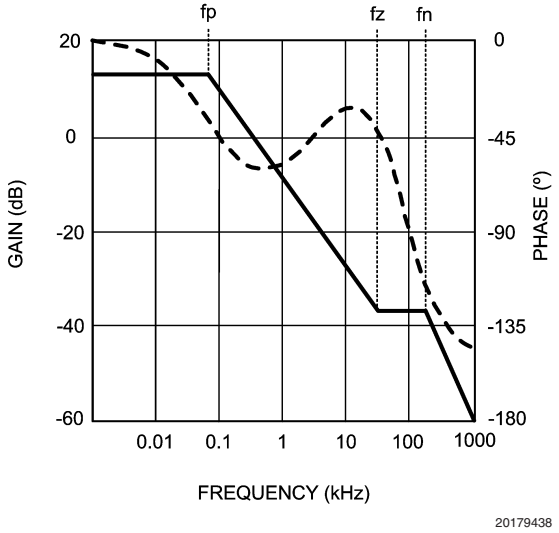


FIGURE 8. Control-Output Transfer Function

The control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency).

Referring to Figure 8, the following should be done to create a -20dB /decade roll-off of the loop gain:

1. Place a pole at 0Hz (fpc)
2. Place a zero at fp (fzc)
3. Place a second pole at fz (fpc1)

The resulting feedback (compensation) bode plot is shown below in Figure 9. Adding the control-output response to the feedback response will then result in a nearly continuous -20db/decade slope.

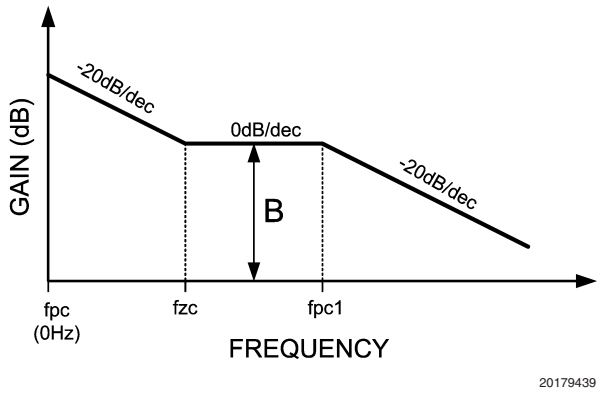


FIGURE 9. Feedback Transfer Function

The control-output corner frequencies can be determined approximately by the following equations:

$$fz = \frac{1}{2\pi \times Re \times Co}$$

$$fp = \frac{1}{10 \times \pi \times Ro \times Co} + \frac{0.5}{2 \times \pi \times L \times fsw \times Co}$$

$$fn = \frac{fsw}{2}$$

Where Co is the output capacitance, Ro is the load resistance, Re is the output capacitor ESR, and fsw is the switching frequency. The effects of slope compensation and current sense gain are included in this equation. However, the equation is an approximation intended to simplify loop compensation calculations. To derive the exact transfer function, use 0.2V/V sense amp gain and 36mVp-p slope compensation.

Since fp is determined by the output network, it shifts with loading. Determine the range of frequencies (fpmin/max) across the expected load range. Then determine the compensation values as described below and shown in Figure 10.

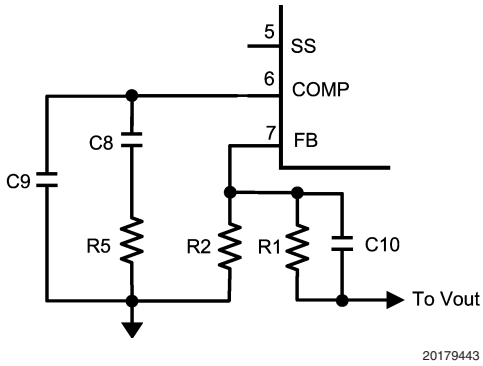


FIGURE 10. Compensation Network

1. The compensation network automatically introduces a low frequency pole (fpc), which is close to 0Hz.

2. Once the fp range is determined, R5 should be calculated using:

$$R5 = \frac{B}{gm} \times \left(\frac{R1 + R2}{R2}\right)$$

Where B is the desired feedback gain in v/v between fp and fz, and gm is the transconductance of the error amplifier. A gain value around 10dB (3.3v/v) is generally a good starting point. Bandwidth increases with increasing values of R5.

3. Next, place a zero (fzc) near fp using C8. C8 can be determined with the following equation:

$$C8 = \frac{1}{2 \times \pi \times fP_{MAX} \times R5}$$

The selected value of C8 should place fzc within a decade above or below fpmax, and not less than fpmin. A higher C8 value (closer to fpmin) generally provides a more stable loop, but too high a value will slow the transient response time. Conversely, a smaller C8 value will result in a faster transient response, but lower phase margin.

Design Information (Continued)

4. A second pole (fpc1) can also be placed at fz. This pole can be created with a single capacitor, C9. The minimum value for this capacitor can be calculated by:

$$C9 = \frac{1}{2 \times \pi \times fz \times R5}$$

C9 may not be necessary in all applications. However if the operating frequency is being synchronized below the nominal frequency, C9 is recommended. Although it is not required for stability, C9 is very helpful in suppressing noise.

A phase lead capacitor can also be added to increase the phase and gain margins. The phase lead capacitor is most helpful for high input voltage applications or when synchronizing to a frequency greater than nominal. This capacitor, shown as C10 in Figure 10, should be placed in parallel with the top feedback resistor, R1. C10 introduces an additional zero and pole to the compensation network. These frequencies can be calculated as shown below:

$$fzff = \frac{1}{2 \times \pi \times R1 \times C10}$$

$$fpff = \frac{fzff \times Vout}{Vfb}$$

A phase lead capacitor will boost loop phase around the region of the zero frequency, fzff. fzff should placed somewhat below the fpz1 frequency set by C9. However, if C10 is too large, it will have no effect.

PCB Layout

Good board layout is critical for switching regulators such as the LM26001. First, the ground plane area must be sufficient for thermal dissipation purposes, and second, appropriate guidelines must be followed to reduce the effects of switching noise.

Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with parasitic trace inductance generates unwanted Ldi/dt noise spikes at the SW node and also at the VIN node. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. Although the LM26001 has 100ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time. Following the important guidelines below will help minimize switching noise and its effect on current sensing.

The switch node area should be as small as possible. The catch diode, input capacitors, and output capacitors should be grounded to a large ground plane, with the bulk input capacitor grounded as close as possible to the catch diode anode. Additionally, the ground area between the catch diode and bulk input capacitor is very noisy and should be somewhat isolated from the rest of the ground plane.

A ceramic input capacitor must be connected as close as possible to the VIN pin and grounded close to the GND pin. Often this capacitor is most easily located on the bottom side of the pcb. If placement close to the GND pin is not practical, the ceramic input capacitor can also be grounded close to the catch diode ground. The above layout recommendations are illustrated below in Figure 11.

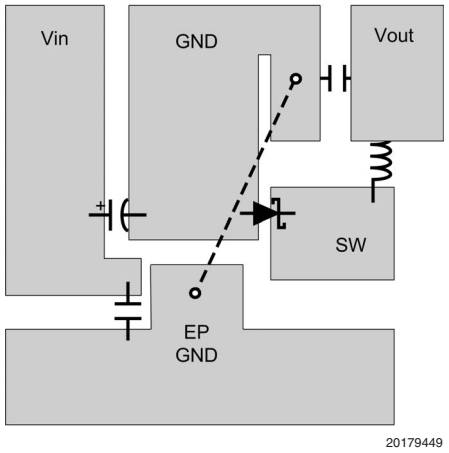


FIGURE 11. Example PCB Layout

It is a good practice to connect the EP, GND pin, and small signal components (COMP, FB, FREQ) to a separate ground plane, shown in Figure 11 as EP GND, and in the schematics as a signal ground symbol. Both the exposed pad and the GND pin must be connected to ground. This quieter plane should be connected to the high current ground plane at a quiet location, preferably near the Vout ground as shown by the dashed line in Figure 11.

The EP GND plane should be made as large as possible, since it is also used for thermal dissipation. Several vias can be placed directly below the EP to increase heat flow to other layers when they are available. The recommended via hole diameter is 0.3mm.

The trace from the FB pin to the resistor divider should be short and the entire feedback trace must be kept away from the inductor and switch node. See Application Note AN-1229 for more information regarding PCB layout for switching regulators.

Thermal Considerations and TSD

Although the LM26001 has a built in current limit, at ambient temperatures above 80˚C, device temperature rise may limit the actual maximum load current. Therefore, temperature rise must be taken into consideration to determine the maximum allowable load current.

Temperature rise is a function of the power dissipation within the device. The following equations can be used to calculate power dissipation (PD) and temperature rise, where total PD is the sum of FET switching losses, FET DC losses, drive losses, Iq, and VBIAS losses:

$$PD_{TOTAL} = Psw_{AC} + Psw_{DC} + PQG + P_{Iq} + P_{VBIAS}$$

Thermal Considerations and TSD

(Continued)

$$Psw_{AC} = Vin \times Iload \times fsw \times \left(\frac{Vin \times 10^{-9}}{1.33}\right)$$

$$Psw_{DC} = D \times Iload^2 \times (0.2 + 0.00065 \times (T_j - 25))$$

$$P_{QG} = Vin \times 4.6 \times 10^{-9} \times fsw$$

$$P_{Iq} = Vin \times Iq$$

$$P_{VBIAS} = Vbias \times I_{VBIAS}$$

Given this total power dissipation, junction temperature can be calculated as follows:

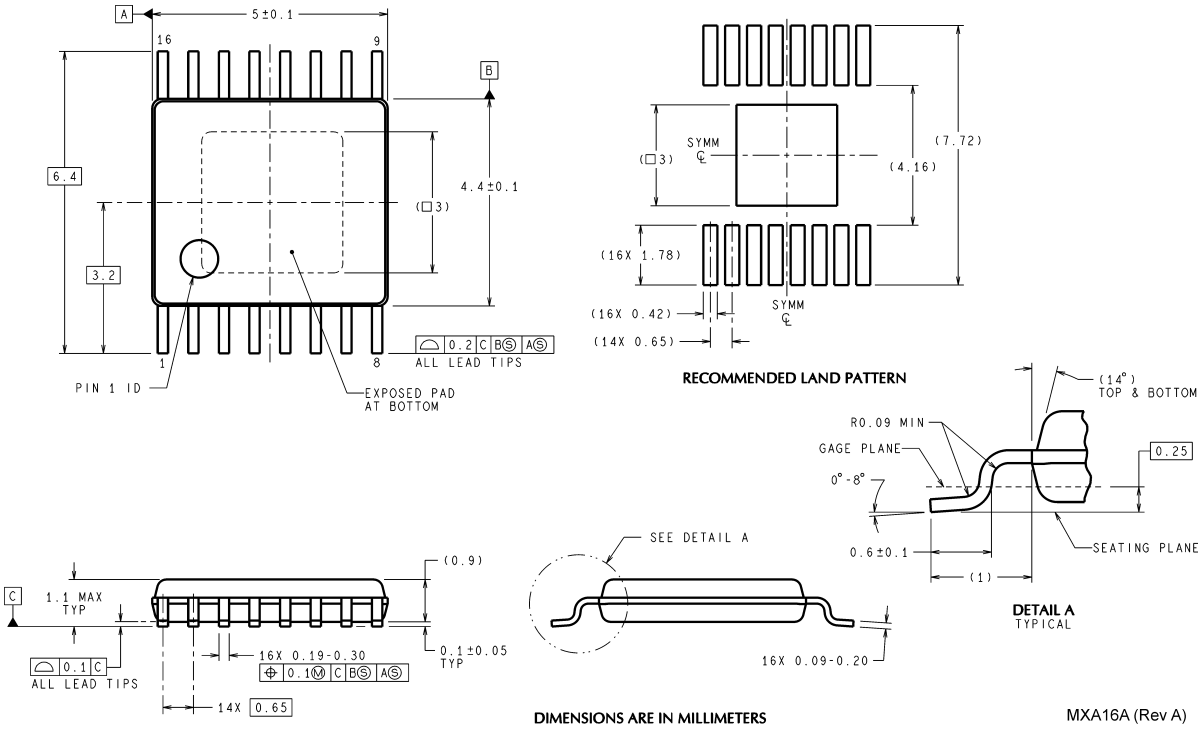
$$Tj = Ta + (PD_{TOTAL} \times \theta_{JA})$$

Where θ_{JA}=38˚C/W (typically) when using a multi-layer board with a large copper plane area. θ_{JA} varies with board type and metallization area.

To calculate the maximum allowable power dissipation, assume Tj = 125˚C. To ensure that junction temperature does not exceed the maximum operating rating of 125˚C, power dissipation should be verified at the maximum expected operating frequency, ambient temperature, and input voltage. The calculated maximum load current is based on continuous operation and may be exceeded during transient conditions.

If the power dissipation remains above the maximum allowable level, device temperature will continue to rise. When the junction temperature exceeds its maximum, the LM26001 engages Thermal Shut Down (TSD). In TSD, the part remains in a shutdown state until the junction temperature falls to within normal operating limits. At this point, the device restarts in soft-start mode.

Physical Dimensions inches (millimeters) unless otherwise noted



eTSSOP-16 Package
16-Lead Exposed Pad TSSOP Package
NS Package Number MXA16A

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