**National Semiconductor**

February 2002

# LMV712
# Low Power, Low Noise, High Output, RRIO Dual Operational Amplifier with Independent Shutdown

## General Description

The LMV712 duals are high performance BiCMOS operational amplifiers intended for applications requiring Rail-to-Rail inputs combined with speed and low noise. They offer a bandwidth of 5MHz and a slew rate of 5V/µs and can handle capacitive loads of up to 200pF without oscillation.

The LMV712 offers two independent shutdown pins. This feature allows disabling of each device separately and reduces the supply current to less than 1µA typical. The output voltage rapidly ramps up smoothly with no glitch as the amplifier comes out of the shutdown mode.

The LMV712 with the shutdown feature is offered in space saving 10-Bump micro SMD and 10 pin Leadless Leadframe Package (LLP) packages. It is also offered in 10 lead MSOP package. These packages are designed to meet the demands of small size, low power, and low cost required by cellular phones and similar battery operated portable electronics.

## Features

(Typical Unless Otherwise Noted)
- 5 MHz GBP
- Slew rate 5 V/µs
- Low noise 20nV/$\sqrt{Hz}$
- Supply current 1.22mA/channel
- $V_{OS}$< 3mV max.
- Low supply voltage 2.7V to 5V.
- Rail-to-Rail inputs and outputs.
- Unity gain stable.
- Small package: 10-Pin LLP, 10-Pin MSOP and 10-Bump micro SMD
- 1.5µA shutdown $I_{CC}$
- 2.2µs turn on

## Applications
- Power amplifier control loop
- Cellular phones
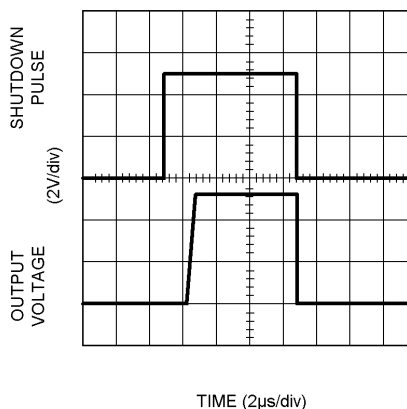- Portable equipment
- Wireless LAN
- Radio systems
- Cordless phones

## Typical Application Circuit
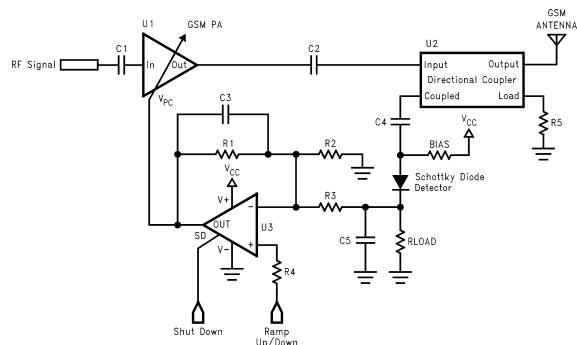


**P.A. Control Loop**

10137034

## Output Waveform vs. Shutdown Pulse



TIME (2µs/div)

10137030

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance (Note 2) | |
| Machine Model | 150V |
| Human Body Model | 1.5kV |
| Differential Input Voltage | ±Supply Voltage |
| Voltage at Input/Output Pin | $(V^+)$ +0.4V to $(V^-)$ −0.4V |
| Supply Voltage $(V^+ - V^-)$ | 5.5V |
| Output Short Circuit $V^+$ | (Note 3) |
| Output Short Circuit $V^-$ | (Note 3) |
| Current at Input Pin | ±10mA |
| Current at Output Pin | ±50mA |
| Storage Temp Range | −65˚C to 150˚C |

| | |
|---|---|
| Mounting Temperature | |
| Infrared or Convection (20 sec) | 235˚C |
| Junction Temperature $T_{JMAX}$ (Note 4) | 150˚C |

## Recommended Operating Conditions (Note 1)

| | |
|---|---|
| Supply Voltage | 2.7V to 5V |
| Temperature Range | $-40\text{°C} \leq T_J \leq 85\text{°C}$ |
| Thermal Resistance | |
| 10-Pin MSOP | 235˚C/W |
| 10-Pin LLP | 53.4˚C/W |
| 10-Bump micro SMD | 196˚C/W |

## 2.7V Electrical Characteristics
Unless otherwise specified, all limits guaranteed for $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.35V and $T_A$ = 25˚C and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Condition | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0.85V and $V_{CM}$ = 1.85V | | 0.4 | 3 **3.2** | mV |
| $I_B$ | Input Bias Current | | | 5.5 | 115 **130** | pA |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 2.7V$ | 50 **45** | 75 | | dB |
| PSRR | Power Supply Rejection Ratio | $2.7V \leq V^+ \leq 5V$, $V_{CM}$ = 0.85V | 70 **68** | 90 | | dB |
| | | $2.7V \leq V^+ \leq 5V$, $V_{CM}$ = 1.85V | 70 **68** | 90 | | dB |
| CMVR | Common Mode Voltage Range | For CMRR ≥ 50dB | | −0.3 | −0.2 | V |
| | | | 2.9 | 3 | | V |
| $I_{SC}$ | Output Short Circuit Current | Sourcing $V_O$ = 0V | 15 **12** | 25 | | mA |
| | | Sinking $V_O$ = 2.7V | 25 **22** | 50 | | mA |
| $V_O$ | Output Swing | $R_L$ = 10kΩ to 1.35V | 2.62 **2.60** | 2.68 | | V |
| | | | | 0.01 | 0.12 **0.15** | V |
| | | $R_L$ = 600Ω to 1.35V | 2.52 **2.50** | 2.55 | | V |
| | | | | 0.05 | 0.23 **0.30** | V |
| $V_O$(SD) | Output Voltage in Shutdown | | | 10 | 200 | mV |
| $I_S$ | Supply Current per Channel | On Mode | | 1.22 | 1.7 **1.9** | mA |
| | | Shutdown Mode | | 0.12 | 1.5 **2.0** | uA |

## 2.7V Electrical Characteristics
Unless otherwise specified, all limits guaranteed for $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.35V and $T_A$ = 25°C and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes. (Continued)

| Symbol | Parameter | Condition | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|
| $A_{VOL}$ | Large Signal Voltage Gain | Sourcing $R_L$ = 10kΩ $V_O$ = 1.35V to 2.3V | 80 **76** | 115 | | dB |
| | | Sinking $R_L$ = 10kΩ $V_O$ = 0.4V to 1.35V | 80 **76** | 113 | | dB |
| | | Sourcing $R_L$ = 600Ω $V_O$ = 1.35V to 2.2V | 80 **76** | 97 | | dB |
| | | Sinking $R_L$ = 600Ω $V_O$ = 0.5V to 1.35V | 80 **76** | 100 | | dB |
| $V_{SD}$ | Shutdown Pin Voltage Range | On Mode | 2.4 to 2.7 | 2.0 to 2.7 | | V |
| | | Shutdown Mode | 0 to 0.8 | 0 to 1 | | V |
| GBWP | Gain-Bandwidth Product | | | 5 | | MHz |
| SR | Slew Rate | (Note 7) | | 5 | | V/µs |
| $\phi_m$ | Phase Margin | | | 60 | | Deg |
| $e_n$ | Input Referred Voltage Noise | f = 1kHz | | 20 | | nV/$\sqrt{Hz}$ |
| $T_{ON}$ | Turn-On Time from Shutdown | | | 2.2 | 4 **4.6** | µs |
| | Turn-On Time from Shutdown (micro SMD) | | 6 **8** | | | µs |

## 5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V^+$ =5V, $V^-$ = 0V, $V_{CM}$ = 2.5V and $T_A$ = 25°C and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Condition | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0.85V and $V_{CM}$ = 1.85V | | 0.4 | 3 **3.2** | mV |
| $I_B$ | Input Bias Current | | | 5.5 | 115 **130** | pA |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 5V | 50 **45** | 80 | | dB |
| PSRR | Power Supply Rejection Ratio | 2.7V ≤ $V^+$ ≤ 5V, $V_{CM}$ = 0.85V | 70 **68** | 90 | | dB |
| | | 2.7V ≤ $V^+$ ≤ 5V, $V_{CM}$ = 1.85V | 70 **68** | 90 | | dB |
| CMVR | Common Mode Voltage Range | For CMRR ≥ 50dB | | −0.3 | −0.2 | V |
| | | | 5.2 | 5.3 | | V |
| $I_{SC}$ | Output Short Circuit Current | Sourcing $V_O$ = 0V | 20 **18** | 35 | | mA |
| | | Sinking $V_O$ = 5V | 25 **21** | 50 | | mA |

## 5V Electrical Characteristics  (Continued)

Unless otherwise specified, all limits guaranteed for $V^+$ =5V, $V^-$ = 0V, $V_{CM}$ = 2.5V and $T_A$ = 25°C and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Condition | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|
| $V_O$ | Output Swing | $R_L$ = 10kΩ to 2.5V | 4.92 **4.90** | 4.98 | | V |
| | | | | 0.01 | 0.12 **0.15** | V |
| | | $R_L$ = 600Ω to 2.5V | 4.82 **4.80** | 4.85 | | V |
| | | | | 0.05 | 0.23 **0.30** | V |
| $V_O$(SD) | Output Voltage in Shutdown | | | 10 | 200 | mV |
| $I_S$ | Supply Current per Channel | On Mode | | 1.17 | 1.7 **1.9** | mA |
| | | Shutdown Mode | | 0.12 | 1.5 **2.0** | uA |
| $A_{VOL}$ | Large Signal Voltage Gain | Sourcing<br>$R_L$ = 10kΩ<br>$V_O$ = 2.5V to 4.6V | 80 **76** | 130 | | dB |
| | | Sinking<br>$R_L$ = 10kΩ<br>$V_O$ = 0.4V to 2.5V | 80 **76** | 130 | | dB |
| | | Sourcing<br>$R_L$ = 600Ω<br>$V_O$ = 2.5V to 4.6V | 80 **76** | 110 | | dB |
| | | Sinking<br>$R_L$ = 600Ω<br>$V_O$ = 0.4V to 2.5V | 80 **76** | 107 | | dB |
| $V_{SD}$ | Shutdown Pin Voltage Range | On Mode | 4.5 to 5 | 3.5 to 5 | | V |
| | | Shutdown Mode | 0 to 0.8 | 0 to 1.5 | | V |
| GBWP | Gain-Bandwidth Product | | | 5 | | MHz |
| SR | Slew Rate | (Note 7) | | 5 | | V/µs |
| $\phi_m$ | Phase Margin | | | 60 | | Deg |
| $e_n$ | Input Referred Voltage Noise | f = 1kHz | | 20 | | nV/$\sqrt{Hz}$ |
| $T_{ON}$ | Turn-On Time for Shutdown | | | 1.6 | 4 **4.6** | µs |
| | Turn-On Time for Shutdown (micro SMD) | | 6 **8** | | | µs |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human body model: 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 100pF.

**Note 3:** Shorting circuit output to either $V^+$ or $V^-$ will adversely affect reliability.

**Note 4:** The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$ and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D$ = $(T_{J(MAX)}$-$T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

**Note 5:** Typical values represent the most likely parametric norm.

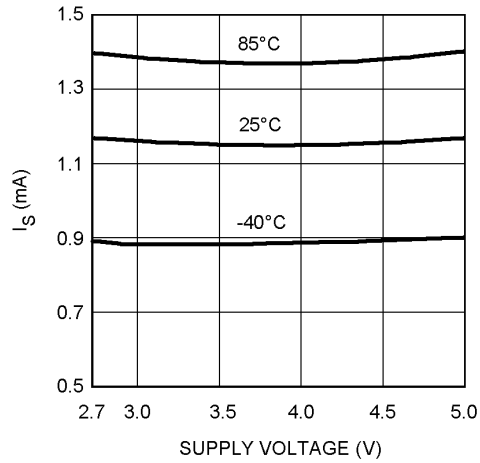**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:** Number specified is the slower of the positive and negative slew rates.

# Typical Performance Characteristics
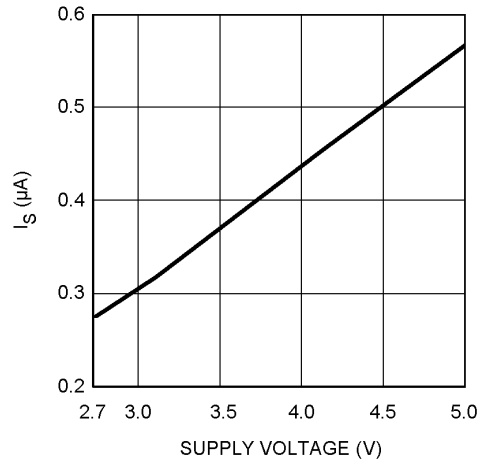Unless otherwise specified, $V_S$ = +5V, single suppy, $T_A$ = 25˚C.

### Supply Current Per Channel vs. Supply Voltage
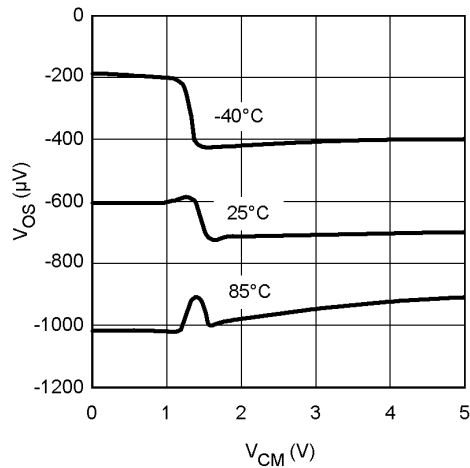


10137001

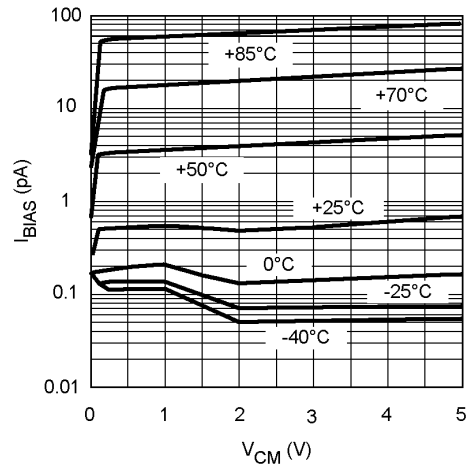### Supply Current vs. Supply Voltage (Shutdown)



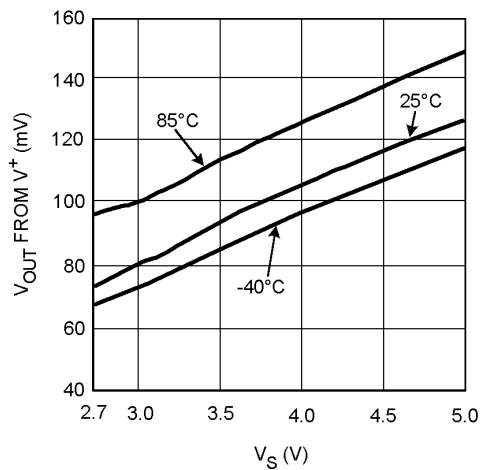10137002

### $V_{OS}$ vs. $V_{CM}$
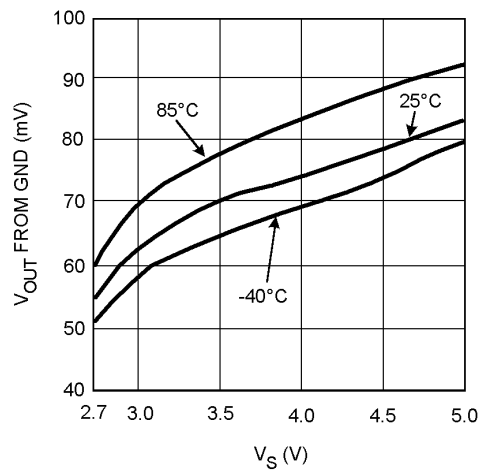


10137003

### $I_B$ vs. $V_{CM}$ Over Temp



10137005

### Output Positive Swing vs. Supply Voltage, $R_L$ = 600$\Omega$



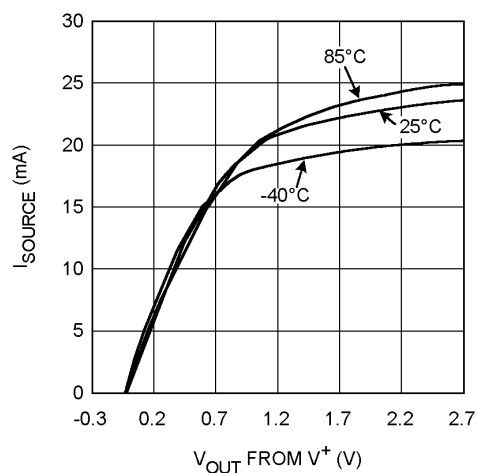10137006

### Output Negative Swing vs. Supply Voltage, $R_L$ = 600$\Omega$



10137007

# Typical Performance Characteristics Unless otherwise specified, $V_S$ = +5V, single suppy, $T_A$ = 25˚C. (Continued)

**Sourcing Current vs. Output Voltage, $V_S$ = 2.7V**



10137008

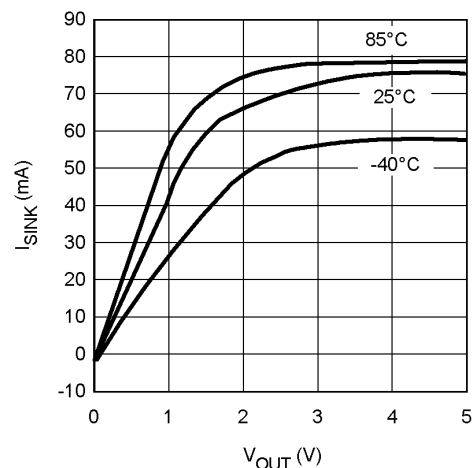**Sourcing Current vs. Output Voltage, $V_S$ = 5V**
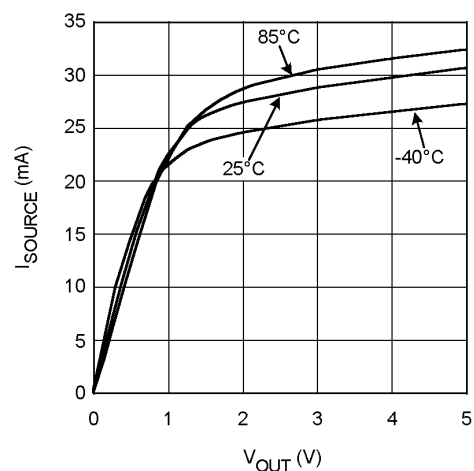


10137010

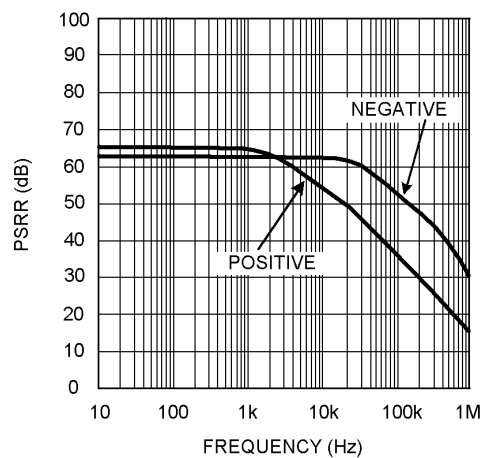**Sinking Current vs. Output Voltage, $V_S$ = 2.7V**
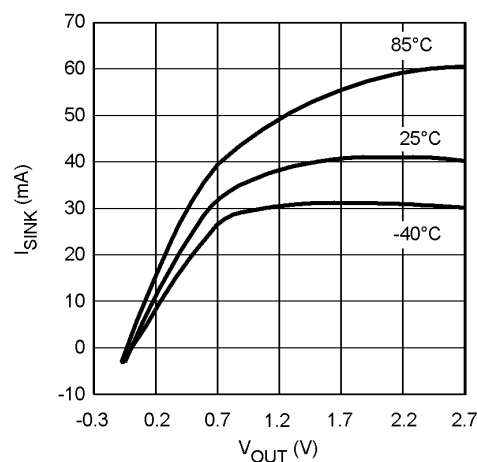


10137009

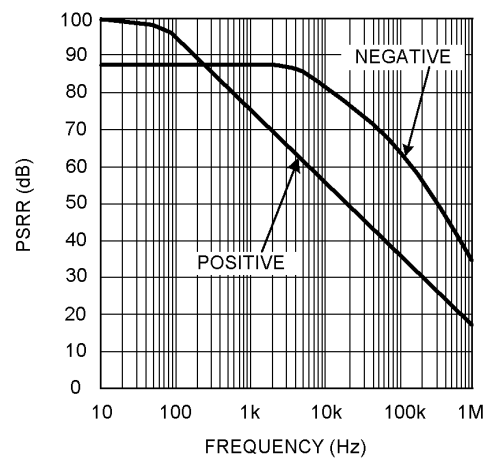**Sinking Current vs. Output Voltage, $V_S$ = 5V**



10137011

**PSRR vs. Frequency $V_S$ = 2.7V**
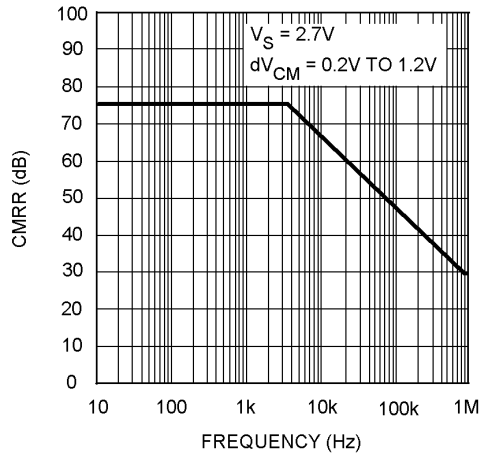


10137018

**PSRR vs. Frequency $V_S$ = 5V**



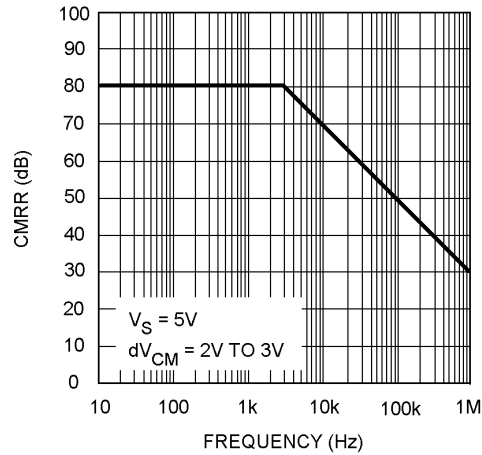10137019

## Typical Performance Characteristics Unless otherwise specified, $V_S$ = +5V, single suppy, $T_A$ = 25˚C. (Continued)
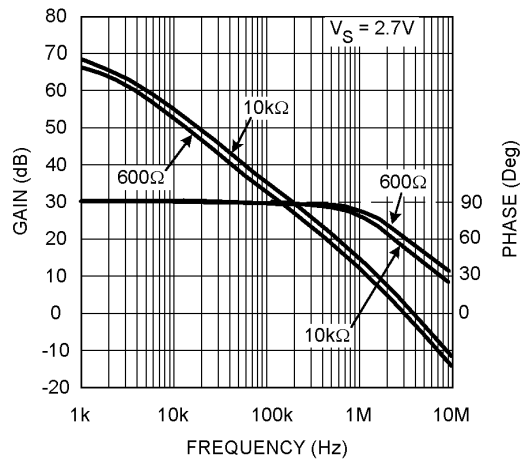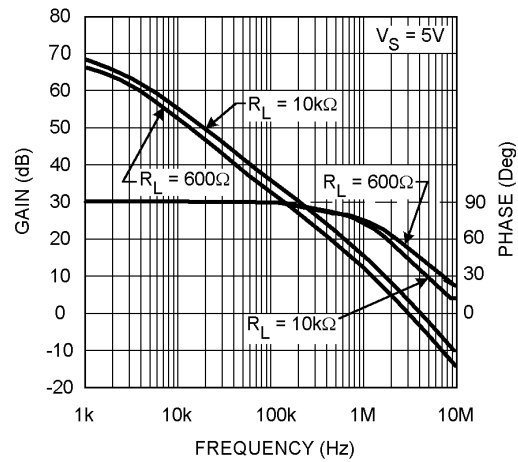
**CMRR vs. Frequency**
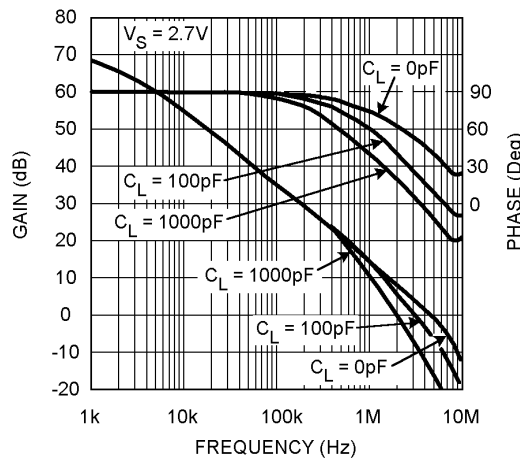


10137016

**CMRR vs. Frequency**



10137017

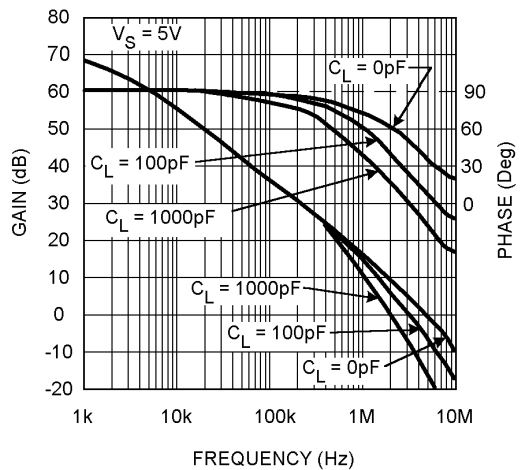**Open Loop Frequency Response vs. $R_L$**



10137012

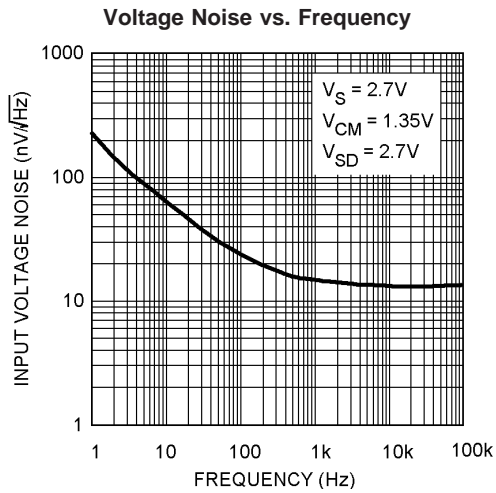**Open Loop Frequency Response vs. $R_L$**



10137014

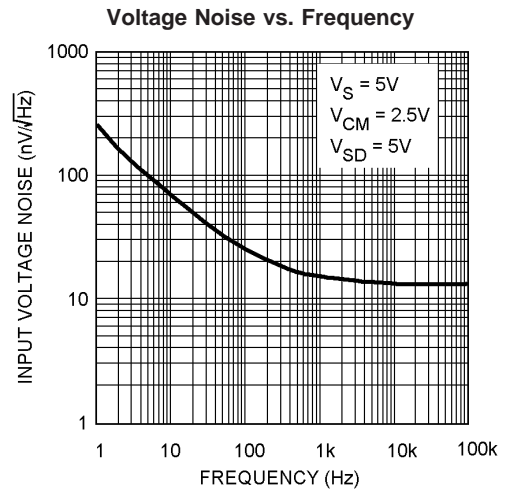**Open Loop Frequency Response vs. $C_L$**



10137013

**Open Loop Frequency Response vs. $C_L$**



10137015

## Typical Performance Characteristics Unless otherwise specified, $V_S$ = +5V, single suppy, $T_A$ = 25˚C. (Continued)

**Voltage Noise vs. Frequency**

$V_S$ = 2.7V
$V_{CM}$ = 1.35V
$V_{SD}$ = 2.7V

INPUT VOLTAGE NOISE (nV/√Hz)

FREQUENCY (Hz)

10137020

**Voltage Noise vs. Frequency**

$V_S$ = 5V
$V_{CM}$ = 2.5V
$V_{SD}$ = 5V

INPUT VOLTAGE NOISE (nV/√Hz)

FREQUENCY (Hz)

10137021

**Non-Inverting Large Signal Pulse Response, $V_S$ = 2.7V**

INPUT

(1V/div)

OUTPUT

TIME (500ns/div)

10137022

**Non-Inverting Large Signal Pulse Response, $V_S$ = 5V**

INPUT

(1V/div)

OUTPUT

TIME (500ns/div)

10137024

**Non-Inverting Small Signal Pulse Response, $V_S$ = 2.7V**

INPUT

(50mV/div)

OUTPUT

TIME (500ns/div)

10137023

**Non-Inverting Small Signal Pulse Response, $V_S$ = 5V**

INPUT

(50mV/div)

OUTPUT
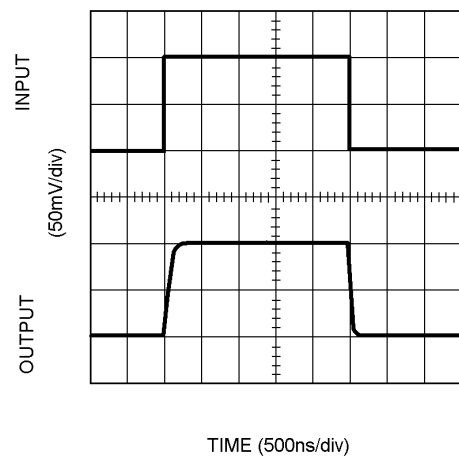
TIME (500ns/div)

10137025

# Typical Performance Characteristics Unless otherwise specified, $V_S$ = +5V, single suppy, $T_A$ = 25˚C. (Continued)

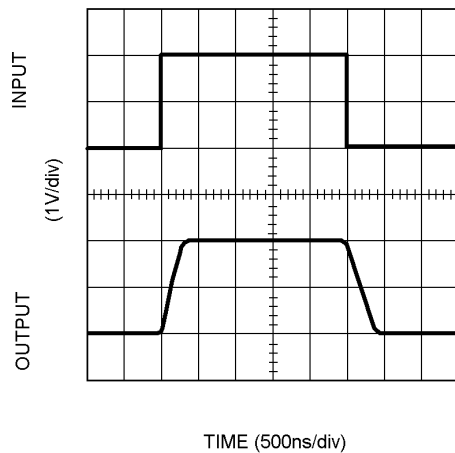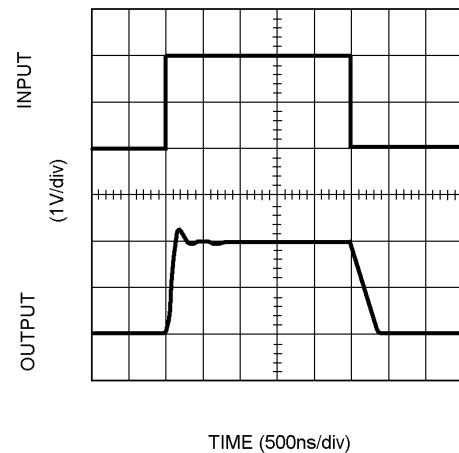**Inverting Large Signal Pulse Response, $V_S$ = 2.7V**

INPUT

(1V/div)

OUTPUT

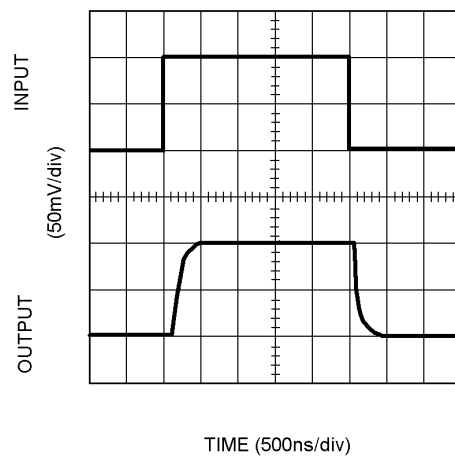TIME (500ns/div)

10137026

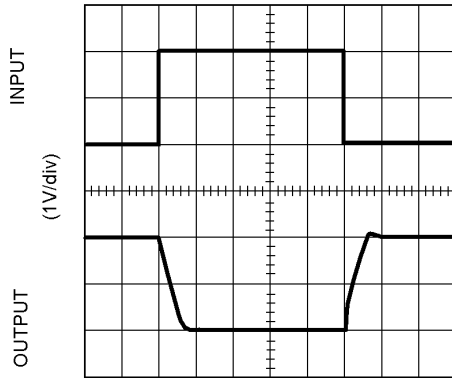**Inverting Large Signal Pulse Response, $V_S$ = 5V**

INPUT

(1V/div)

OUTPUT
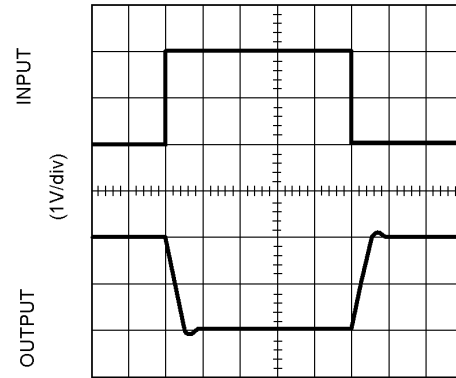
TIME (500ns/div)

10137028

**Inverting Small Signal Pulse Response, $V_S$ = 2.7V**

INPUT

(50mV/div)

OUTPUT
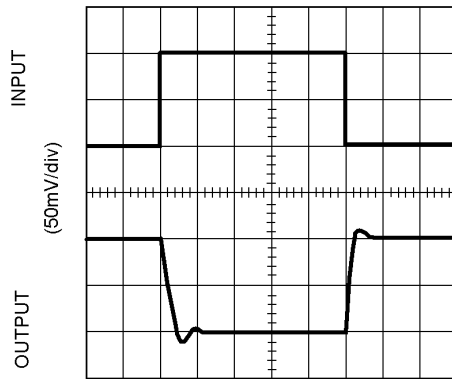
TIME (500ns/div)

10137027

**Inverting Small Signal Pulse Response $V_S$ = 5V**

INPUT

(50mV/div)

OUTPUT
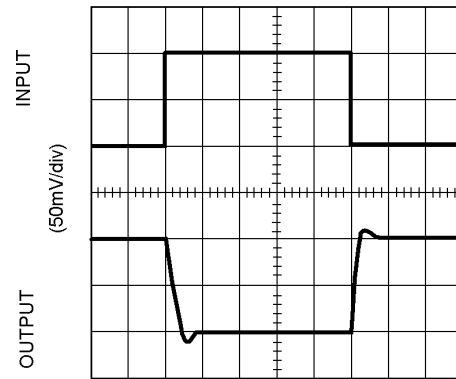
TIME (500ns/div)

10137029

**Turn on Time Response $V_S$ = 5V**

SHUTDOWN PULSE

(2V/div)

OUTPUT VOLTAGE
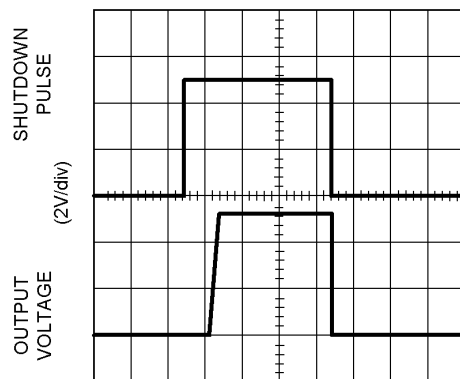
TIME (2µs/div)

10137030

**Input Common Mode Capacitance vs. $V_{CM}$ $V_S$ = 5V**

$C_{CM}$ TO GROUND
FMEAS = 1MHz
FOLLOWER CONFIG

$V_{OUT}$ FOLLOWS $V_{IN}$ ($V_{CM}$)

$C_{DIFF}$ (pF)

$V_{CM}$ (V)
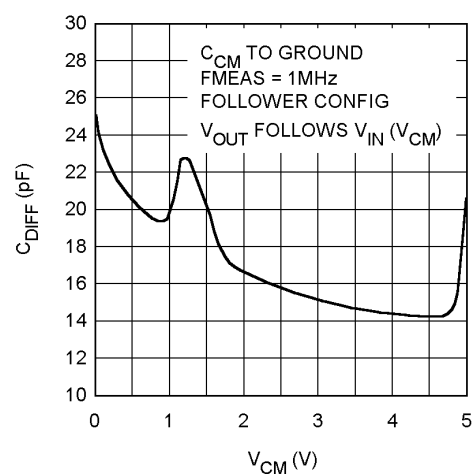
10137004

# Application Information

## Theory of Operation

The LMV712 dual op amp is derived from the LMV711 single op amp. *Figure 1* contains a simplified schematic of one channel of the LMV712.



10137031

**FIGURE 1.**

Rail-to-Rail input is achieved by using in parallel, one NMOS differential pair (MN1 and MN2) and one PMOS differential pair (MP1 and MP2). When the common mode input voltage ($V_{CM}$) is nea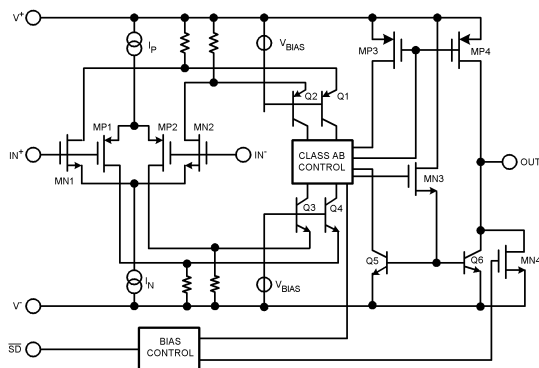r $V^+$, the NMOS pair is on and the PMOS pair is off. When $V_{CM}$ is near $V^-$, the NMOS pair is off and the PMOS pair is on. When $V_{CM}$ is between $V^+$ and $V^-$, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage ($V_{OS}$) characteristic, the offset voltage of the LMV712 becomes a function of $V_{CM}$. $V_{OS}$ has a crossover point at 1.4V above $V^-$. Refer to the '$V_{OS}$ vs. $V_{CM}$' curve in the Typical Performance Characteristics section. Caution should be taken in situations where input signal amplitude is comparable to $V_{OS}$ value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The current coming out of the input differential pairs gets mirrored through two folded cascode stages (Q1, Q2, Q3, Q4) into the 'class AB control' block. This circuitry generates voltage gain, defines the op amp's dominant pole and limits the maximum current flowing at the output stage. MN3 introduces a voltage level shift and acts as a high impedance to low impedance buffer.

The output stage is composed of a PMOS and a NPN transistor in a common source/emitter configuration, delivering a rail-to-rail output excursion.

The MN4 transistor ensures that the LMV712 output remains near $V^-$ when the amplifier is in shutdown mode.

## Shutdown Pin

The LMV712 offers independent shutdown pins for the dual amplifiers. When the shutdown pin is tied low, the respective amplifier shuts down and the supply current is reduced to less than 1μA. In shutdown mode, the amplifier's output level stays at $V^-$. In a 2.7V operation, when a voltage between 1.5V to 2.7V is applied to the shutdown pin, the amplifier is enabled. As the amplifier is coming out of the shutdown mode, the output waveform ramps up without any glitch. This is demonstrated in *Figure 2*.
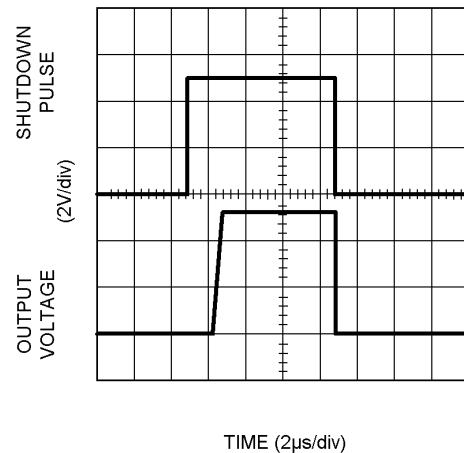


10137030

**FIGURE 2.**

A glitch-free output waveform is highly desirable in many applications, one of which is power amplifier control loops. In this application, the LMV712 is used to drive the power amplifier's power control. If the LMV712 did not have a smooth output ramp during turn on, it would directly cause the power amplifier to produce a glitch at its output. This adversely affects the performance of the system.

To enable the amplifier, the shutdown pin must be pulled high. It should not be left floating in the event that any leakage current may inadvertently turn off the amplifier.

## Printed Circuit Board Consideration

To properly bypass the power supply, several locations on a printed circuit board need to be considered. A 6.8μF or greater tantalum capacitor should be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1μF ceramic capacitor should be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the $V^+$ pin needs to be bypassed with a 0.1μF capacitor. If the amplifier is operated in a dual power supply, both $V^+$ and $V^-$ pins need to be bypassed.

It is good practice to use a ground plane on a printed circuit board to provide all components with a low inductive ground connection.

Surface mount components in 0805 size or smaller are recommended in the LMV712 application circuits. Designers can take advantage of the micro SMD, MSOP and LLP miniature sizes to condense board layout in order to save space and reduce stray capacitance.

## Capacitive Load Tolerance

The LMV712 can directly drive 200pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an under-damped pulse response or oscillation. To drive a heavier capacitive load, *Figure 3* can be used.

10

## Application Information (Continued)
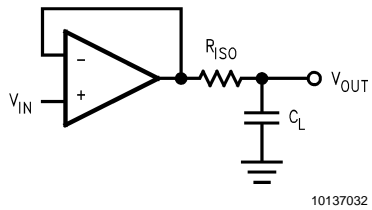


10137032

**FIGURE 3.**

In *Figure 3*, the isolation resistor $R_{ISO}$ and the load capacitor $C_L$ form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of $R_{ISO}$. The bigger the $R_{ISO}$ resistor value, the more stable $V_{OUT}$ will be. But the DC accuracy is degraded when the $R_{ISO}$ gets bigger. If there were a load resistor in *Figure 3*, the output voltage would be divided by $R_{ISO}$ and the load resistor.

The circuit in *Figure 4* is an improvement to the one in *Figure 3* because it provides DC accuracy as well as AC stability. In this circuit, $R_F$ provides the DC accuracy by using feed-forward techniques to connect $V_{IN}$ to $R_L$. $C_F$ and $R_{ISO}$ serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin

in the overall feedback loop. Increased capacitive drive is possible by increasing the value of $C_F$. This in turn will slow down the pulse response.



10137033
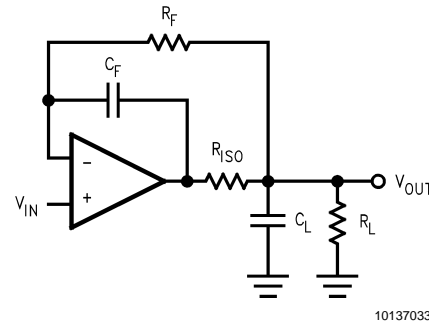
**FIGURE 4.**

**Latchup**

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR (silicon controlled rectifier) effects. The input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMV712 is designed to withstand 150mA surge current on all the pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

# Connection Diagrams

**10-Pin MSOP**

OUT A  1
-IN A   2
+IN A   3
V⁻      4
SD A    5

10  V⁺
9   OUT B
8   -IN B
7   +IN B
6   SD B

10137036

**Top View**

**10-Pin LLP**

OUT A  1
-IN A   2
+IN A   3
V⁻      4
SD A    5

10  V⁺
9   OUT B
8   -IN B
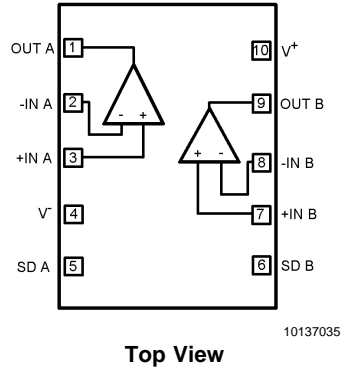7   +IN B
6   SD B

10137035
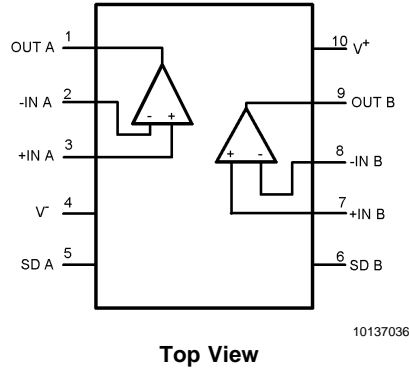
**Top View**

**10-Bump micro SMD**

A2
V⁺

A1 OUTA
B1 -INA
C1 +INA
D1 SDA

A3 OUTB
B3 -INB
C3 +INB
D3 SDB

V⁻
D2

10137037

**Top View**

A2
V⁺

A3 OUTB
B3 -INB
C3 +INB
D3 SDB

A1 OUTA
B1 -INA
C1 +INA
D1 SDA

V⁻
D2

10137038
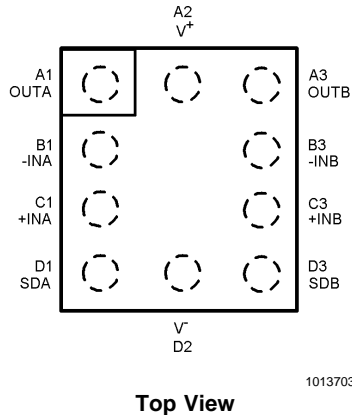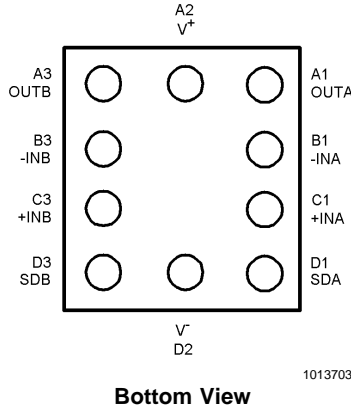
**Bottom View**

## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 10-Pin MSOP | LMV712MM | A61 | 1k Units Tape and Reel | MUB10A |
| | LMV712MMX | | 3.5k Units Tape and Reel | |
| 10-Pin LLP | LMV712LD | A62 | 1k Units Tape and Reel | LDA10A |
| | LMV712LDX | | 3.5k Units Tape and Reel | |
| 10-Bump micro SMD | LMV712BL | A76A | 250 Units Tape and Reel | BLP10AAB |
| | LMV712BLX | | 3k Units Tape and Reel | |

# Physical Dimensions   inches (millimeters)
unless otherwise noted
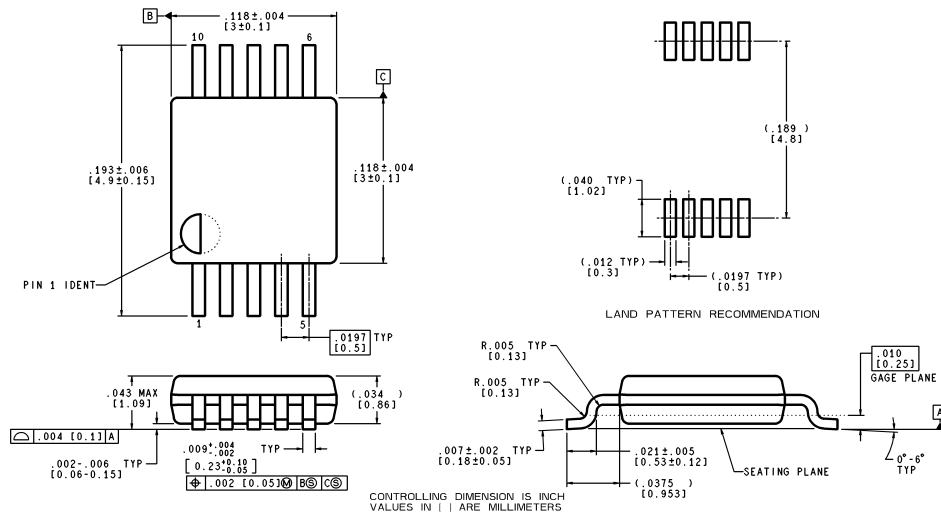
**10-Pin MSOP**
**NS Package Number MUB10A**
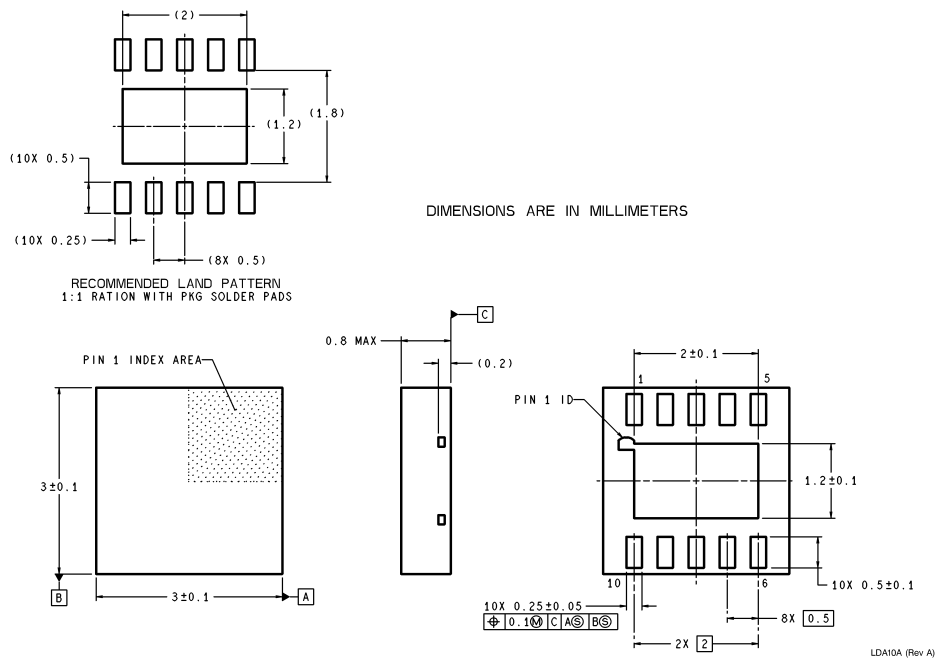
**10-Pin LLP**
**NS Package Number LDA10A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

SYMM

10X Ø 0.275 / 0.250

SYMM

(0.5)

(0.5)

DIMENSIONS ARE IN MILLIMETERS

**LAND PATTERN RECOMMENDATION**

TOP SIDE COATING

BUMP A1 CORNER

X3

0.125 / 0.050

C

BUMP

SILICON

0.235 / 0.205

B

X2

SYMM

SYMM

X1

0.5

D    C    B    A

0.5

10X Ø 0.31 / 0.29

⊕ 0.005Ⓢ C AⓈ BⓈ

A

BLP10XXX (Rev B)

**10-Bump micro SMD**
**NS Package Number BLP10AAB**
**X1 = 1.514 ±0.030mm      X2 = 1.996±0.030mm      X3 = 0.945 ±0.100mm**

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

### LIFE SUPPORT POLICY