Replacement of
**MC34063A**

# DC-to-DC Converter Control Circuits

**MIK34063A**

October 1997 – revised November 1999

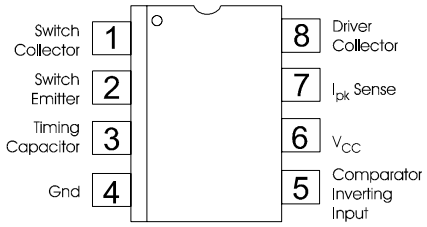
## Description

The MIK34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

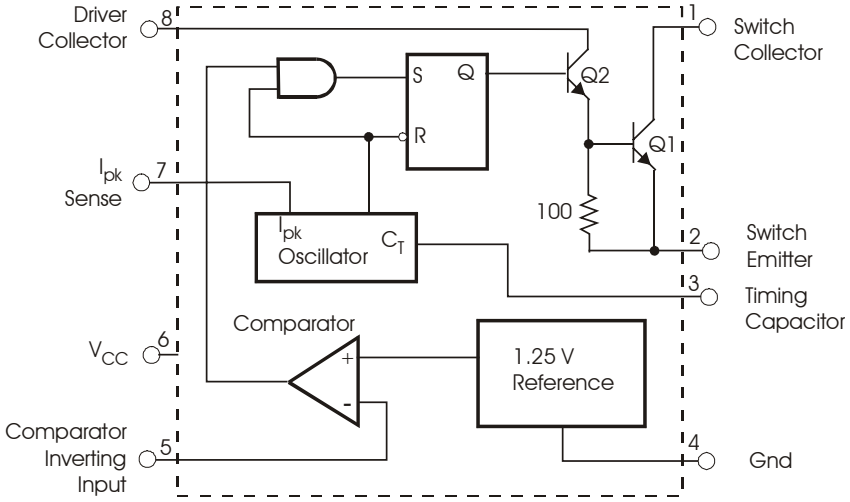
## Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

## Pin connections




## Schematic Diagram




## Absolute Maximum Ratings

| Symbol | Parameter | Maximum | Units |
|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 40 | Vdc |
| $V_{IR}$ | Comparator Input Voltage Range | -0.3 to +40 | Vdc |
| $V_{C(switch)}$ | Switch Collector Voltage | 40 | Vdc |
| $V_{E(switch)}$ | Switch Emitter Voltage ($V_{PIN1}$ = 40 V) | 40 | Vdc |
| $V_{CE(switch)}$ | Switch Collector to Emitter Voltage | 40 | Vdc |
| $V_{C(driver)}$ | Driver Collector Voltage | 40 | Vdc |
| $I_{C(driver)}$ | Driver Collector Current (Note 1) | 100 | mA |
| $I_{SW}$ | Switch Current | 1.5 | A |
| $T_J$ | Operating Junction Temperature | +150 | °C |
| $T_A$ | Operating Ambient Temperature Range | 0 to +70 | °C |
| Tstg | Storage Temperature Range | -65 to +150 | °C |

## Electrical characteristics

(Vcc = 5.0 V, $T_A = T_{low}$ to $T_{high}$ , unless otherwise specified.)

| Characteristics | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Frequency ($V_{pin5}$ = 0V, $C_T$ = 1.0 nF, $T_A$ = 25°C) | $f_{OSC}$ | 24 | 33 | 42 | kHz |
| Charge Current($V_{CC}$ = 5.0V to 40V, $T_A$ = 25°C) | $I_{chg}$ | 24 | 35 | 42 | µA |
| Discharge Current ($V_{CC}$ = 5.0V to 40V, $T_A$ = 25°C) | $I_{dischg}$ | 140 | 220 | 260 | µA |
| Discharge to Charge Current Ratio (Pin 7 to $V_{CC}$, $T_A$ = 25°C) | $I_{dischg}$ / $I_{chg}$ | 5.2 | 6.5 | 7.5 | – |
| Current Limit Sense Voltage ($I_{chg}$ = $I_{dischg}$, $T_A$ = 25°C) | $V_{ipk(sence)}$ | 250 | 300 | 350 | mV |
| **OUTPUT SWITCH (NOTE 2)** | | | | | |
| Saturation Voltage, Darlington Connection ($I_{SW}$ = 1.0 A, Pins 1, 8 connected) | $V_{CE(sat)}$ | – | 1.0 | 1.3 | V |
| Saturation Voltage, Darlington Connection ($I_{SW}$ = 1.0 A, $R_{pin\ 8}$ = 82Ω to $V_{CC}$ , Forced β ≅ 20) | $V_{CE(sat)}$ | – | 0.45 | 0.7 | V |
| DC Current Gain ($I_{SW}$ = 1.0 A, $V_{CE}$ = 5.0 V, $T_A$ = 25°C) | $h_{FE}$ | 50 | 75 | – | – |
| Collector Off-State Current ($V_{CE}$ = 40 V) | $I_{C(off)}$ | – | 40 | 100 | µA |
| **COMPARATOR** | | | | | |
| Threshold Voltage<br>($T_A$=25°C)<br>($T_A$ =$T_{low}$ to $T_{high}$) | Vth | <br>1.225<br>1.21 | <br>1.25<br>– | <br>1.275<br>1.29 | V |
| Threshold Voltage Line Regulation<br>(Vcc=3.0 V to 40 V) | $Reg_{line}$ | – | 1.4 | 5.0 | mV |
| Input Bias Current<br>(Vin=0 V) | $I_{IB}$ | – | -20 | -400 | nA |
| **TOTAL DEVICE** | | | | | |
| Supply Current (Vcc = 5.0 V to 40 V, $C_T$ = 1.0 nF, Pin 7 = $V_{CC}$, Vpin 5 > Vth, Pin 2 = Gnd, remaining pins open) | $I_{CC}$ | – | – | 4.0 | mA |

Note1: Maximum package power dissipation limits must be observed.
Note2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

## Typical Performance Characteristics

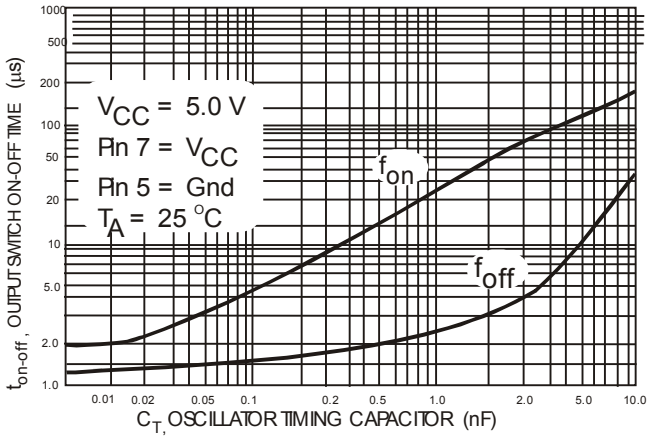



Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor.

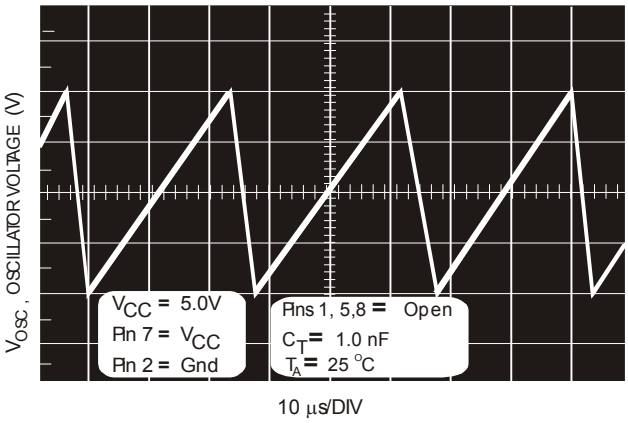



Figure 2. Timing Capacitor Waveform.

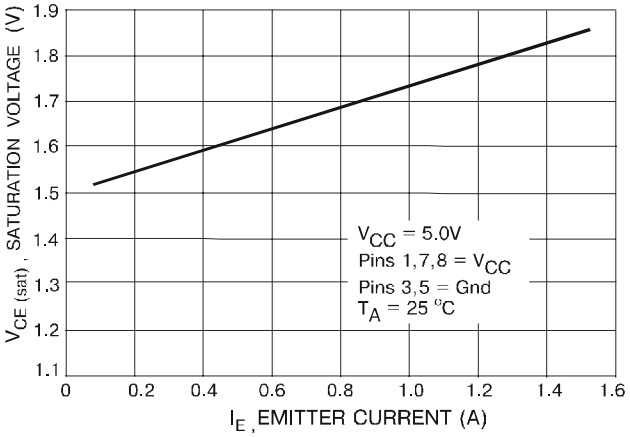



Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current.

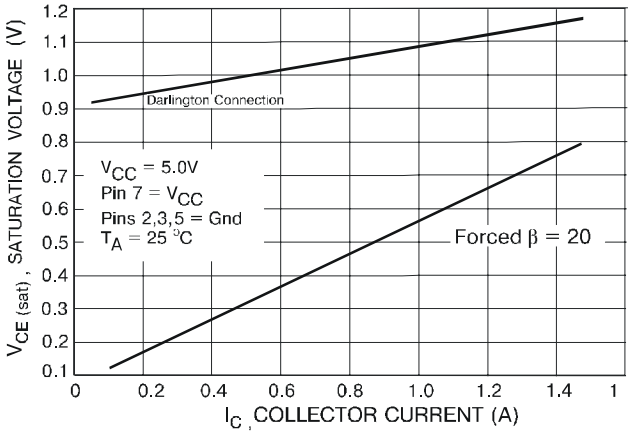



Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current.

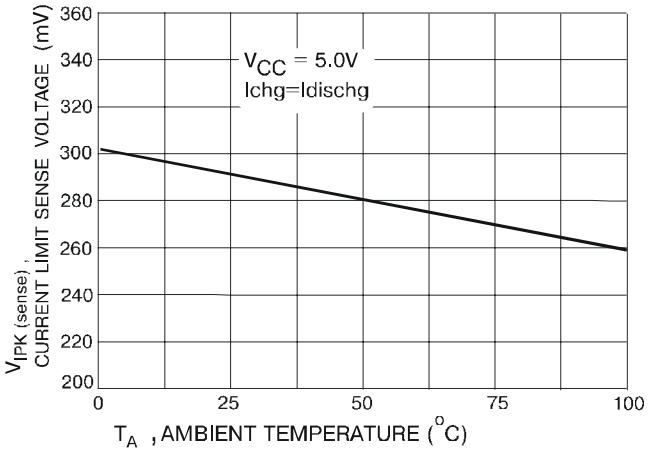



Figure 5. Current Limit Sense Voltage versus Temperature.

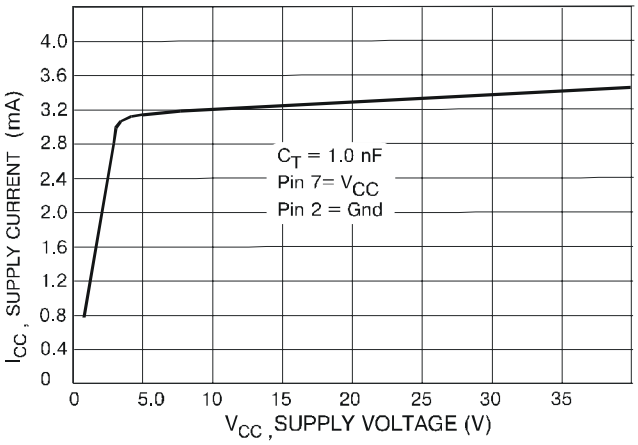



Figure 6. Standby Supply Current versus Supply Voltage.

## Application Information

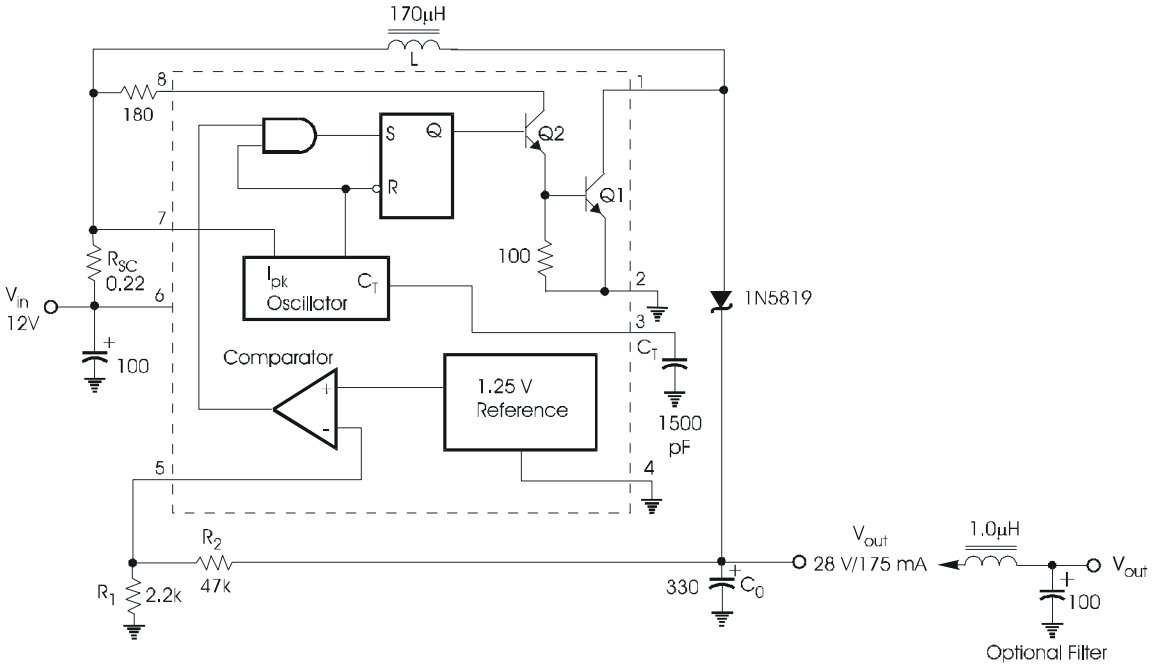



Figure 1. Step-Up Converter.

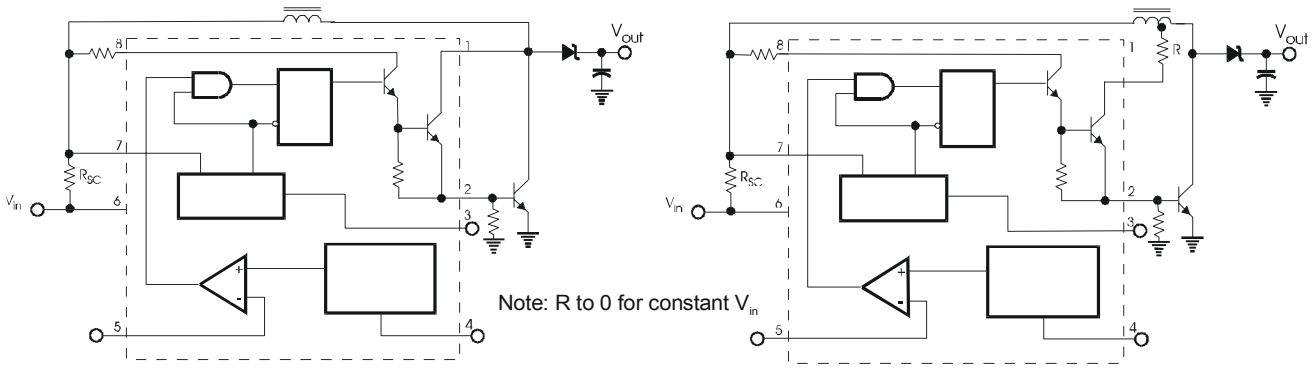



Figure 2a. External NPN Switch.

Figure 2b. External NPN Saturated Switch.

Figure 2. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A.

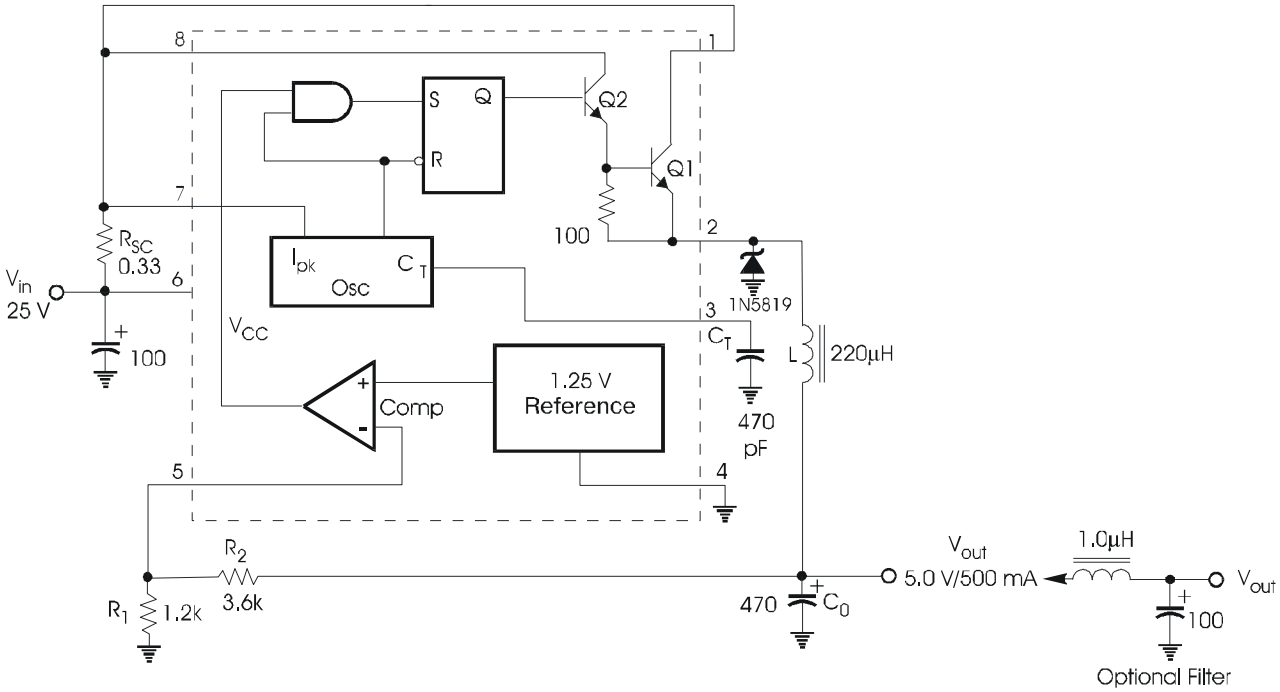



Figure 3. Step-Down Converter.

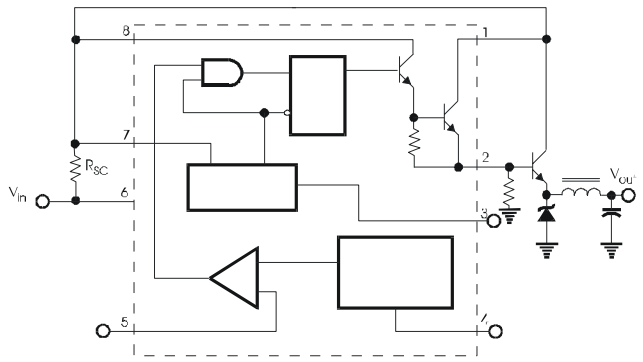



Figure 4a. External NPN Switch.

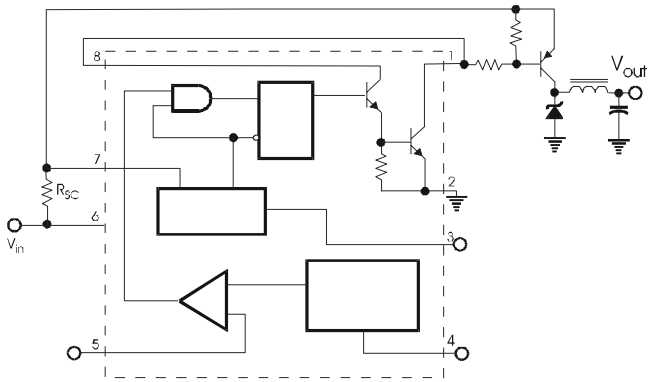



Figure 4b. External PNP Suturated Switch.

Figure 4. External Current Boost Connections for $I_c$ Peak Greater than 1.5 A.

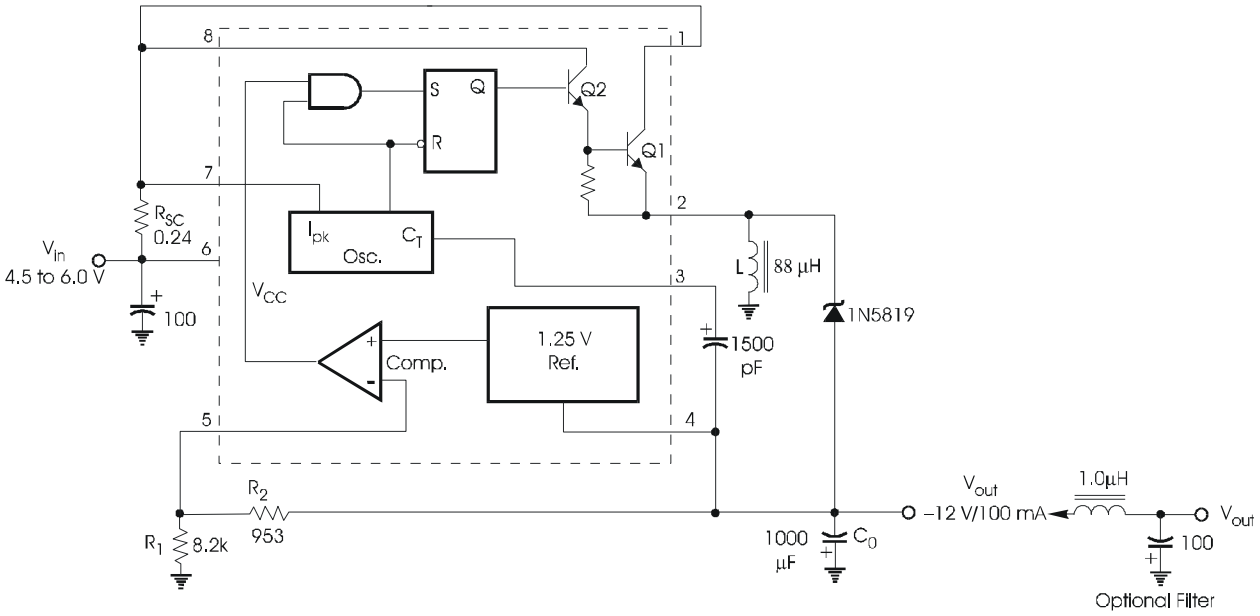



Figure 5. Voltage Inverting Converter.

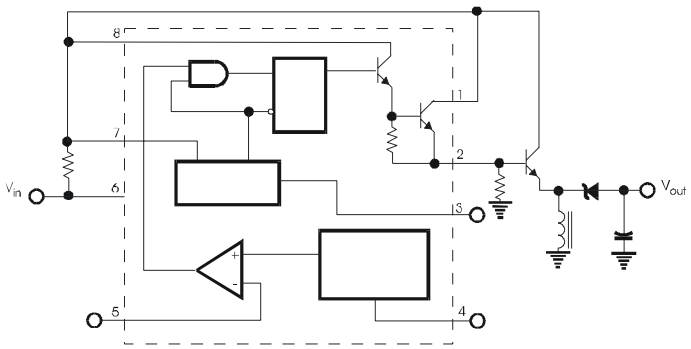



Figure 6a. External NPN Switch.

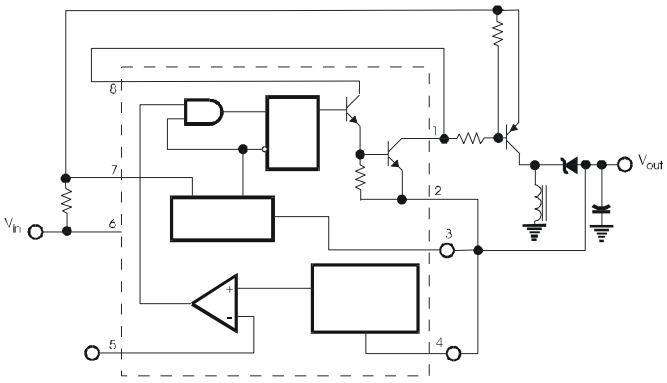



Figure 6b. External PNP Saturated Switch.

Figure 6. External Current Boost Connections for $I_c$ Peak Greater than 1.5 A.

## Design Formula Table

| Calculation | Step-Up | Step-Down | Voltage-Inverting |
|---|---|---|---|
| $t_{on}/t_{off}$ | $\frac{V_{out}+V_F-V_{in(\min)}}{V_{in(\min)}-V_{sat}}$ | $\frac{V_{out}+V_F}{V_{in(\min)}-V_{sat}-V_{out}}$ | $\frac{\lvert V_{out}\rvert+V_F}{V_{in}+V_{sat}}$ |
| $(t_{on}+t_{off})max$ | $\frac{1}{f_{min}}$ | $\frac{1}{f_{min}}$ | $\frac{1}{f_{min}}$ |
| $C_T$ | $4.0 \times 10^{-5}\ t_{on}$ | $4.0 \times 10^{-5}\ t_{on}$ | $4.0 \times 10^{-5}\ t_{on}$ |
| $I_{pk(switch)}$ | $2I_{out(\max)}\left(\frac{t_{on}}{t_{off}}+1\right)$ | $2I_{out(\max)}$ | $2I_{out(\max)}\left(\frac{t_{on}}{t_{off}}+1\right)$ |
| $R_{SC}$ | $0.3/I_{pk(switch)}$ | $0.3/I_{pk(switch)}$ | $0.3/I_{pk(switch)}$ |
| $L_{(min)}$ | $\left(\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(\max)}$ | $\left(\frac{V_{in(\min)}-V_{sat}-V_{out}}{I_{pk(switch)}}\right)\times t_{on(\max)}$ | $\left(\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(\max)}$ |
| $C_O$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ | $\frac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(pp)}}$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ |

**TERMS AND DEFINITIONS**

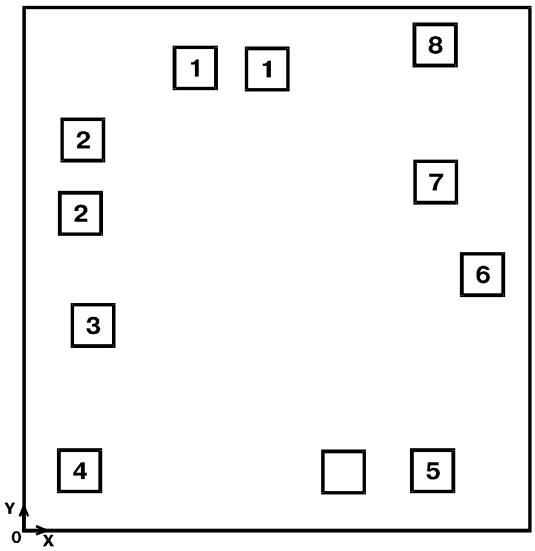
$V_{sat}$ - Saturation voltage of the output switch.
$V_F$ - Forward voltage drop of the output rectifier.

**The following power supply characteristics must be chosen:**

$$|V_{out}| = 1.25\left(1+\frac{R_2}{R_1}\right)$$

$V_{in}$ - Nominal input voltage.
$V_{out}$ - Desired output voltage,
$I_{out}$ - Desired output current.
$f_{min}$ - Minimum desired output switching frequency at the selected values of $V_{in}$ and $I_O$.
$V_{ripple(p-p)}$ –Desired peack-to-peack output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

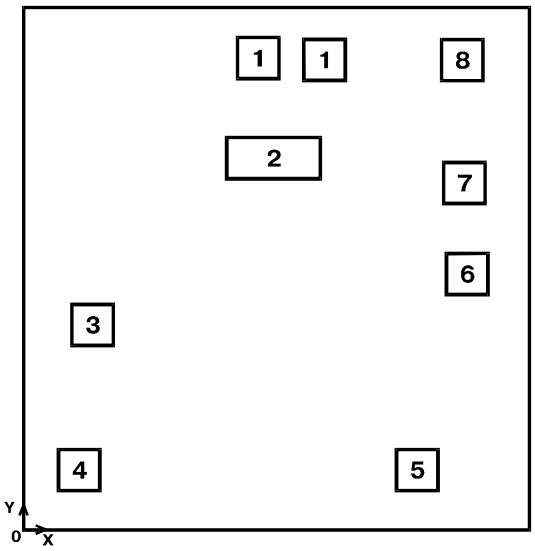
## Pad Location MIK 34063A




Chip size: 1.95 x 2.0 mm

| Pad N | Pad name |
|---|---|
| 1 | Switch Collector |
| 2 | Switch Emitter |
| 3 | Timing Capacitor |
| 4 | Gnd |
| 5 | Comparator Inverting Input |
| 6 | $V_{CC}$ |
| 7 | $I_{pk}$ Sence |
| 8 | Driver Collector |

## Pad Location MIK 34063A (new design)




Chip size: 1.72 x 1.82 mm

| Pad N | Pad name |
|---|---|
| 1 | Switch Collector (Note 1) |
| 2 | Switch Emitter (Note 1) |
| 3 | Timing Capacitor |
| 4 | Gnd |
| 5 | Comparator Inverting Input |
| 6 | $V_{CC}$ |
| 7 | $I_{pk}$ Sence |
| 8 | Driver Collector |

Note 1: Two wires must be connected to 1 and 2 pin.