Preferred Devices

# **Complementary Silicon Plastic Power Transistors**

Designed for use as high-frequency drivers in audio amplifiers.

#### **Features**

• DC Current Gain Specified to 5.0 Amperes

 $\begin{array}{l} h_{FE} \, = 70 \; (Min) \; @ \; I_{C} = 0.5 \; Adc \\ = 10 \; (Min) \; @ \; I_{C} = 2.0 \; Adc \end{array}$ 

• Collector-Emitter Sustaining Voltage -

 $V_{CEO(sus)} = 250 \text{ Vdc (Min)} - \text{MJE}15032, \text{MJE}15033$ 

• High Current Gain – Bandwidth Product

 $f_T = 30 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc}$ 

• TO-220AB Compact Package

• Epoxy Meets UL 94 V-0 @ 0.125 in

• ESD Ratings: Machine Model C

Human Body Model 3B

• Pb-Free Packages are Available\*

# **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit	
Collector–Emitter Voltage	$V_{CEO}$	250	Vdc	
Collector-Base Voltage	$V_{CB}$	250	Vdc	
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc	
Collector Current – Continuous – Peak	I <sub>C</sub>	8.0 16	Adc	
Base Current	Ι <sub>Β</sub>	2.0	Adc	
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	50 0.40	W W/°C	
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2.0 0.016	W W/°C	
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	°C	

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

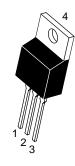


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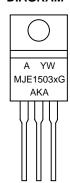
http://onsemi.com

# 8.0 AMPERES POWER TRANSISTORS COMPLEMENTARY SILICON 250 VOLTS, 50 WATTS

# MARKING DIAGRAM



TO-220 CASE 221A STYLE 1



MJE1503x = Specific Device Code

x = 2 or 3

A = Assembly Location

Y = Year
W = Work Week
G = Pb-Package

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MJE15032	TO-220	50 Units/Rail
MJE15032G	TO-220 (Pb-Free)	50 Units/Rail
MJE15033	TO-220	50 Units/Rail
MJE15033G	TO-220 (Pb-Free)	50 Units/Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Preferred** devices are recommended choices for future use and best overall value.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 1) $(I_C = 10 \text{ mAdc}, I_B = 0)$	V <sub>CEO(sus)</sub>	250	-	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 250 Vdc, I <sub>E</sub> = 0)	Ісво	-	10	μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	10	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain $ \begin{aligned} &(I_C=0.5 \text{ Adc, } V_{CE}=5.0 \text{ Vdc}) \\ &(I_C=1.0 \text{ Adc, } V_{CE}=5.0 \text{ Vdc}) \\ &(I_C=2.0 \text{ Adc, } V_{CE}=5.0 \text{ Vdc}) \end{aligned} $	h <sub>FE</sub>	70 50 10	_ _ _	-
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.1 Adc)	V <sub>CE(sat)</sub>	-	0.5	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	V <sub>BE(on)</sub>	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (Note 2) (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1.0 MHz)	f⊤	30	_	MHz

<sup>1.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%. 2.  $f_T = |h_{fe}| \bullet f_{test}$ .

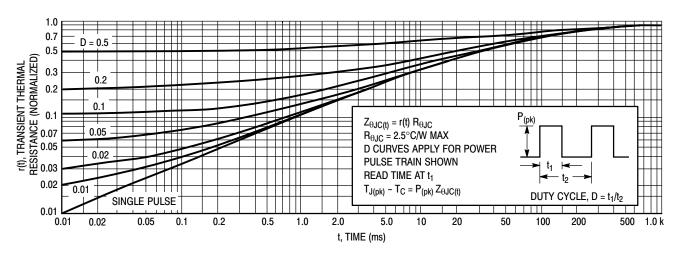


Figure 1. Thermal Response

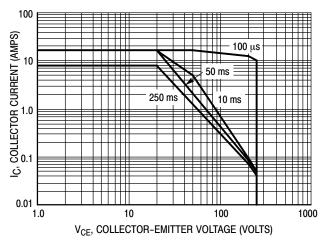


Figure 2. MJE15032 & MJE15033 Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 2 and 4 is based on  $T_{J(pk)}=150^{\circ}C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)}$  < 150°C.  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

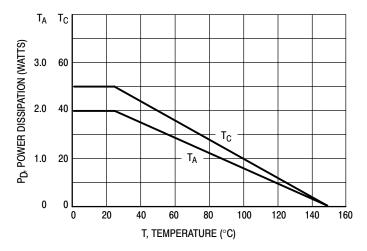
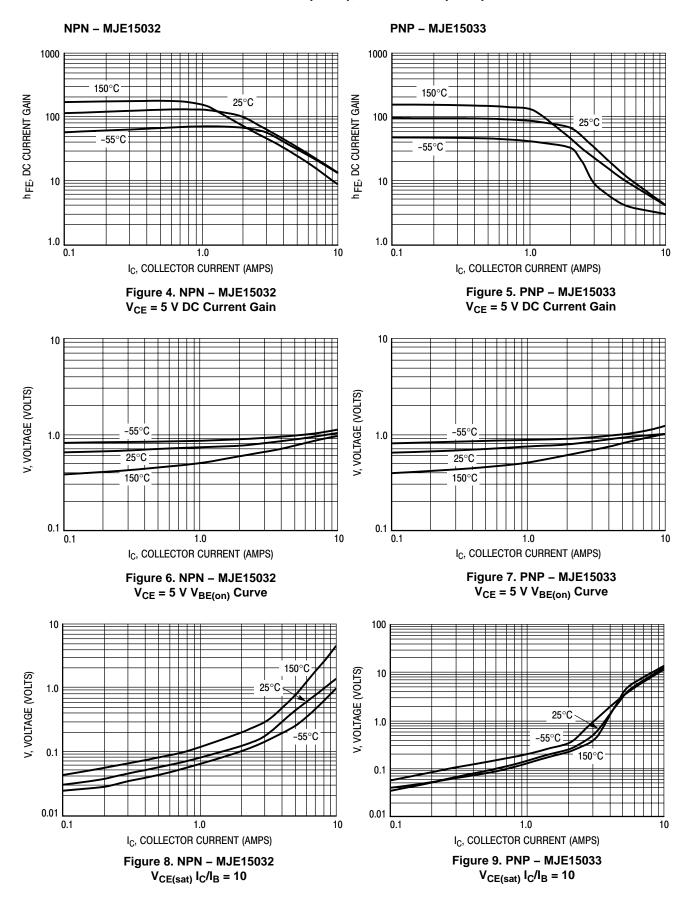
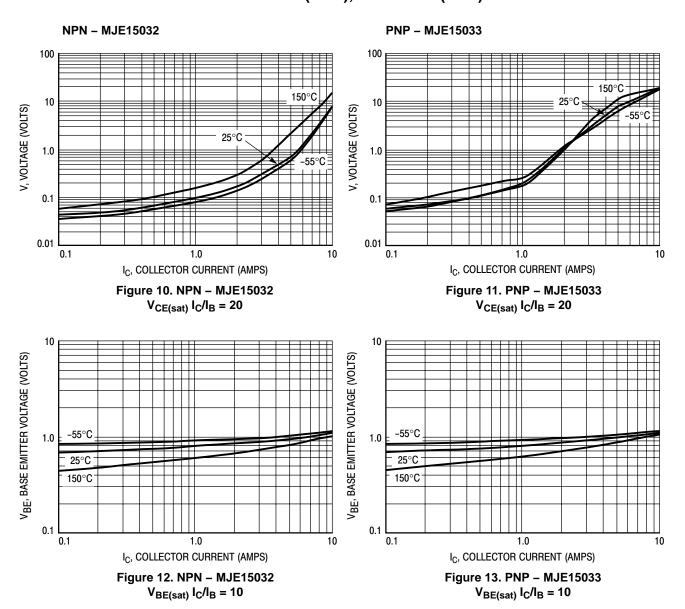


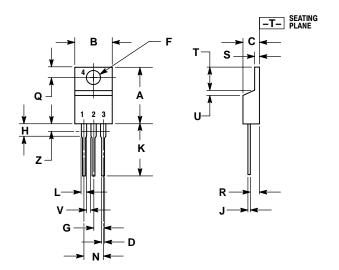
Figure 3. Power Derating





# PACKAGE DIMENSIONS

TO-220 CASE 221A-09 **ISSUE AA** 



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	88.0
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

STYLE 1:

PIN 1. BASE

COLLECTOR 2.

EMITTER

COLLECTOR

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