DATA SHEET

TDA8920

2 × 50 W class-D power amplifier

Preliminary specification

File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

2 × 50 W class-D power amplifier

TDA8920

FEATURES

- High efficiency (90%)
- Operating voltage from ±15 V to ±30 V
- Very low quiescent current
- Low distortion
- Fixed gain of 30 dB
- High output power
- Output power limiter
- Good ripple rejection
- Usable as a mono amplifier in Bridge-Tied Load (BTL) or as a stereo Single-Ended (SE) amplifier
- Tracking possibility for oscillator frequency
- Differential audio inputs
- No switch-on or switch-off plops
- Short-circuit proof across the load
- Electrostatic discharge protection on all pins
- Thermally protected.

APPLICATIONS

- Television sets
- Home-sound systems
- Multimedia systems.

GENERAL DESCRIPTION

The TDA8920 is a high efficiency class-D audio power amplifier. It can be used in a mono Bridge-Tied Load (BTL) or in a stereo Single-Ended (SE) configuration. The device operates over a wide supply voltage range from ±15 V up to ±30 V and consumes a very low quiescent current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{DD}	operating supply voltage		±15	±25	±30	V
$I_{q(tot)}$	total quiescent current		–	50	60	mA
η	efficiency	P_o = 10 W	85	90	–	%
Stereo single-ended configuration						
P_o	output power	THD = 10%	tbf	35	–	W
$G_{v(cl)}$	closed loop voltage gain		29	30	31	dB
$|Z_i|$	input impedance		80	120	–	kΩ
$V_{n(o)}$	noise output voltage		–	100	–	μV
SVRR	supply voltage ripple rejection		60	–	–	dB
α_{cs}	channel separation		50	tbf	–	dB
Mono bridge-tied load configuration						
P_o	output power	THD = 10%	–	130	–	W
$G_{v(cl)}$	closed loop voltage gain		35	36	37	dB
$|Z_i|$	input impedance		40	60	–	kΩ
$V_{n(o)}$	noise output voltage		–	140	–	μV
SVRR	supply voltage ripple rejection		66	–	–	dB
$|\Delta V_O|$	DC output offset voltage		–	–	50	mV

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ORDERING INFORMATION

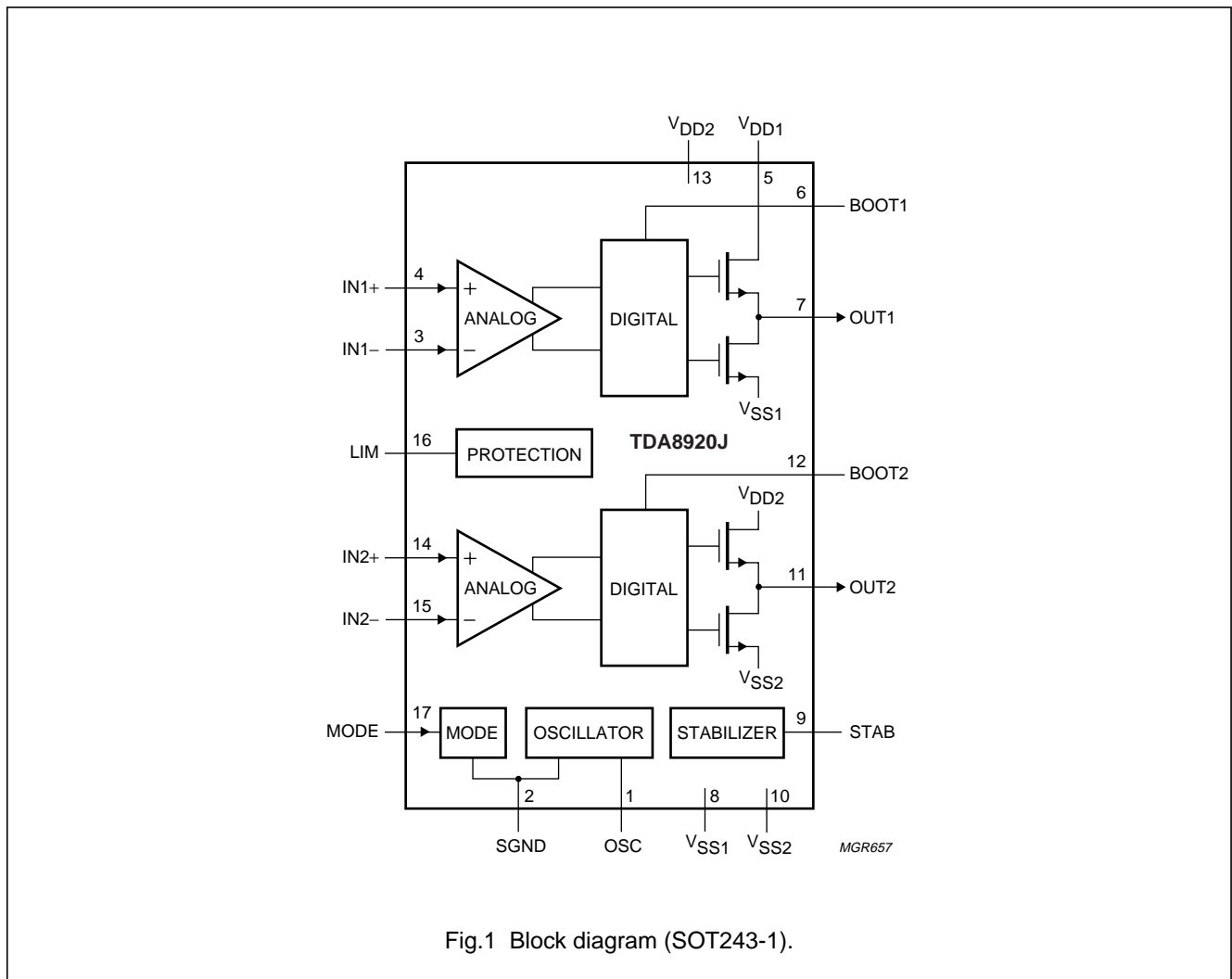| TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8920J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1
TDA8920TH	HSOP20	heatsink small outline package; 20 leads	SOT418-1

BLOCK DIAGRAM

Fig.1 Block diagram (SOT243-1).

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PINNING

SYMBOL	PIN	DESCRIPTION
OSC	1	oscillator frequency adjustment
SGND	2	signal ground (0 V)
IN1−	3	negative input channel 1
IN1+	4	positive input channel 1
V_{DD1}	5	positive supply voltage 1
BOOT1	6	bootstrapping capacitor 1
OUT1	7	output 1
V_{SS1}	8	negative supply voltage 1; note 1
STAB	9	internal stabilizer decoupling
V_{SS2}	10	negative supply voltage 2; note 1
OUT2	11	output 2
BOOT2	12	bootstrapping capacitor 2
V_{DD2}	13	positive supply voltage 2
IN2+	14	positive input channel 2
IN2−	15	negative input channel 2
LIM	16	current limiting adjustment
MODE	17	mode select input

Note

1. The case of the package is connected to pins 8 and 10 (V_{SS1} and V_{SS2}). Therefore no other voltage than V_{SS} should be connected to the case or the heatsink.
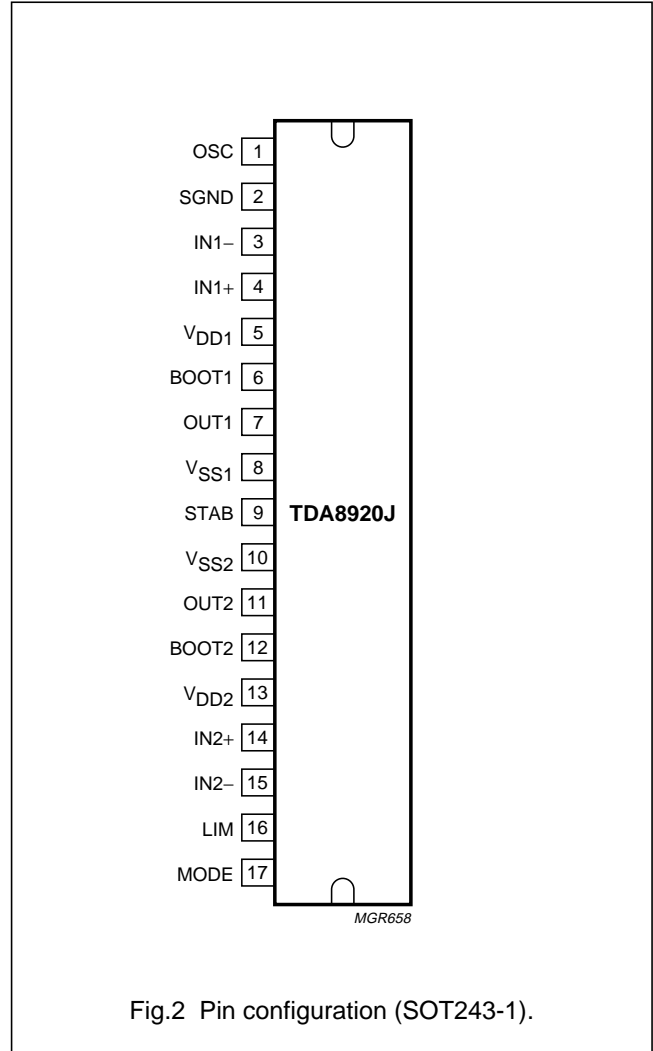

Fig.2 Pin configuration (SOT243-1).

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FUNCTIONAL DESCRIPTION

The TDA8920 is a multi purpose audio power amplifier in class-D technology. It contains two independent amplifiers with high output power, high efficiency (90%), low distortion and a low quiescent current. The amplifiers can be connected in the following configurations:

- Mono bridge-tied load amplifier
- Stereo single-ended amplifiers.

The amplifier can be switched in three operating modes with the mode select input:

- Standby mode, with a very low supply current (practically zero)
- Mute mode; the amplifiers are operational but the audio signal at the output is suppressed
- Operating mode (amplifier fully operational) with output signal.

  For suppressing plop noise the amplifier will remain automatically for approximately 500 ms in the mute mode before switching to operating mode. During this time the coupling capacitors at the input are fully charged. An example of a switching circuit for driving the mode select input is illustrated in Fig.3.

Pulse Width Modulation (PWM) frequency

The output signal of the amplifier is a PWM signal with a sample frequency of 500 kHz. The use of a second order LC filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC and pin SGND. With the resistor value given in the application diagram, the oscillating frequency is typical 500 kHz. The oscillator frequency can be calculated using:

$$f_{osc} = \frac{5.10^9}{R_{OSC}} [Hz]$$

If two or more devices are used in the same audio system it is advised to have both devices working on the same oscillation frequency. This can be realized by connecting all OSC pins together.

Current limiting

With an external resistor R_{LIM} connected between pin LIM and V_{SS} the maximum output current of the amplifiers can be set. If pin LIM is short-circuited to V_{SS}, then the maximum output current is limited to 7 A. The relationship between maximum output current and resistor value is given by:

$$I_{O(max)} = \frac{70.10^3}{\left(10.10^3 + R_{LIM}\right)} [A]$$

Protections

Protections are included to avoid the device being damaged at:

- Over-temperature $T_j > 150\ °C$
- Short-circuit of the loudspeaker terminals: when short-circuited the power dissipation is limited
- A maximum current limiter which limits the maximum output current to 7 A, or to the value set by R_{LIM}. During limiting the current is measured and when the current is higher than 7 A, the amplifier is switched off within 3 μs and every 20 ms the IC tries to restart. The dissipation will be low because of this low duty cycle.
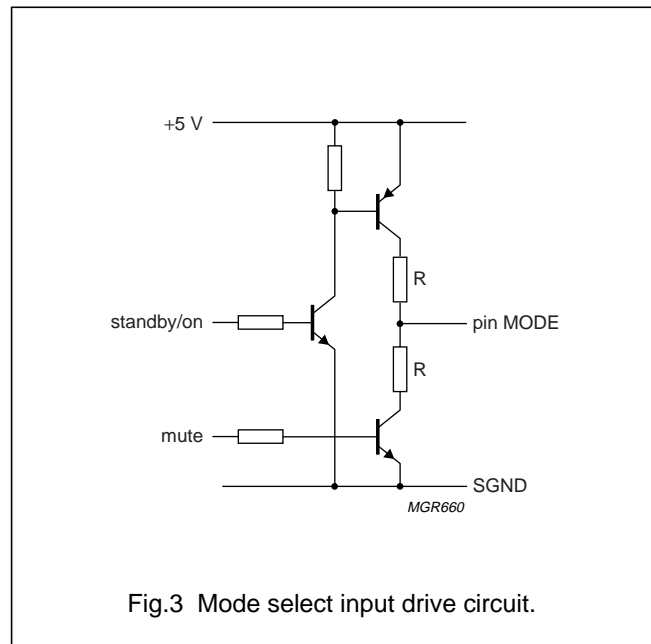- ESD protection (human body model: 3000 V and machine model: 300 V).

Fig.3 Mode select input drive circuit.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	±30	V
V_{ms}	mode select switch voltage	with respect to SGND	–	5.5	V
V_{sc}	short-circuit voltage of output pins		–	±30	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	7.5	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		10	K/W

QUALITY SPECIFICATION

Quality according to *"SNW-FQ-611-part E"*, if this type is used as an audio amplifier.

SWITCHING CHARACTERISTICS

V_{DD} = ±25 V; T_{amb} = 25 °C; measured in Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{osc}	oscillator frequency	400	500	600	kHz
$V_{OSC(p-p)}$	voltage at tracking point (peak-to-peak value)	–	1.75	–	V

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DC CHARACTERISTICS

$V_{DD} = \pm 25$ V; $T_{amb} = 25$ °C; measured in Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range	note 1	± 15	± 25	± 30	V
$I_{q(tot)}$	total quiescent current		–	50	60	mA
I_{stb}	standby current		–	0.2	50	µA
Amplifier outputs						
$|V_{OO}|$	output offset voltage	on and mute	–	–	50	mV
$|\Delta V_{OO}|$	delta output offset voltage	on $\leftrightarrow$ mute	–	–	30	mV
Mode select input; see Fig.4						
V_{ms}	input voltage range	note 2	0	–	5.5	V
I_{ms}	input current	$V_{ms} = 5.5$ V	–	–	tbf	µA
V_{th1+}	threshold voltage	standby $\rightarrow$ mute; note 2	–	–	2	V
V_{th1-}	threshold voltage	mute $\rightarrow$ standby; note 2	1	–	–	V
$V_{ms(hys1)}$	hysteresis $|(V_{th1+}) - (V_{th1-})|$		–	200	–	mV
V_{th2+}	threshold voltage	mute $\rightarrow$ on; note 2	–	–	4	V
V_{th2-}	threshold voltage	on $\rightarrow$ mute; note 2	3	–	–	V
$V_{ms(hys2)}$	hysteresis $|(V_{th2+}) - (V_{th2-})|$		–	200	–	mV

Notes

1. The circuit is DC adjusted at $V_{DD} = \pm 15$ V to ± 30 V.

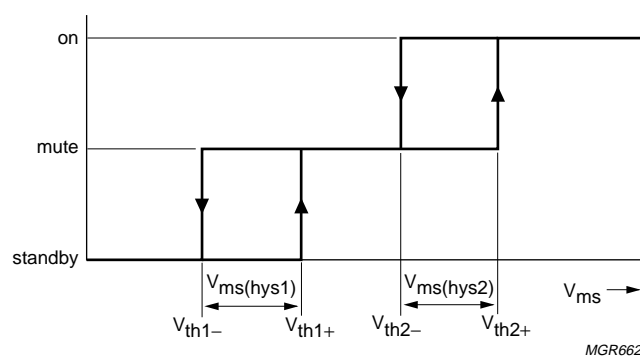2. Referenced to SGND (0 V).

Fig.4 Mode select transfer characteristic.

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AC CHARACTERISTICS

Stereo single-ended application

$V_{DD} = \pm25$ V; $R_L = 8$ Ω; $f_i = 1$ kHz; $T_{amb} = 25$ °C; measured in Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	tbf	30	–	W
		THD = 10%	tbf	35	–	W
		THD = 0.5%; $V_p = \pm30$ V	–	40	–	W
		THD = 10%; $V_p = \pm30$ V	–	50	–	W
THD	total harmonic distortion	$P_o = 1$ W; note 1				
		$f_i = 1$ kHz	–	0.1	0.15	%
		$f_i = 10$ kHz	–	0.2	–	%
$G_{v(cl)}$	closed loop voltage gain		29	30	31	dB
η	efficiency	$P_o = $ tbf W; $f_i = 1$ kHz; note 2	85	90	–	%
SVRR	supply voltage ripple rejection	on; note 3	–	60	–	dB
		on; note 4	tbf	tbf	–	dB
		mute; note 3	–	60	–	dB
		standby; note 3	–	80	–	dB
$\lvert Z_i\rvert$	input impedance		80	120		kΩ
$V_{n(o)}$	noise output voltage	on; note 5	–	100	200	μV
		on; note 6	–	tbf	–	μV
		mute; note 7	–	100	–	μV
α_{cs}	channel separation	note 8	50	tbf	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	1	dB
V_o	output signal	mute; note 9	–	–	500	μV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)} = 1$ V	–	65	–	dB

Notes

1. Total harmonic distortion is measured in a bandwidth of 22 Hz to 22 kHz, using an 11th-order low-pass filter. When distortion is measured using a lower order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band.

2. Output power measured across the loudspeaker load.

3. $V_{ripple} = V_{ripple(max)} = 2$ V (p-p); $f_i = 100$ Hz; $R_s = 0$ Ω.

4. $V_{ripple} = V_{ripple(max)} = 2$ V (p-p); $f_i = 1$ kHz; $R_s = 0$ Ω.

5. B = 22 Hz to 22 kHz; $R_s = 0$ Ω.

6. B = 22 Hz to 22 kHz; $R_s = 10$ kΩ.

7. B = 22 Hz to 22 kHz; independent of R_s.

8. $P_o = $ tbf W; $R_s = 0$ Ω.

9. $V_i = V_{i(max)} = 1$ V (RMS).

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Mono bridge-tied load application

$V_{DD} = \pm 25$ V; $R_L = 8$ Ω; $f_i = 1$ kHz; $T_{amb} = 25$ °C; measured in Fig.6; unless otherwise specified.

| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	tbf	100	–	W
		THD = 10%	tbf	130	–	W
		THD = 0.5%; $V_p = \pm 30$ V	–	150	–	W
		THD = 10%; $V_p = \pm 30$ V	–	190	–	W
THD	total harmonic distortion	$P_o = 1$ W; note 1				
		$f_i = 1$ kHz	–	0.1	0.15	%
		$f_i = 10$ kHz	–	0.2	–	%
$G_{v(cl)}$	closed loop voltage gain		35	36	37	dB
η	efficiency	P_o = tbf W; $f_i = 1$ kHz; note 2	tbf	tbf	–	%
SVRR	supply voltage ripple rejection	on; note 3	–	66	–	dB
		on; note 4	tbf	–	–	dB
		mute; note 3	–	66	–	dB
		standby; note 3	80	–	–	dB
$|Z_i|$	input impedance		40	60	–	kΩ
$V_{n(o)}$	noise output voltage	on; note 5	–	140	280	μV
		on; note 6	–	tbf	–	μV
		mute; note 7	–	140	–	μV
V_o	output signal	mute; note 8	–	–	tbf	mV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)} = 1$ V	–	65	–	dB

Notes

1. Total harmonic distortion is measured in a bandwidth of 22 Hz to 22 kHz, using an 11th-order low-pass filter. When distortion is measured using a lower order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band.

2. Output power measured across the loudspeaker load.

3. $V_{ripple} = V_{ripple(max)} = 2$ V (p-p); $f_i = 100$ Hz; $R_s = 0$ Ω.

4. $V_{ripple} = V_{ripple(max)} = 2$ V (p-p); $f_i = 1$ kHz; $R_s = 0$ Ω.

5. B = 22 Hz to 22 kHz; $R_s = 0$ Ω.

6. B = 22 Hz to 22 kHz; $R_s = 10$ kΩ.

7. B = 22 Hz to 22 kHz; independent of R_s.

8. $V_i = V_{i(max)} = 1$ V (RMS).

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APPLICATION AND TEST INFORMATION
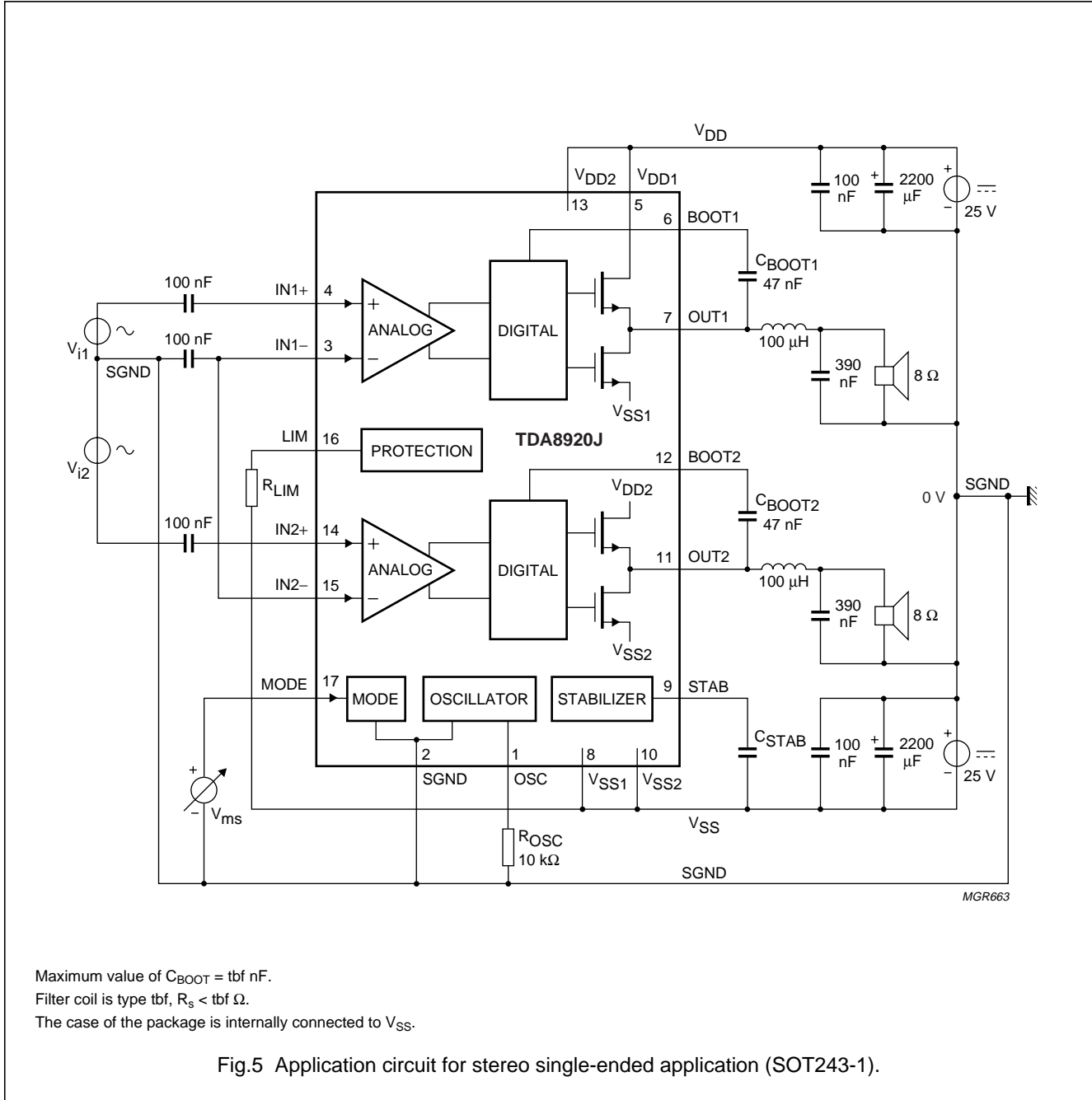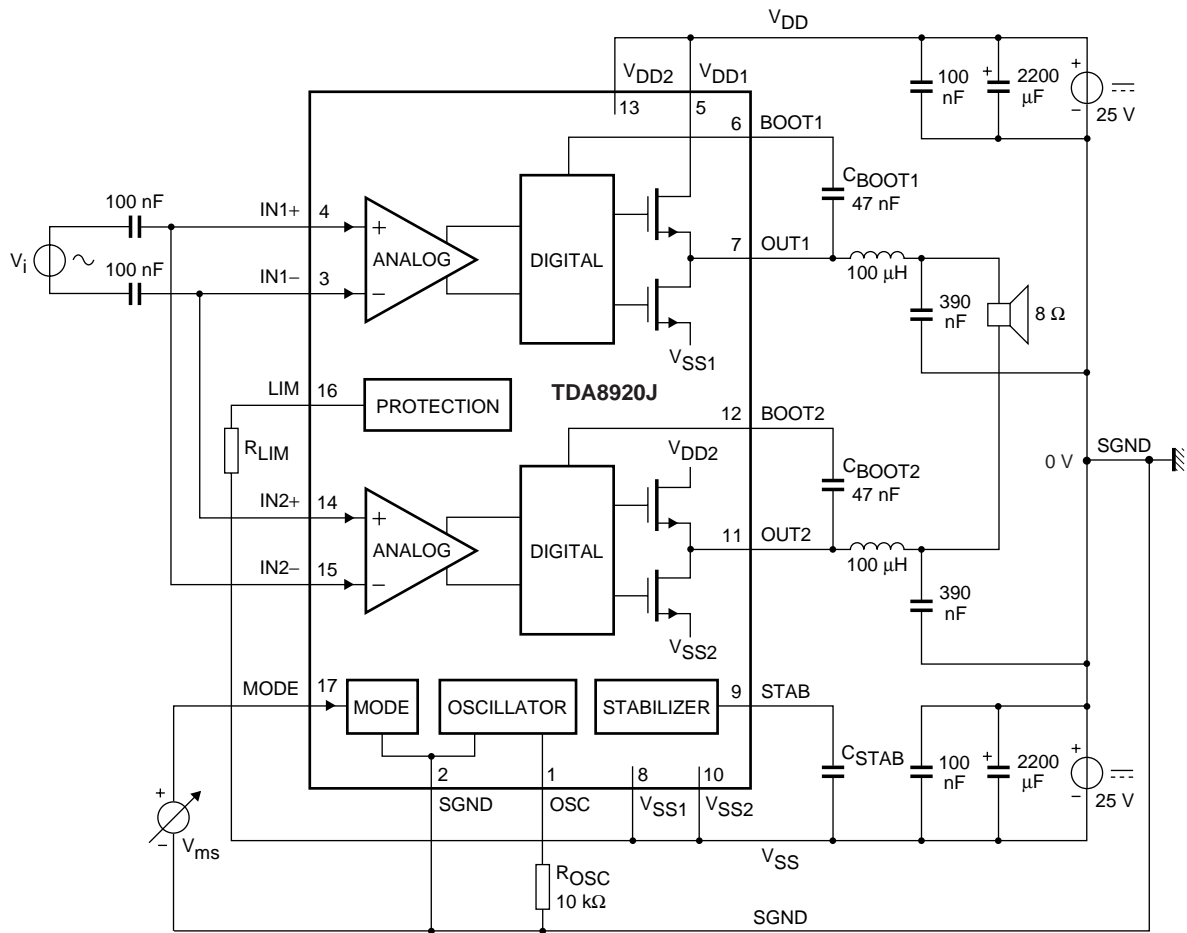
Maximum value of C_{BOOT} = tbf nF.

Filter coil is type tbf, R_s < tbf Ω.

The case of the package is internally connected to V_{SS}.

Fig.5 Application circuit for stereo single-ended application (SOT243-1).

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Maximum value of C_{BOOT} = tbf nF.

Filter coil is type tbf, R_s < tbf Ω.

The case of the package is internally connected to V_{SS}.

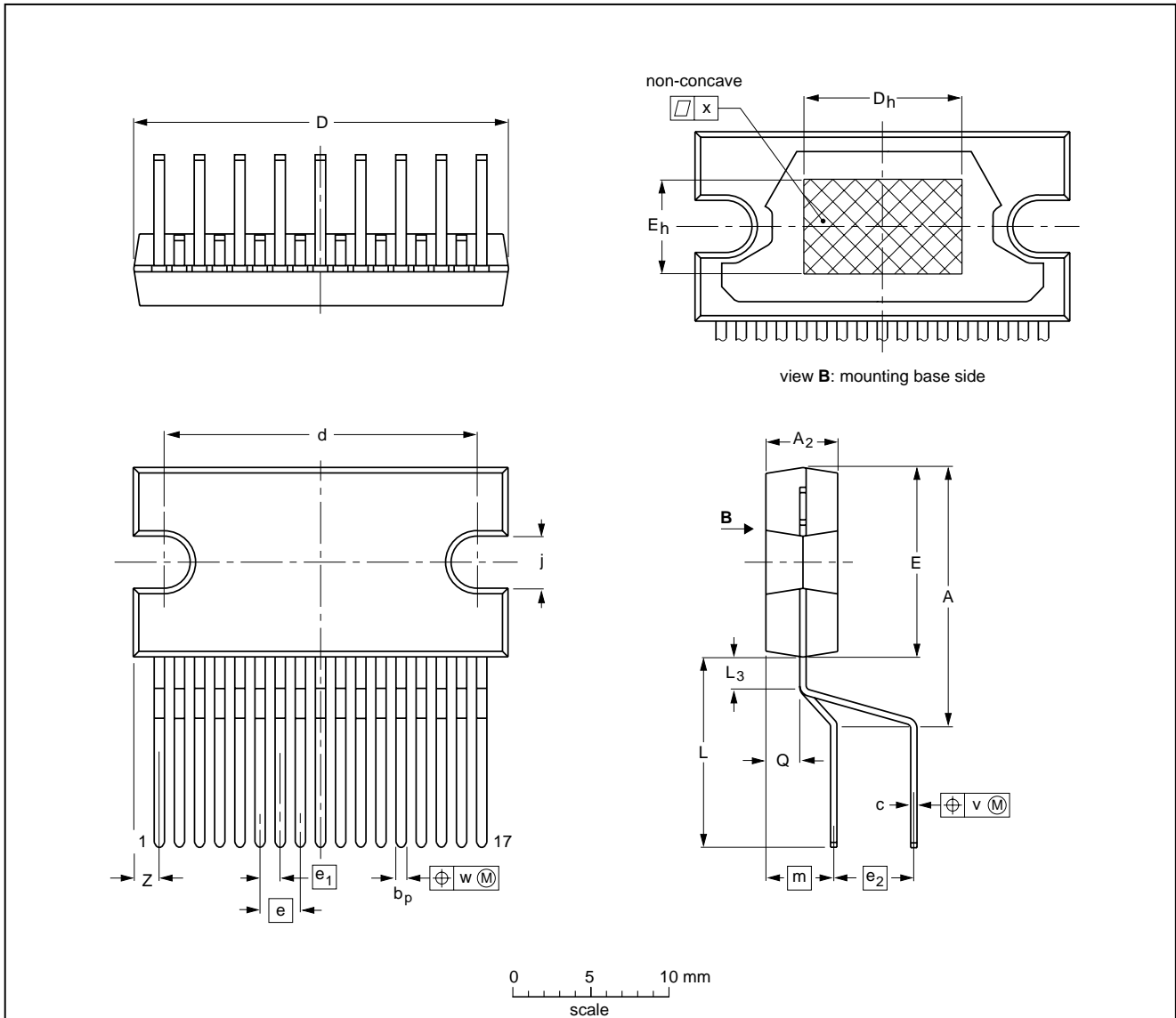Fig.6 Application circuit for mono bridge-tied load application (SOT243-1).

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PACKAGE OUTLINES

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1

non-concave

D_h

view **B**: mounting base side

0   5   10 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
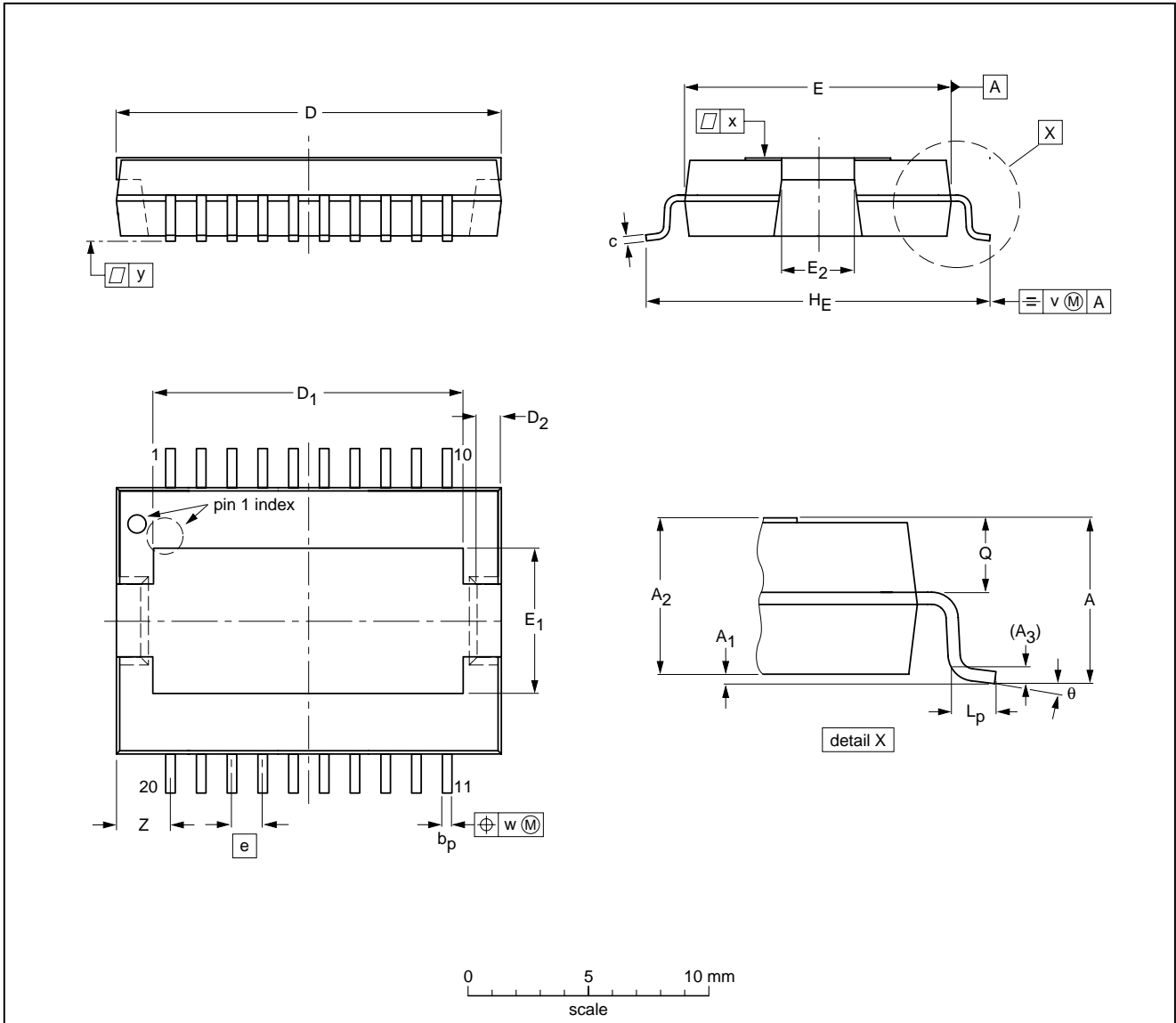
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~95-03-11~~ 97-12-16

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HSOP20: heatsink small outline package; 20 leads

SOT418-1


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0        5        10 mm
scale
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DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	D₁	D₂	E[1]	E₁	E₂	e	HE	Lₚ	Q	v	w	x	y	Z	θ
mm	3.7	0.3 0.1	3.5 3.2	0.35	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.1	2.5 2.0	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-1						~~97-11-03~~ 98-02-25

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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	**REFLOW**[1]	**DIPPING**
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[2]	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[3]	suitable	–
	PLCC[4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[4][5]	suitable	–
	SSOP, TSSOP, VSO	not recommended[6]	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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