

Thyristors

BT151F series

GENERAL DESCRIPTION

Passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

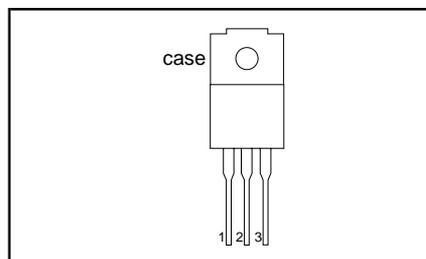
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|-----------------------|--------------------------------------|-------------------|-------------------|-------------------|------|
| V_{DRM} , V_{RRM} | Repetitive peak off-state voltages | 500 500 | 650 650 | 800 800 | V |
| $I_{T(AV)}$ | Average on-state current | 5.7 | 5.7 | 5.7 | A |
| $I_{T(RMS)}$ | RMS on-state current | 9 | 9 | 9 | A |
| I_{TSM} | Non-repetitive peak on-state current | 100 | 100 | 100 | A |

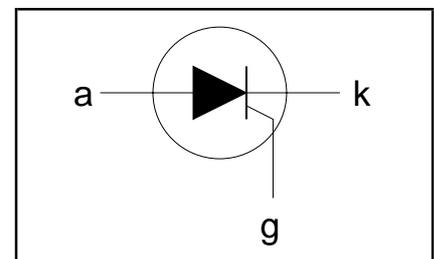
PINNING - SOT186

| PIN | DESCRIPTION |
|------|-------------|
| 1 | cathode |
| 2 | anode |
| 3 | gate |
| case | isolated |

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|-----------------------|--------------------------------------|---|------|--------------------------|--------------------------|-------------|------------------|
| | | | | -500 500 ¹ | -650 650 ¹ | -800 800 | |
| V_{DRM} , V_{RRM} | Repetitive peak off-state voltages | | - | -500 500 ¹ | -650 650 ¹ | -800 800 | V |
| $I_{T(AV)}$ | Average on-state current | half sine wave; $T_{hs} \leq 87^\circ\text{C}$ all conduction angles | - | 5.7 | | | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_j = 125^\circ\text{C}$ prior to surge; with reapplied $V_{DRM(max)}$ | - | 9 | | | A |
| I_{TSM} | Non-repetitive peak on-state current | $t = 10\text{ ms}$ | - | 100 | | | A |
| | | $t = 8.3\text{ ms}$ | - | 110 | | | A |
| | | $t = 10\text{ ms}$ | - | 50 | | | A ² s |
| I^2t | I^2t for fusing | $I_{TM} = 20\text{ A}$; $I_G = 50\text{ mA}$; $dI_G/dt = 50\text{ mA}/\mu\text{s}$ | - | 50 | | | A μs |
| I_{GM} | Peak gate current | | - | 2 | | | A |
| V_{GM} | Peak gate voltage | | - | 5 | | | V |
| V_{RGM} | Peak reverse gate voltage | | - | 5 | | | V |
| P_{GM} | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| T_{stg} | Storage temperature | | -40 | 150 | | | $^\circ\text{C}$ |
| T_j | Operating junction temperature | | - | 125 | | | $^\circ\text{C}$ |

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

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ISOLATION LIMITING VALUE & CHARACTERISTIC $T_{hs} = 25\text{ °C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------|---|--------------------------------------|------|------|------|------|
| V_{isol} | Repetitive peak voltage from all three terminals to external heatsink | R.H. \leq 65% ; clean and dustfree | - | | 1500 | V |
| C_{isol} | Capacitance from T2 to external heatsink | $f = 1\text{ MHz}$ | - | 12 | - | pF |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|---|--|------|------|------|------|
| $R_{th\ j-hs}$ | Thermal resistance junction to heatsink | with heatsink compound | - | - | 4.5 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | without heatsink compound in free air | - | 55 | 6.5 | K/W |

STATIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------|---------------------------|---|------|------|------|------|
| I_{GT} | Gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$ | - | 2 | 15 | mA |
| I_L | Latching current | $V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$ | - | 10 | 40 | mA |
| I_H | Holding current | $V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$ | - | 7 | 20 | mA |
| V_T | On-state voltage | $I_T = 23\text{ A}$ | - | 1.4 | 1.75 | V |
| V_{GT} | Gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$ | - | 0.6 | 1.5 | V |
| I_D, I_R | Off-state leakage current | $V_D = V_{DRM(max)}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$ | 0.25 | 0.4 | - | V |
| | | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j = 125\text{ °C}$ | - | 0.1 | 0.5 | mA |

DYNAMIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|--|--|------|------|------|------------|
| dV_D/dt | Critical rate of rise of off-state voltage | $V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\text{ °C}$; exponential waveform | | | | |
| | | Gate open circuit $R_{GK} = 100\ \Omega$ | 50 | 130 | - | V/ μ s |
| t_{gt} | Gate controlled turn-on time | $I_{TM} = 40\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1\text{ A}$; $di_G/dt = 5\text{ A}/\mu$ s | 200 | 1000 | - | V/ μ s |
| t_q | Circuit commutated turn-off time | $V_D = 67\% V_{DRM(max)}$; $T_j = 125\text{ °C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $di_{TM}/dt = 30\text{ A}/\mu$ s; $dV_D/dt = 50\text{ V}/\mu$ s; $R_{GK} = 100\ \Omega$ | - | 70 | - | μ s |

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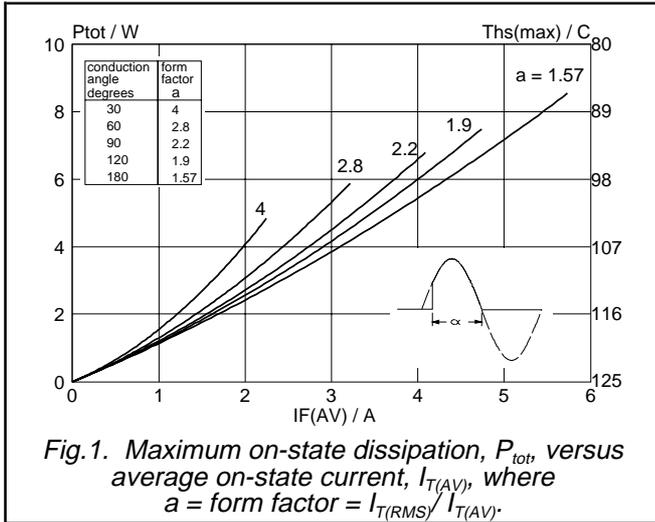


Fig. 1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$.

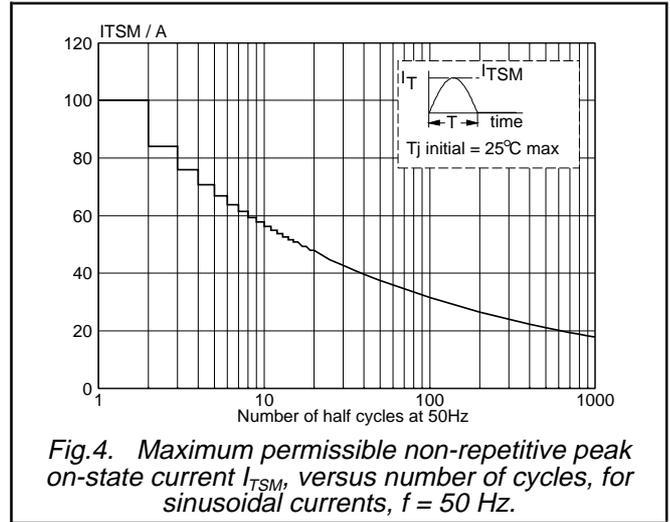


Fig. 4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 \text{ Hz}$.

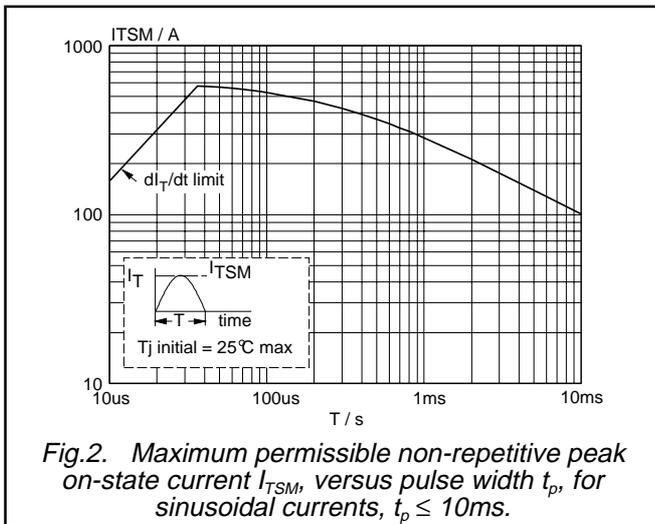


Fig. 2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10 \text{ ms}$.

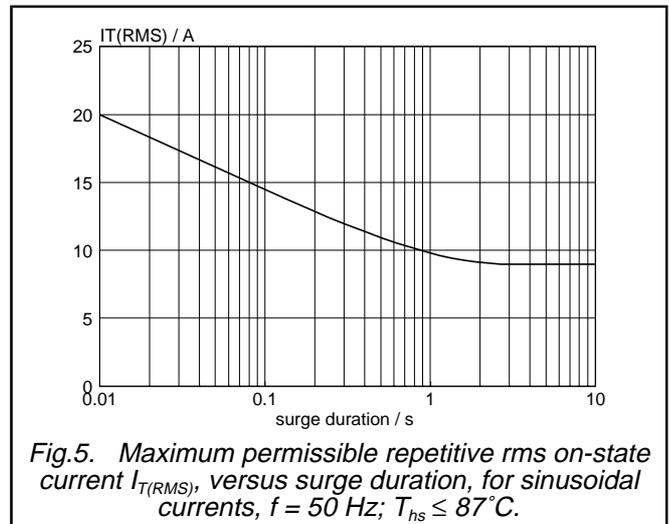


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 \text{ Hz}$; $T_{hs} \leq 87^\circ\text{C}$.

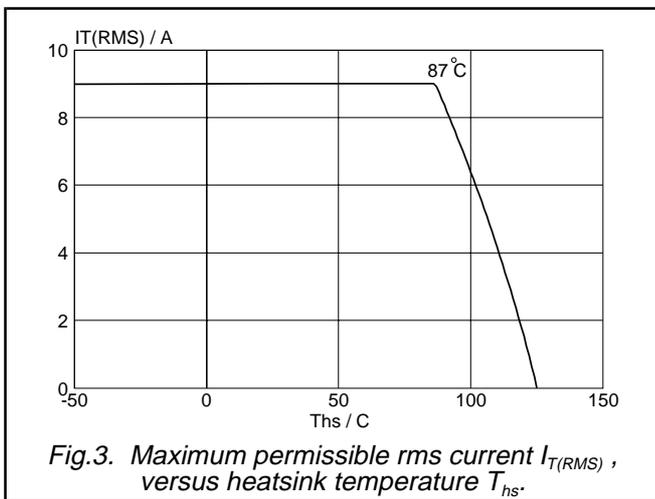


Fig. 3. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs} .

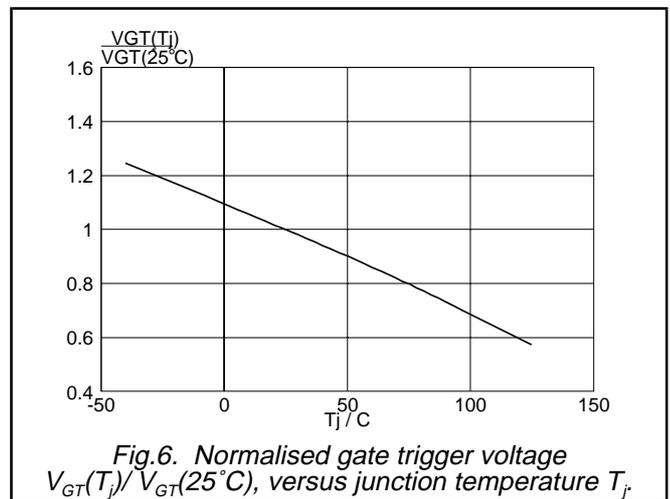
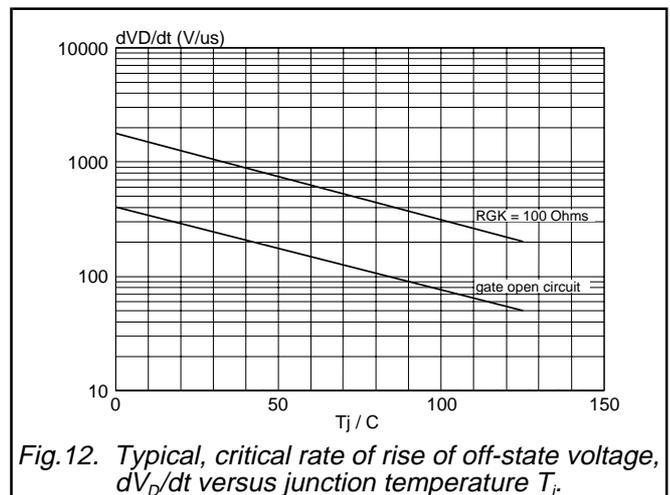
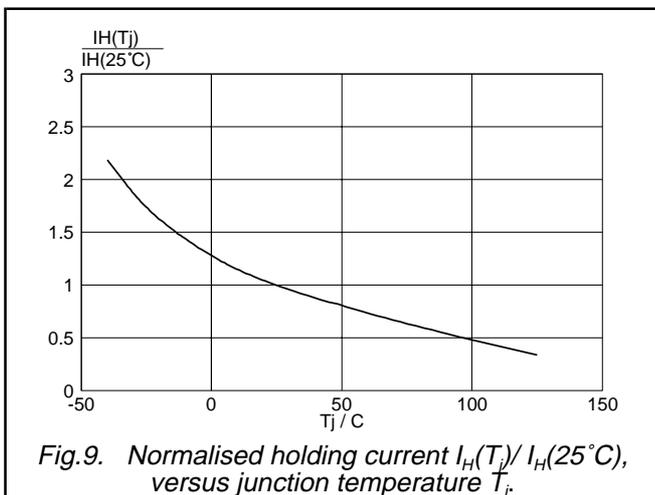
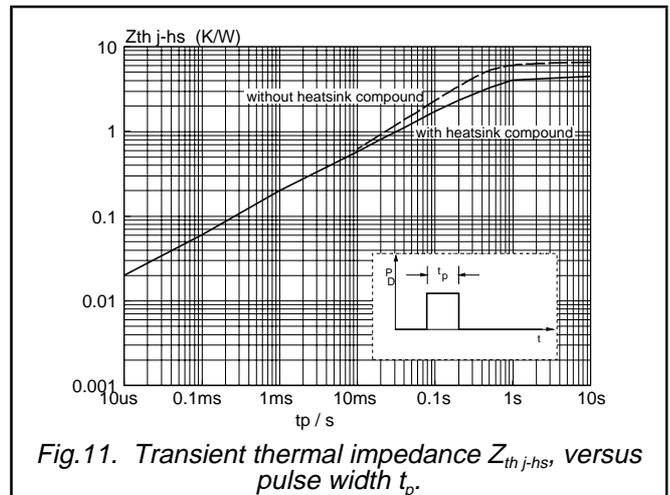
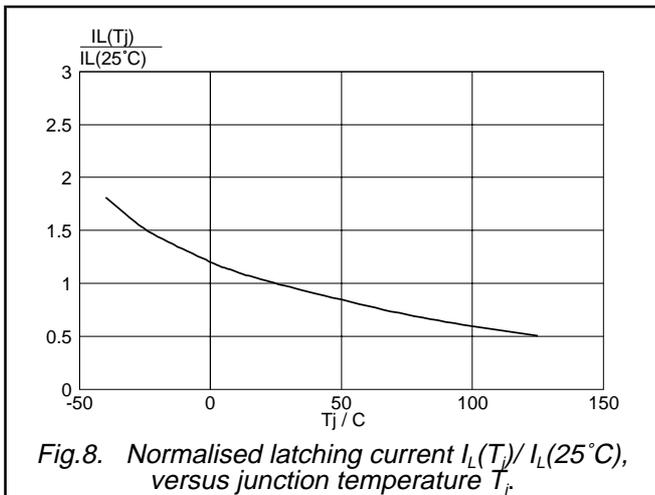
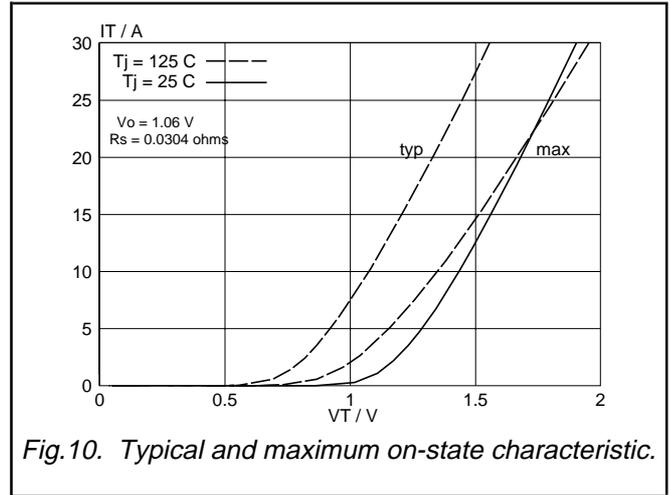
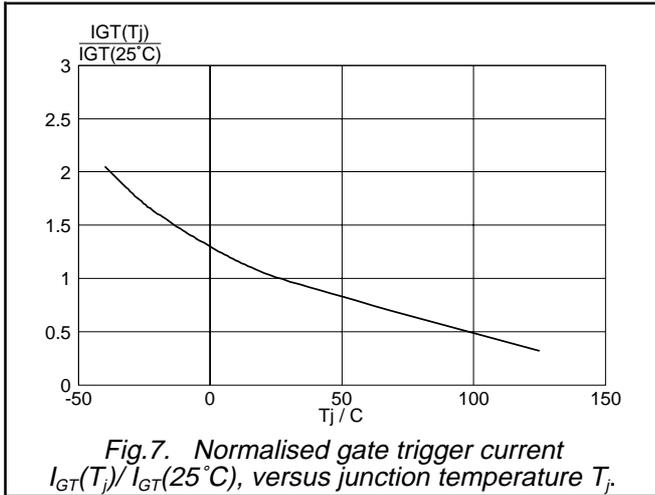


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

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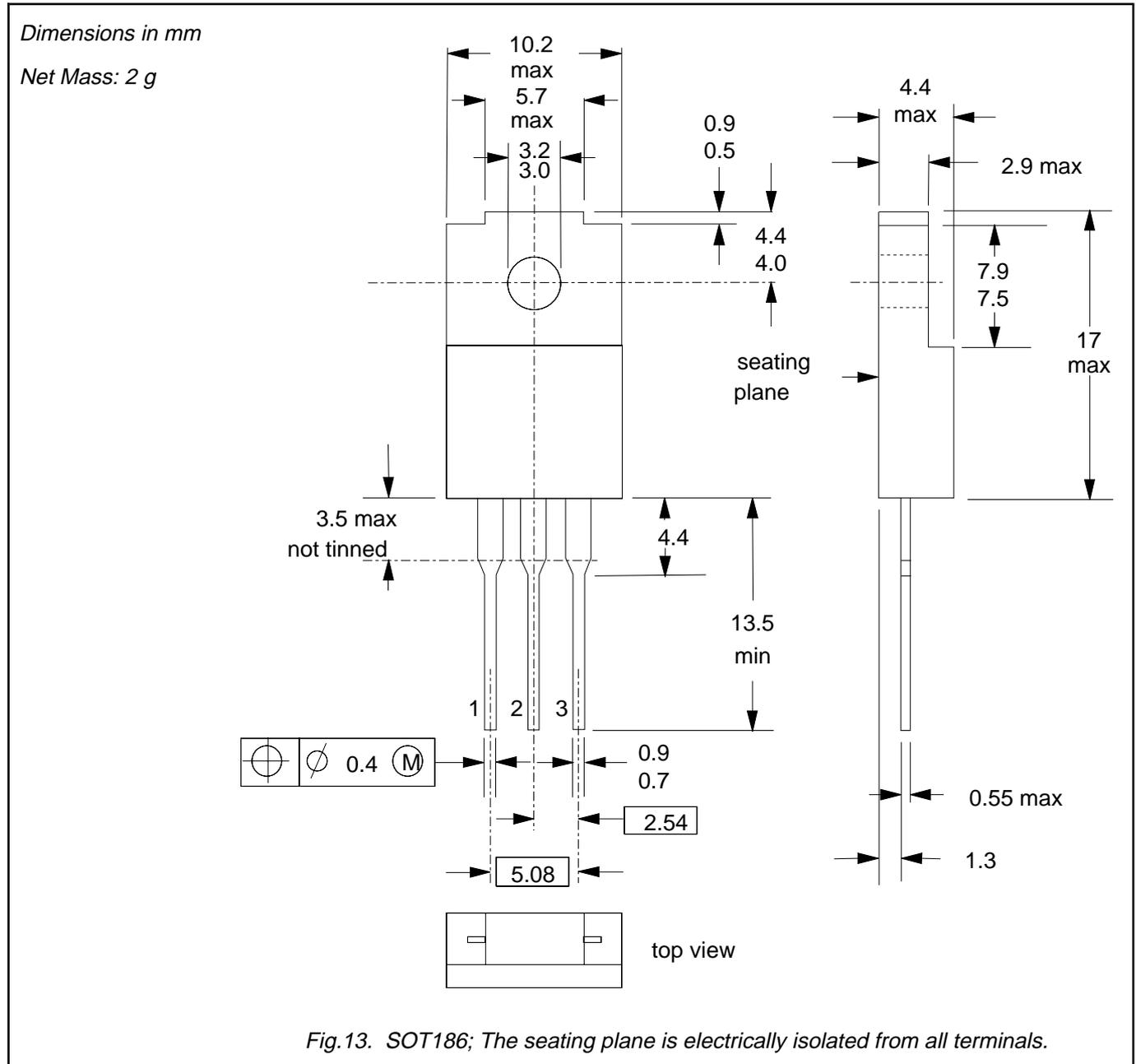
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MECHANICAL DATA



Notes

1. Refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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