



DAC714

16-Bit DIGITAL-TO-ANALOG CONVERTER With Serial Data Interface

FEATURES:

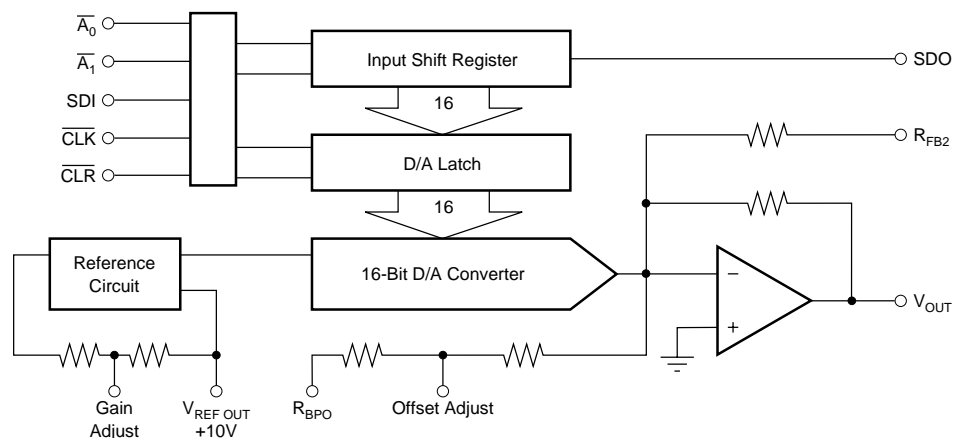
- SERIAL DIGITAL INTERFACE
- VOLTAGE OUTPUT: $\pm 10\text{V}$, $\pm 5\text{V}$, 0 to $+10\text{V}$
- ± 1 LSB INTEGRAL LINEARITY
- 16-BIT MONOTONIC OVER TEMPERATURE
- PRECISION INTERNAL REFERENCE
- LOW NOISE: $120\text{nV}/\sqrt{\text{Hz}}$ Including Reference
- 16-LEAD PLASTIC AND CERAMIC SKINNY DIP AND PLASTIC SOIC PACKAGES

DESCRIPTION

The DAC714 is a complete monolithic digital-to-analog converter including a $+10\text{V}$ temperature compensated reference, current-to-voltage amplifier, a high-speed synchronous serial interface, a serial output which allows cascading multiple converters, and an asynchronous clear function which immediately sets the output voltage to midscale.

The output voltage range is $\pm 10\text{V}$, $\pm 5\text{V}$, or 0 to $+10\text{V}$ while operating from $\pm 12\text{V}$ or $\pm 15\text{V}$ supplies. The gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short circuit to ground.

The 16-pin DAC714 is available in a plastic 0.3" DIP, ceramic 0.3" Cerdip, and wide-body plastic SOIC package. The DAC714P, U, HB, and HC are specified over the -40°C to $+85^\circ\text{C}$ temperature range while the DAC714HL is specified over the 0°C to $+70^\circ\text{C}$ range.



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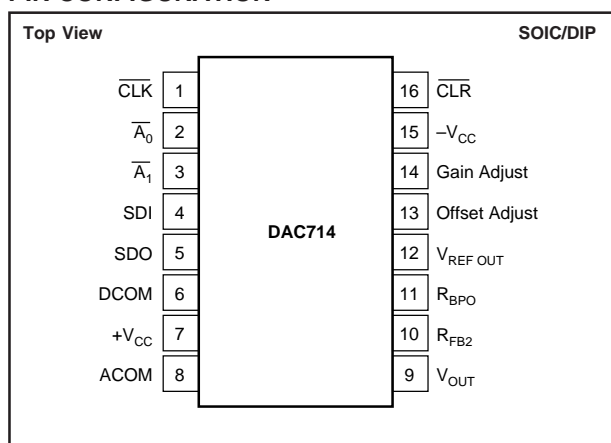
SPECIFICATIONS

At $T_A = +25^{\circ}\text{C}$, $+V_{CC} = +12\text{V}$ and $+15\text{V}$, $-V_{CC} = -12\text{V}$, and -15V , unless otherwise noted.

| | DAC714P, U | | | DAC714HB | | | DAC714HC | | | DAC714HL | | | |
|---|------------|------------|------------------------|----------|------------|------------------------|----------|------------|------------------------|----------|------------|------------------------|--------------------------|
| PARAMETER | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| TRANSFER CHARACTERISTICS | | | | | | | | | | | | | |
| ACCURACY | | | | | | | | | | | | | |
| Linearity Error | | | ±4 | | | ±2 | | | ±1 | | | ±1 | LSB |
| T _{MIN} to T _{MAX} | | | ±8 | | | ±4 | | | ±2 | | | ±2 | LSB |
| Differential Linearity Error | | | ±4 | | | ±2 | | | ±1 | | | ±1 | LSB |
| T _{MIN} to T _{MAX} | | | ±8 | | | ±4 | | | ±2 | | | ±1 | LSB |
| Monotonicity | 14 | | | 15 | | | 16 | | | 16 | | | Bits |
| Monotonicity Over Spec Temp Range | 13 | | | 14 | | | 15 | | | 16 | | | Bits |
| Gain Error ⁽³⁾ | | | ±0.1 | | | ±0.1 | | | ±0.1 | | | ±0.1 | % |
| T _{MIN} to T _{MAX} | | | ±0.25 | | | ±0.25 | | | ±0.25 | | | ±0.25 | % |
| Unipolar/Bipolar Zero Error ⁽³⁾ | | | ±0.1 | | | ±0.1 | | | ±0.1 | | | ±0.1 | % of FSR ⁽²⁾ |
| T _{MIN} to T _{MAX} | | | ±0.2 | | | ±0.2 | | | ±0.2 | | | ±0.2 | % of FSR |
| Power Supply Sensitivity of Gain | | | ±0.003 | | | ±0.003 | | | ±0.003 | | | ±0.003 | %FSR/%V _{CC} |
| | | | ±30 | | | ±30 | | | ±30 | | | ±30 | ppm FSR/%V _{CC} |
| DYNAMIC PERFORMANCE | | | | | | | | | | | | | |
| Settling Time | | | | | | | | | | | | | |
| (to ±0.003%FSR, 5kΩ 500pF Load) ⁽⁴⁾ | | | | | | | | | | | | | |
| 20V Output Step | | 6 | 10 | | 6 | 10 | | 6 | 10 | | 6 | 10 | μs |
| 1LSB Output Step ⁽⁵⁾ | | 4 | | | 4 | | | 4 | | | 4 | | μs |
| Output Slew Rate | | 10 | | | 10 | | | 10 | | | 10 | | V/μs |
| Total Harmonic Distortion | | | | | | | | | | | | | |
| 0dB, 1001Hz, f _S = 100kHz | | 0.005 | | | 0.005 | | | 0.005 | | | 0.005 | | % |
| −20dB, 1001Hz, f _S = 100kHz | | 0.03 | | | 0.03 | | | 0.03 | | | 0.03 | | % |
| −60dB, 1001Hz, f _S = 100kHz | | 3.0 | | | 3.0 | | | 3.0 | | | 3.0 | | % |
| SINAD: 1001Hz, f _S = 100kHz | | 87 | | | 87 | | | 87 | | | 87 | | dB |
| Digital Feedthrough ⁽⁵⁾ | | 2 | | | 2 | | | 2 | | | 2 | | nV−s |
| Digital-to-Analog Glitch Impulse ⁽⁵⁾ | | 15 | | | 15 | | | 15 | | | 15 | | nV−s |
| Output Noise Voltage (includes reference) | | 120 | | | 120 | | | 120 | | | 120 | | nV/√Hz |
| ANALOG OUTPUT | | | | | | | | | | | | | |
| Output Voltage Range | | | | | | | | | | | | | |
| +V _{CC} , −V _{CC} = ±11.4V | ±10 | | | ±10 | | | ±10 | | | ±10 | | | V |
| Output Current | ±5 | | | ±5 | | | ±5 | | | ±5 | | | mA |
| Output Impedance | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | Ω |
| Short Circuit to ACOM Duration | | Indefinite | | | Indefinite | | | Indefinite | | | Indefinite | | |
| REFERENCE VOLTAGE | | | | | | | | | | | | | |
| Voltage | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | +9.975 | +10.000 | +10.025 | V |
| T _{MIN} to T _{MAX} | +9.960 | | +10.040 | +9.960 | | +10.040 | +9.960 | | +10.040 | +9.960 | | +10.040 | V |
| Output Resistance | | 1 | | | 1 | | | 1 | | | 1 | | Ω |
| Source Current | 2 | | | 2 | | | 2 | | | 2 | | | mA |
| Short Circuit to ACOM Duration | | Indefinite | | | Indefinite | | | Indefinite | | | Indefinite | | |
| INTERFACE | | | | | | | | | | | | | |
| RESOLUTION | | | | | | | | | | | | | |
| DIGITAL INPUTS | | 16 | | | 16 | | | 16 | | | 16 | | Bits |
| Serial Data Input Code | | | | | | | | | | | | | |
| Logic Levels ⁽¹⁾ | | | | | | | | | | | | | |
| V _{IH} | +2.0 | | (V _{CC} −1.4) | +2.0 | | (V _{CC} −1.4) | +2.0 | | (V _{CC} −1.4) | +2.0 | | (V _{CC} −1.4) | V |
| V _{IL} | 0 | | +0.8 | 0 | | +0.8 | 0 | | +0.8 | 0 | | +0.8 | V |
| I _{IH} (V _I = +2.7V) | | | ±10 | | | ±10 | | | ±10 | | | ±10 | μA |
| I _{IL} (V _I = +0.4V) | | | ±10 | | | ±10 | | | ±10 | | | ±10 | μA |
| DIGITAL OUTPUT | | | | | | | | | | | | | |
| Serial Data | | | | | | | | | | | | | |
| V _{OL} (I _{SINK} = 1.6mA) | 0 | | +0.4 | 0 | | +0.4 | 0 | | +0.4 | 0 | | +0.4 | V |
| V _{OH} (I _{SOURCE} = 500μA), T _{MIN} to T _{MAX} | +2.4 | | +5 | +2.4 | | +5 | +2.4 | | +5 | +2.4 | | +5 | V |
| POWER SUPPLY REQUIREMENTS | | | | | | | | | | | | | |
| Voltage | | | | | | | | | | | | | |
| +V _{CC} | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | +11.4 | +15 | +16.5 | V |
| −V _{CC} | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | −11.4 | −15 | −16.5 | V |
| Current (No Load, ±15V Supplies) ⁽⁶⁾ | | | | | | | | | | | | | |
| +V _{CC} | | 13 | 16 | | 13 | 16 | | 13 | 16 | | 13 | 16 | mA |
| −V _{CC} | | 22 | 26 | | 22 | 26 | | 22 | 26 | | 22 | 26 | mA |
| Power Dissipation ⁽⁷⁾ | | | 625 | | | 625 | | | 625 | | | 625 | mW |
| TEMPERATURE RANGES | | | | | | | | | | | | | |
| Specification | | | | | | | | | | | | | |
| All Grades | −40 | | +85 | −40 | | +85 | −40 | | +85 | 0 | | +70 | °C |
| Storage | −60 | | +150 | −60 | | +150 | −60 | | +150 | −60 | | +150 | °C |
| Thermal Coefficient, θ _{JA} | | 75 | | | 75 | | | 75 | | | 75 | | °C/W |

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for $\pm 10\text{V}$ output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3 σ limit. Not 100% tested for this parameter. (5) For the worst-case Binary Two's Complement code changes: FFFF_H to 0000_H and 0000_H to FFFF_H. (6) During power supply turn on, the transient supply current may approach 3x the maximum quiescent specification. (7) Typical (i.e. rated) supply voltages times maximum currents.

PIN CONFIGURATION



PIN DESCRIPTIONS

| PIN | LABEL | DESCRIPTION |
|-----|----------------------|--|
| 1 | CLK | Serial Data Clock |
| 2 | A ₀ | Enable for Input Register (Active Low) |
| 3 | A ₁ | Enable for D/A Latch (Active Low) |
| 4 | SDI | Serial Data Input |
| 5 | SDO | Serial Data Output |
| 6 | DCOM | Digital Ground |
| 7 | +V _{CC} | Positive Power Supply |
| 8 | ACOM | Analog Ground |
| 9 | V _{OUT} | D/A Output |
| 10 | R _{FB2} | ±10V Range Feedback Output |
| 11 | R _{BPO} | Bipolar Offset |
| 12 | V _{REF OUT} | Voltage Reference Output |
| 13 | Offset Adjust | Offset Adjust |
| 14 | Gain Adjust | Gain Adjust |
| 15 | -V _{CC} | Negative Power Supply |
| 16 | CLR | Clear |



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|---------------------------------|
| +V _{CC} to Common | 0V to +17V |
| -V _{CC} to Common | 0V to -17V |
| +V _{CC} to -V _{CC} | 34V |
| ACOM to DCOM | ±0.5V |
| Digital Inputs to Common | -1V to (V _{CC} - 0.7V) |
| External Voltage Applied to BPO and Range Resistors | ±V _{CC} |
| V _{REF OUT} | Indefinite Short to Common |
| V _{OUT} | Indefinite Short to Common |
| SDO | Indefinite Short to Common |
| Power Dissipation | 750mW |
| Storage Temperature | -60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

| PRODUCT | PACKAGE | LINEARITY ERROR max at +25°C | TEMPERATURE RANGE |
|----------|--------------|---------------------------------|----------------------|
| DAC714P | Plastic DIP | ±4 LSB | -40°C to +85°C |
| DAC714U | Plastic SOIC | ±4 LSB | -40°C to +85°C |
| DAC714HB | Ceramic DIP | ±2 LSB | -40°C to +85°C |
| DAC714HC | Ceramic DIP | ±1 LSB | -40°C to +85°C |
| DAC714HL | Ceramic DIP | ±1 LSB | 0°C to +70°C |

PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ |
|---------|--------------|--|
| DAC714P | Plastic DIP | 180 |
| DAC714U | Plastic SOIC | 211 |
| DAC714H | Ceramic DIP | 129 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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TIMING SPECIFICATIONS

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{CC} = +12\text{V}$ or $+15\text{V}$, $-V_{CC} = -12\text{V}$ or -15V .

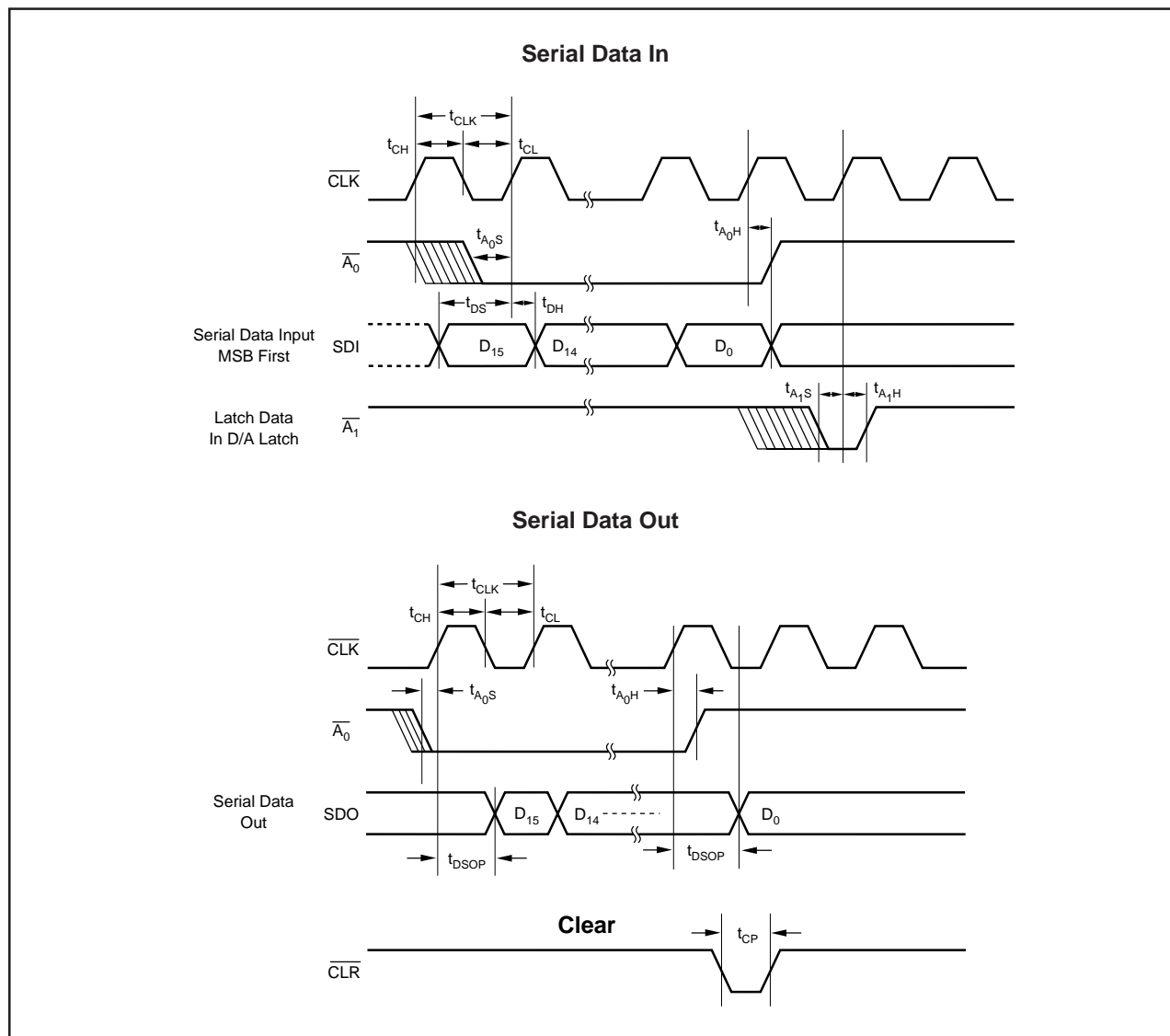
| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|------------|---------------------------------|-----|-----|-------|
| t_{CLK} | Data Clock Period | 100 | | ns |
| t_{CL} | Clock LOW | 50 | | ns |
| t_{CH} | Clock HIGH | 50 | | ns |
| t_{A0S} | Setup Time for $\overline{A_0}$ | 50 | | ns |
| t_{A1S} | Setup Time for $\overline{A_1}$ | 50 | | ns |
| t_{A0H} | Hold Time for $\overline{A_0}$ | 0 | | ns |
| t_{A1H} | Hold Time for $\overline{A_1}$ | 0 | | ns |
| t_{DS} | Setup Time for DATA | 50 | | ns |
| t_{DH} | Hold Time for DATA | 10 | | ns |
| t_{DSOP} | Output Propagation Delay | | 140 | ns |
| t_{CP} | Clear Pulsewidth | 200 | | ns |

TRUTH TABLE

| $\overline{A_0}$ | $\overline{A_1}$ | \overline{CLK} | \overline{CLR} | DESCRIPTION |
|------------------|------------------|---------------------------------|------------------|-----------------------------------|
| 0 | 1 | $1 \rightarrow 0 \rightarrow 1$ | 1 | Shift Serial Data into SDI |
| 1 | 0 | $1 \rightarrow 0 \rightarrow 1$ | 1 | Load D/A Latch |
| 1 | 1 | $1 \rightarrow 0 \rightarrow 1$ | 1 | No Change |
| 0 | 0 | $1 \rightarrow 0 \rightarrow 1$ | 1 | Two Wire Operation ⁽¹⁾ |
| X | X | 1 | 1 | No Change |
| X | X | X | 0 | Reset D/A Latch |

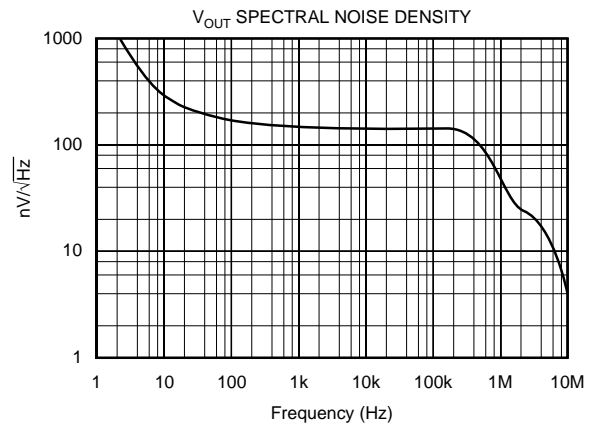
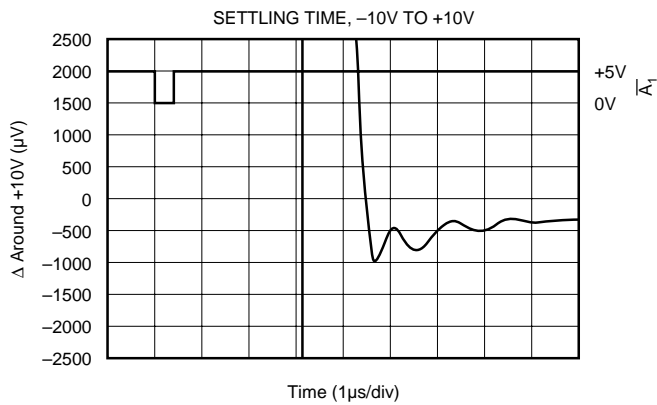
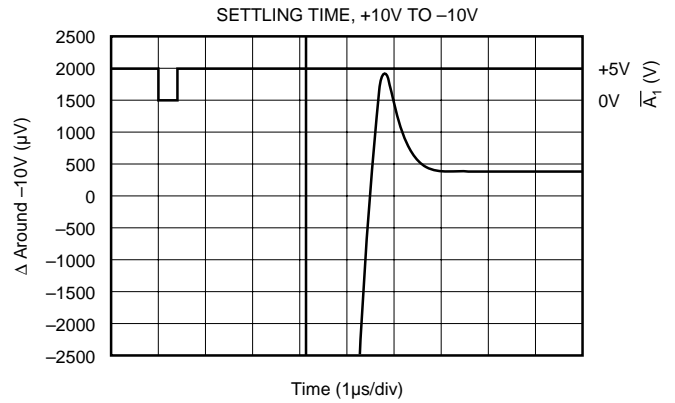
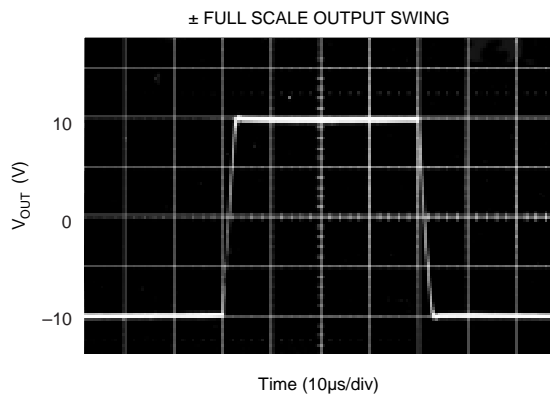
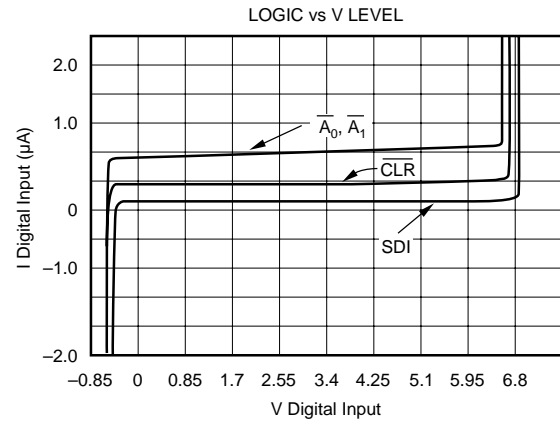
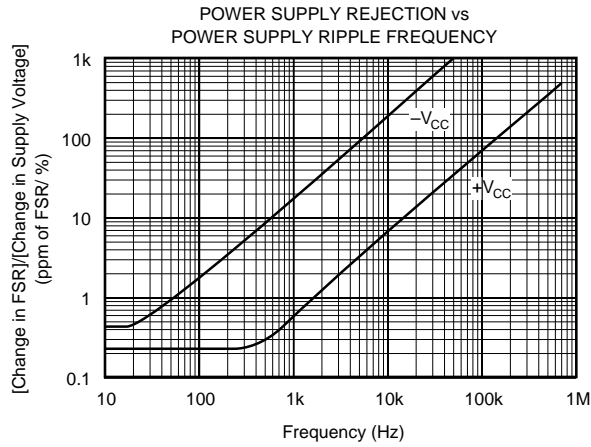
NOTES: X = Don't Care. (1) All digital input changes will appear at the output.

TIMING DIAGRAMS



TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of $\pm 1/2\text{LSB}$ means that the output step size can range from $1/2\text{LSB}$ to $3/2\text{LSB}$ when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than -1LSB , the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of the C and L grades is guaranteed over the specification temperature range to 16 bits.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within $\pm 0.003\%$ of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry (FFFF_H to 0000_H , and 0000_H to FFFF_H ; BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_s .

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_s .

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from 0000_H to FFFF_H .

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

The DAC714 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and a serial interface.

INTERFACE LOGIC

The DAC714 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to the block diagram shown in Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic “0” will enter the latch. When the enable inputs return to logic “1”, the data is latched.

The $\overline{\text{CLR}}$ input resets both the input latch and the D/A latch to 0000_H (midscale).

LOGIC INPUT COMPATIBILITY

The DAC714 digital inputs are TTL compatible (1.4V switching level), low leakage, and high impedance. Thus the inputs are suitable for being driven by any type of 5V logic Family, such as CMOS. An equivalent circuit for the digital inputs is shown in Figure 2.

The inputs will float to logic “0” if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

The DAC714 is designed to accept binary two’s complement (BTC) input codes with the MSB first which are compatible with bipolar analog output operation. For this configuration, a digital input of 7FFF_H produces a plus full scale output, 8000_H produces a minus full scale output, and 0000_H produces bipolar zero output.

INTERNAL REFERENCE

The DAC714 contains a +10V reference. The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

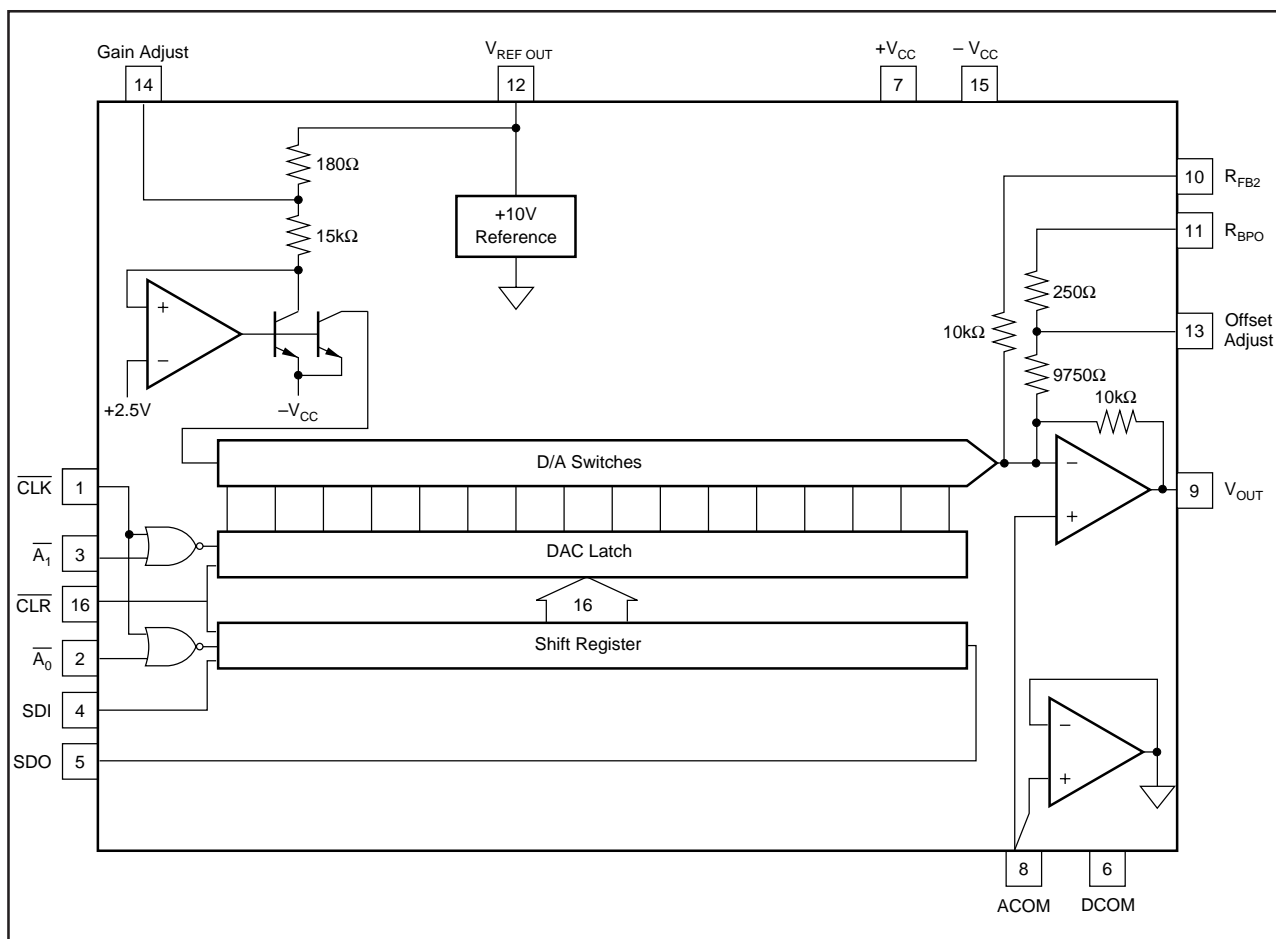


FIGURE 1. DAC714 Block Diagram.

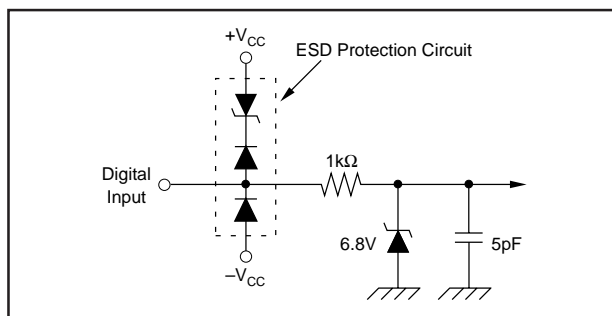


FIGURE 2. Equivalent Circuit of Digital Inputs.

OUTPUT VOLTAGE SWING

The output amplifier of the DAC714 is designed to achieve a $\pm 10\text{V}$ output range while operating on $\pm 11.4\text{V}$ or higher power supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of $\pm 0.3\%$.

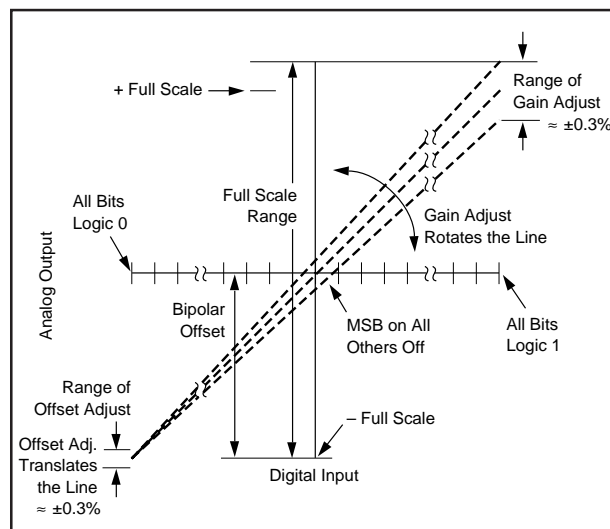


FIGURE 3. Relationship of Offset and Gain Adjustments.

Offset Adjustment

Apply the digital input code, 8000_H, that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for -10V (or 0V unipolar).

| DAC714 CALIBRATION VALUES | | | |
|---|----------------------|-----------------------|--------------------|
| DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC | ANALOG OUTPUT (V) | | DESCRIPTION |
| | BIPOLAR 20V RANGE | UNIPOLAR 10V RANGE | |
| 7FFF _H 4000 _H 0001 _H | +9.999695 | +9.999847 | + Full Scale -1LSB |
| 0000 _H | +5.000000 | +7.500000 | 3/4 Scale |
| 0001 _H | +0.000305 | +5.000153 | BPZ + 1LSB |
| 0000 _H | 0.000000 | +5.000000 | Bipolar Zero (BPZ) |
| FFFF _H C000 _H 8000 _H | -0.000305 | +4.999847 | BPZ - 1LSB |
| | -5.000000 | +2.500000 | 1/4 Scale |
| | -10.000000 | 0.000000 | Minus Full Scale |

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of the DAC714 system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305 μ V. With a load current of 5mA, series wiring and connector resistance of only 60m Ω will cause a voltage drop of 300 μ V. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 m Ω per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinch long will result in a voltage drop of 150 μ V.

The analog output of DAC714 has an LSB size of 305 μ V (-96dB) in the bipolar mode. The rms noise floor of the D/A should remain below this level in the frequency range of interest. The DAC714's output noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10 μ F tantalum capacitor at $-V_{CC}$. Applications with less

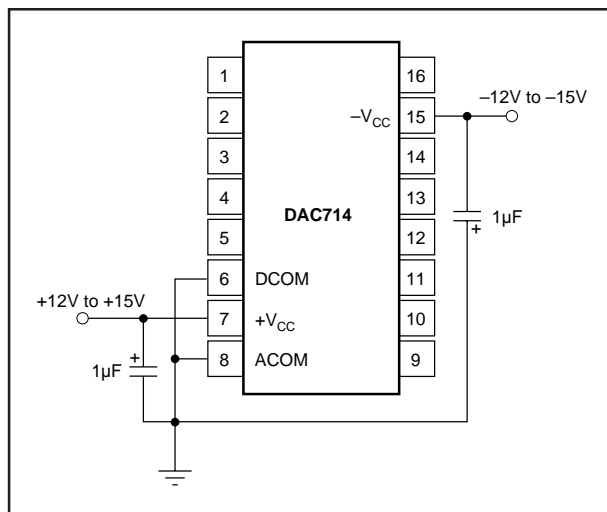


FIGURE 4. Power Supply Connections.

critical settling time may be able to use 0.01 μ F at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

The DAC714 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5 μ A for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC714s are used or if DAC714 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3 . As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in DAC714 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least $\pm 0.3\%$ of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of the DAC714 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of $30\mu\text{V}$ to $50\mu\text{V}$ per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, $+5\text{V}$.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC714 output amplifier is connected internally to provide a 20V output range. For other ranges and configurations, see Figures 6 and 7.

DIGITAL INTERFACE

SERIAL INTERFACE

The DAC714 has a serial interface with two data buffers which can be used for either synchronous or asynchronous updating of multiple D/A converters. $\overline{\text{A0}}$ is the enable control for the input shift register. $\overline{\text{A1}}$ is the enable for the D/A Latch. $\overline{\text{CLK}}$ is used to strobe data into the latches enabled by $\overline{\text{A0}}$ and $\overline{\text{A1}}$. A CLR function is also provided and when enabled it sets the shift register and the D/A Latch to 0000_{H} (output voltage is midscale).

Multiple DAC714s can be connected to the same $\overline{\text{CLK}}$ and data lines in two ways. The output of the serial shift register is available as SDO so that any number of DAC714s can be cascaded on the same input bit stream as shown in Figures 8 and 9. This configuration allows all D/A converters to be updated simultaneously and requires a minimum number of control signals. These configurations do require $16N$ $\overline{\text{CLK}}$ cycles to load any given D/A converter, where N is the number of D/A converters.

The DAC714 can also be connected in parallel as shown in Figure 10. This configuration allows any D/A converter in the system to be updated in a maximum of 16 CLK cycles.

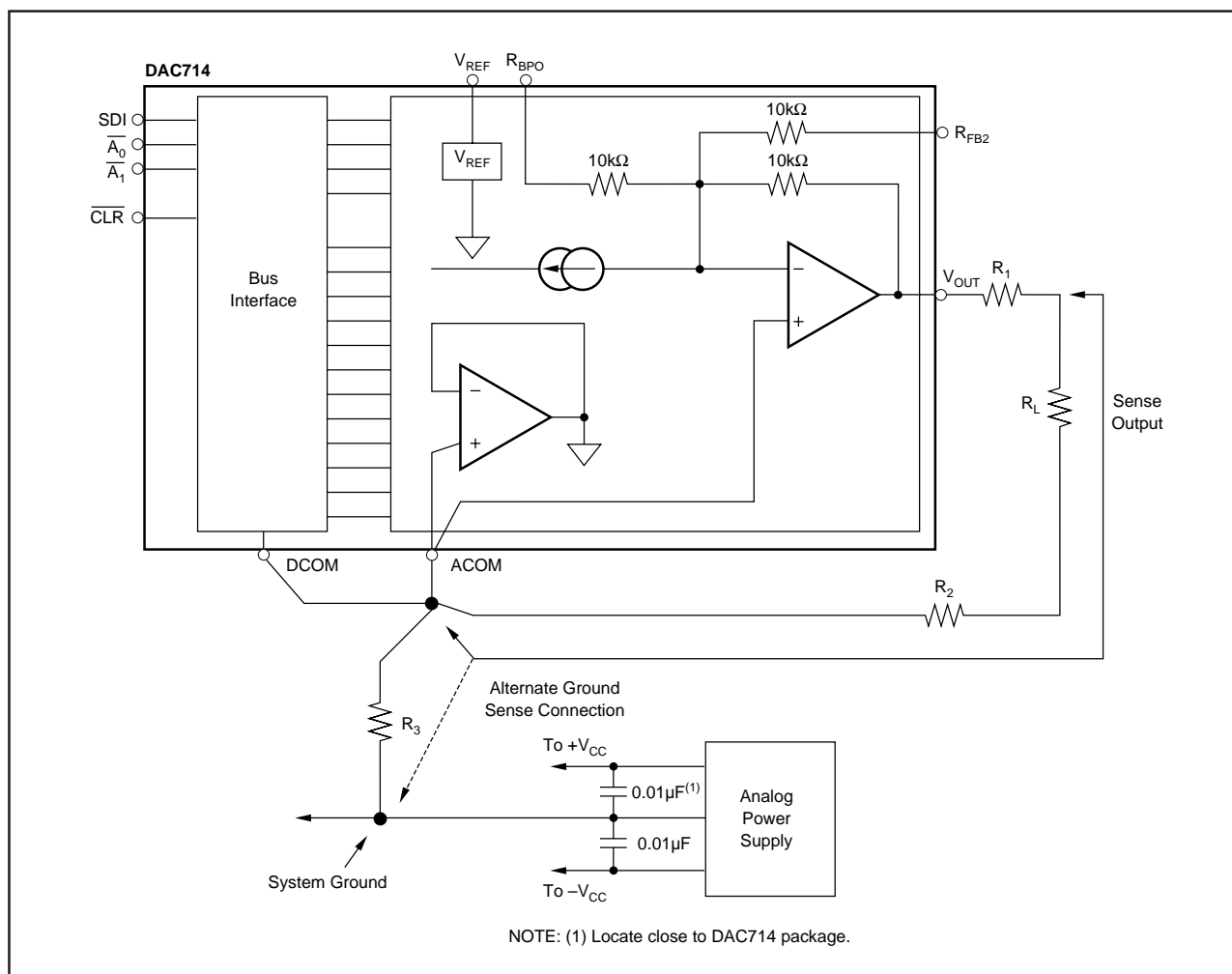


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

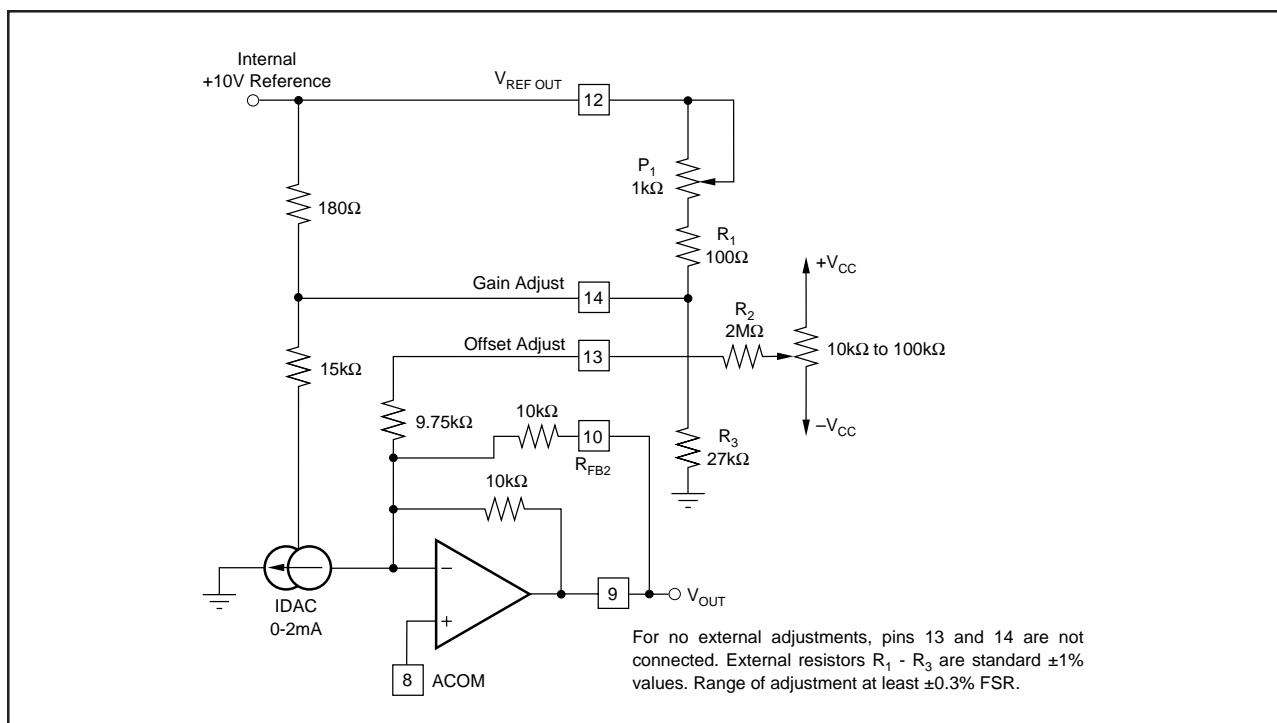


FIGURE 6a. Manual Offset and Gain Adjust Circuits; Unipolar Mode (0V to +10V output range).

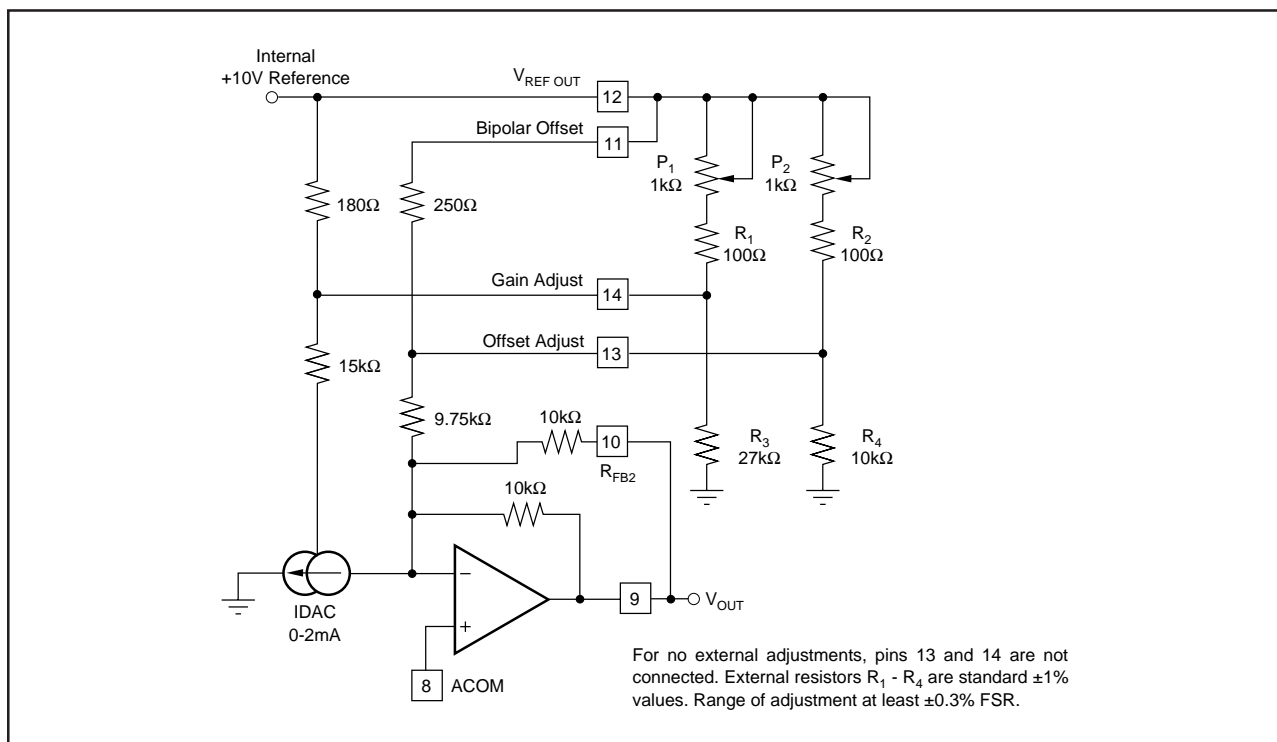


FIGURE 6b. Manual Offset and Gain Adjust Circuits; Bipolar Mode (-5V to +5V output range).

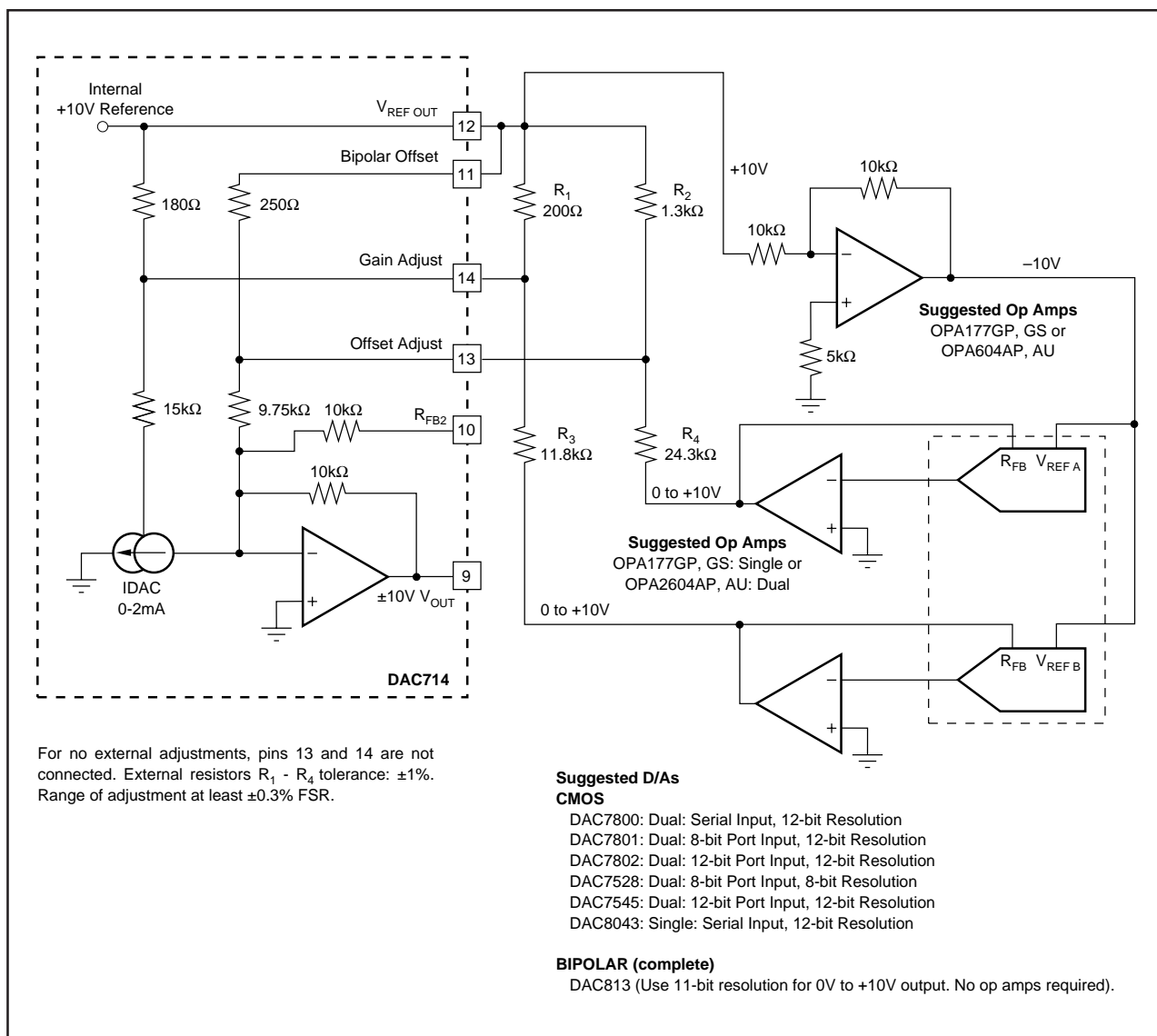


FIGURE 7. Gain and Offset Adjustment in the Bipolar Mode Using D/A Converters (–10V to +10V output range).

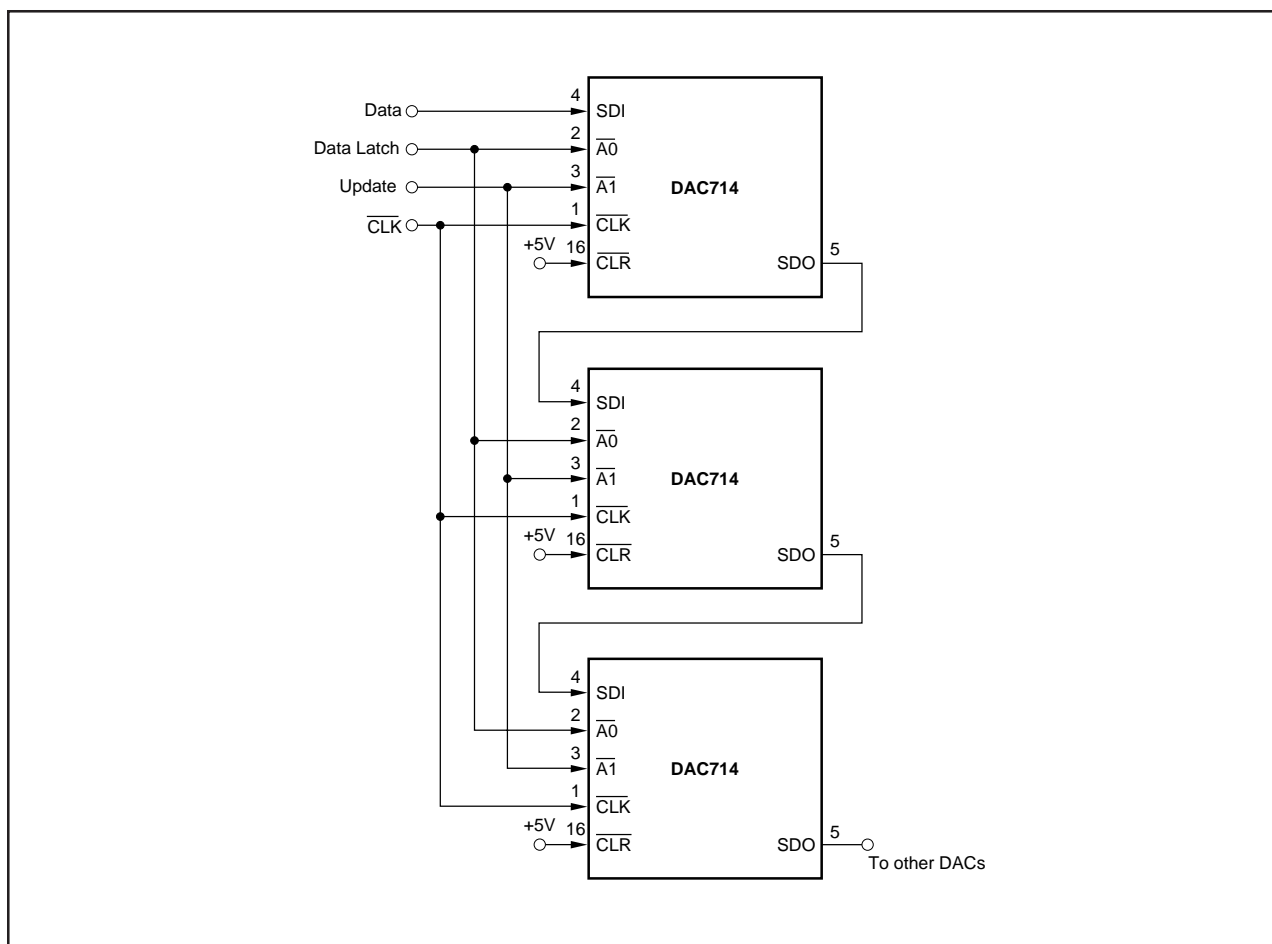


FIGURE 8a. Cascaded Serial Bus Connection with Synchronous Update.

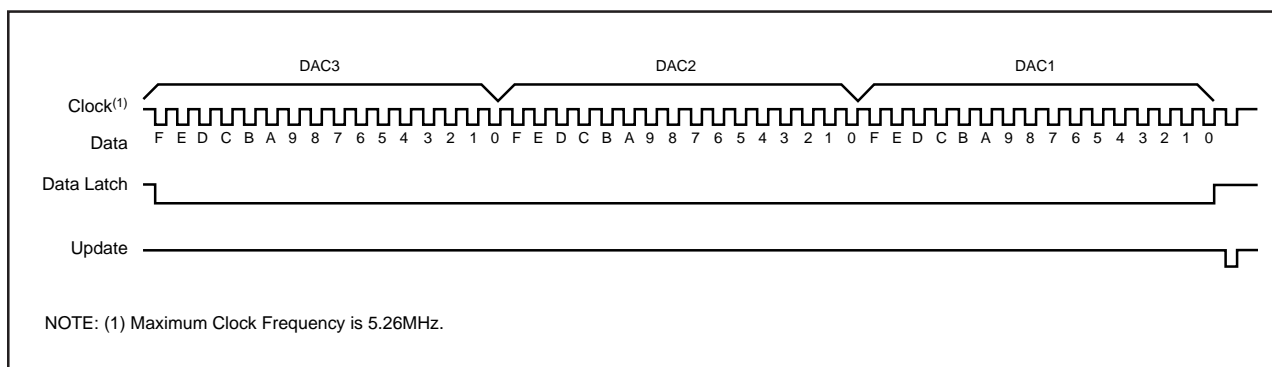


FIGURE 8b. Timing Diagram For Figure 8a.

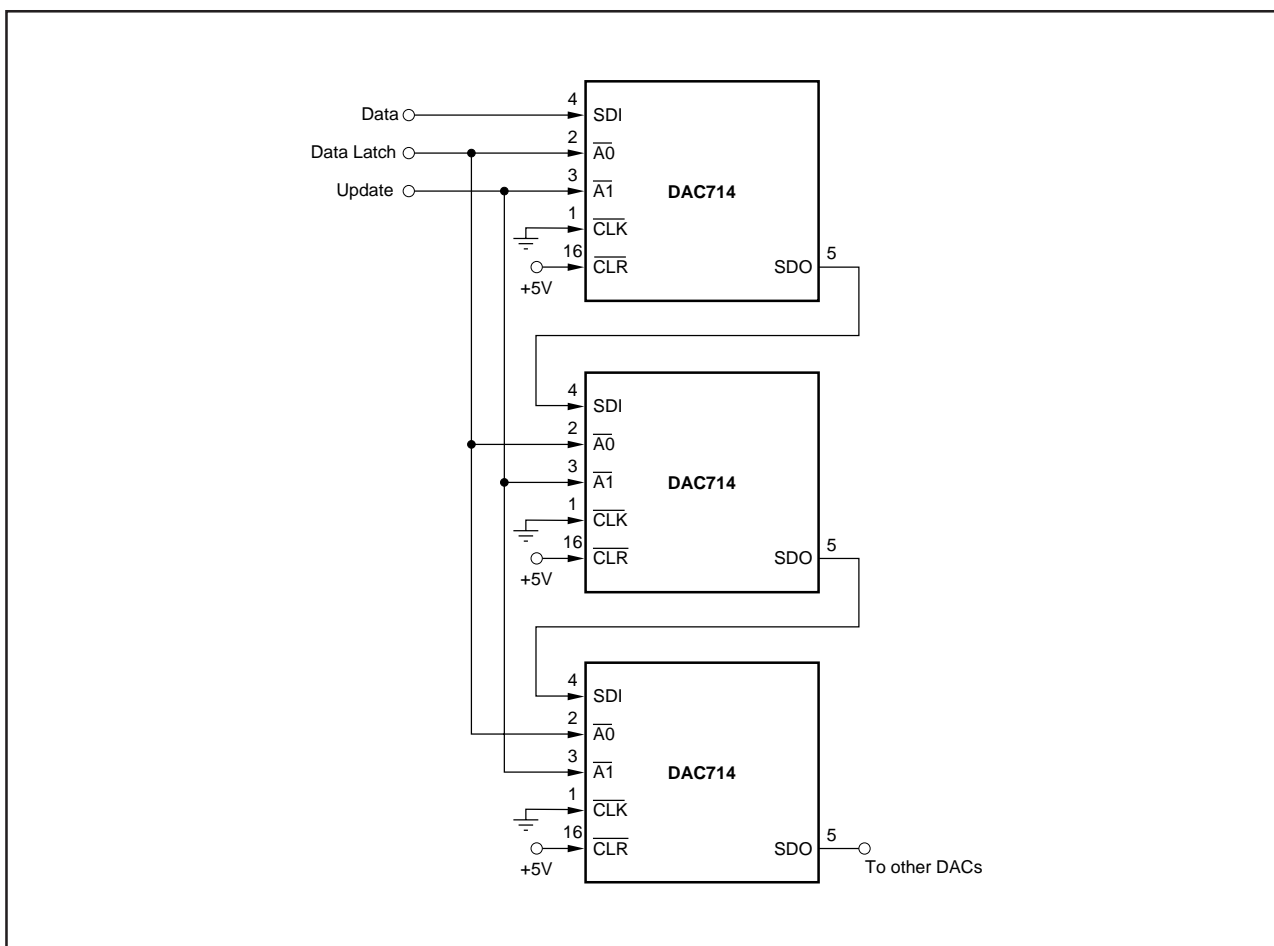


FIGURE 9a. Cascaded Serial Bus Connection with Asynchronous Update.

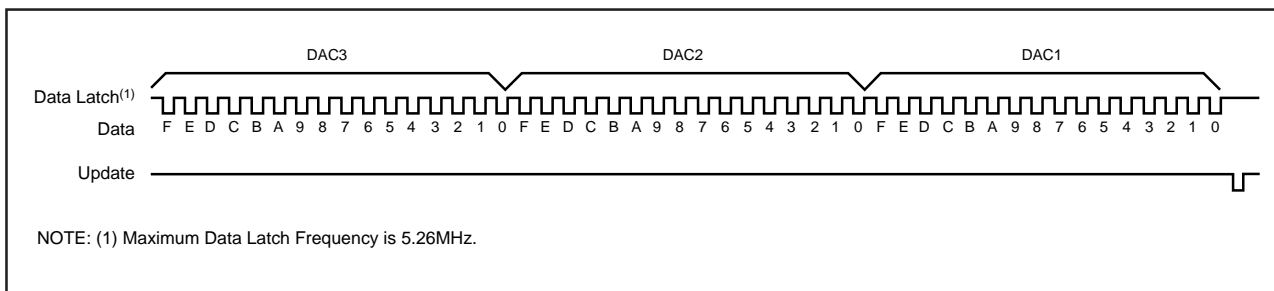


FIGURE 9b. Timing Diagram For Figure 9a.

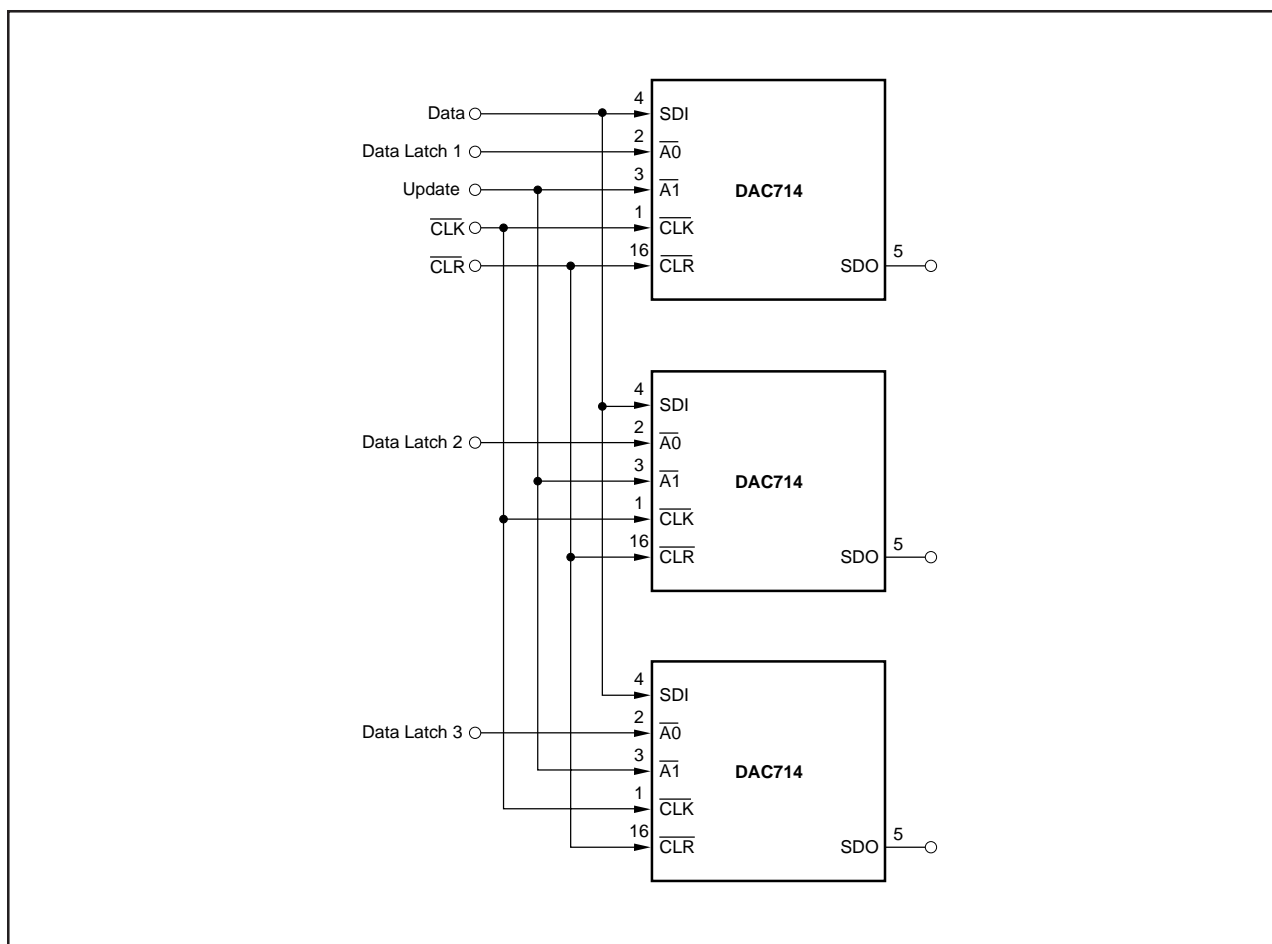


FIGURE 10a. Parallel Bus Connection.

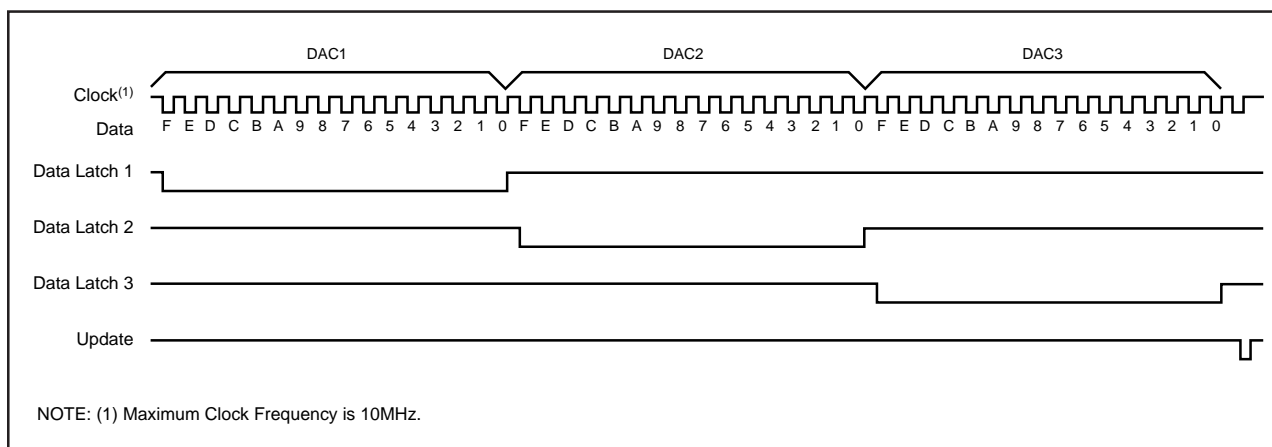


FIGURE 10b. Timing Diagram For Figure 10a.

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