

Document Title

1Mx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	October 31, 2002	Preliminary
0.1	Revised - Deleted 44-TSOP2-400R package type. - Added Commercial product.	December 11, 2002	Preliminary

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1Mx8 bit Low Power full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 1M x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F

GENERAL DESCRIPTION

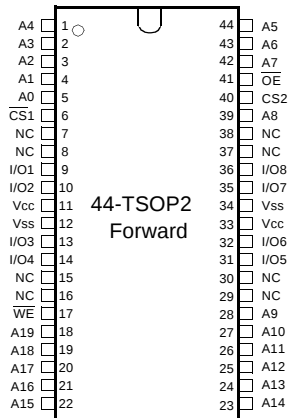
The K6X8008C2B families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support various operating temperature range for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6X8008C2B-B	Commercial(0~70°C)	4.5~5.5V	55 ¹⁾ /70ns	40μA	50mA	44-TSOP2-400F
K6X8008C2B-F	Industrial(-40~85°C)			40μA		
K6X8008C2B-Q	Automotive(-40~125°C)			50μA		

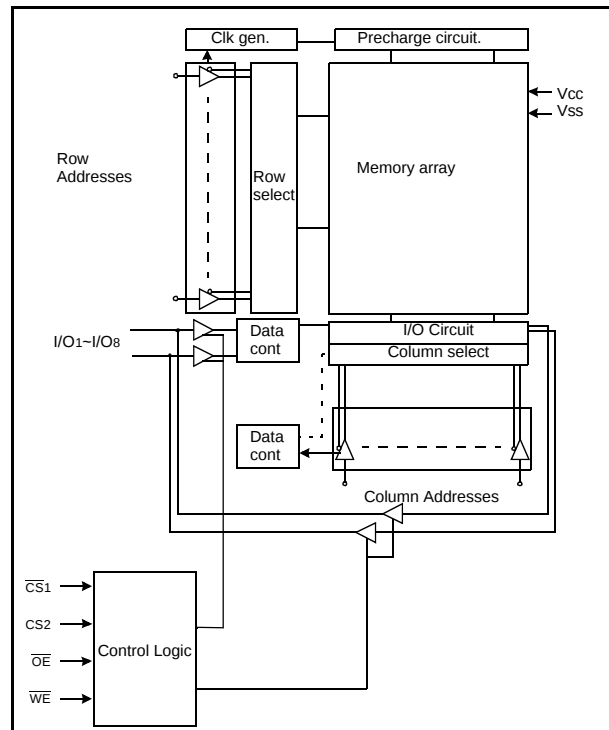
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS1}$, $\overline{CS2}$	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	A0~A19	Address Inputs
I/O1~I/O8	Data Inputs/Outputs	NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X8008C2B-TB55 K6X8008C2B-TB70	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL	K6X8008C2B-TF55 K6X8008C2B-TF70	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL	K6X8008C2B-TQ55 K6X8008C2B-TQ70	44-TSOP2-F, 55ns, L 44-TSOP2-F, 70ns, L

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O ₁₋₈	Mode	Power
H	X	X	X	High-Z	Deselected	Standby
X	L	X	X	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X	L	Din	Write	Active

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V(max.7.0V)	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6X8008C2B-B
		-40 to 85	°C	K6X8008C2B-F
		-40 to 125	°C	K6X8008C2B-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6X8008C2B Family	4.5	5.0	5.5	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6X8008C2B Family	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	K6X8008C2B Family	-0.5 ³⁾	-	0.8	V

Note:

1. Commercial Product: T_A=0 to 70°C, otherwise specified.
Industrial Product: T_A=-40 to 85°C, otherwise specified.
Automotive Product: T_A=-40 to 125°C, otherwise specified.
2. Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns.
3. Undershoot: -3.0V in case of pulse width ≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

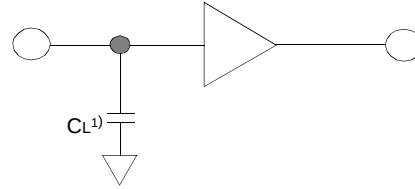
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , $\overline{WE}$ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	10	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	10	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	50	mA	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	3	mA	
Standby Current(CMOS)	I _{SB1}	Other input =0~V _{CC} , 1) $\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V ($\overline{CS_1}$ controlled) or 2) 0V≤CS ₂ ≤0.2V(CS ₂ controlled)	K6X8008C2B-B	-	-	40	μA
			K6X8008C2B-F	-	-	40	
			K6X8008C2B-Q	-	-	50	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.8 to 2.4V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS

($V_{CC}=4.5\sim 5.5\text{V}$, Commercial product: $T_A=0$ to 70°C , Industrial product: $T_A=-40$ to 85°C , Automotive product: $T_A=-40$ to 125°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	55	-	70	-	ns
	Address Access Time	tAA	-	55	-	70	ns
	Chip Select to Output	tCO	-	55	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	35	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	20	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
	Output Hold from Address Change	tOH	10	-	10	-	ns
Write	Write Cycle Time	tWC	55	-	70	-	ns
	Chip Select to End of Write	tCW	45	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	45	-	60	-	ns
	Write Pulse Width	tWP	40	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	20	0	20	ns
	Data to Write Time Overlap	tDW	25	-	30	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
	End Write to Output Low-Z	tOW	5	-	5	-	ns

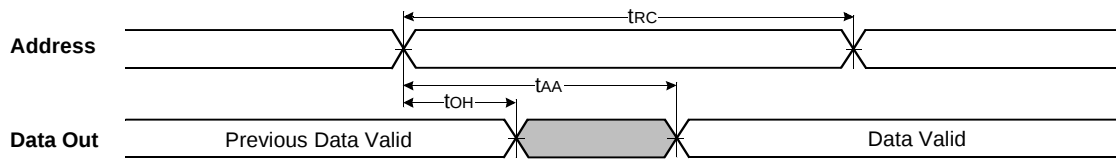
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$		2.0	-	5.5	V
Data retention current	IDR	$V_{CC}=3.0\text{V}, \overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$		-	-	30	μA
						30	
						40	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ms
Recovery time	tRDR			5	-	-	

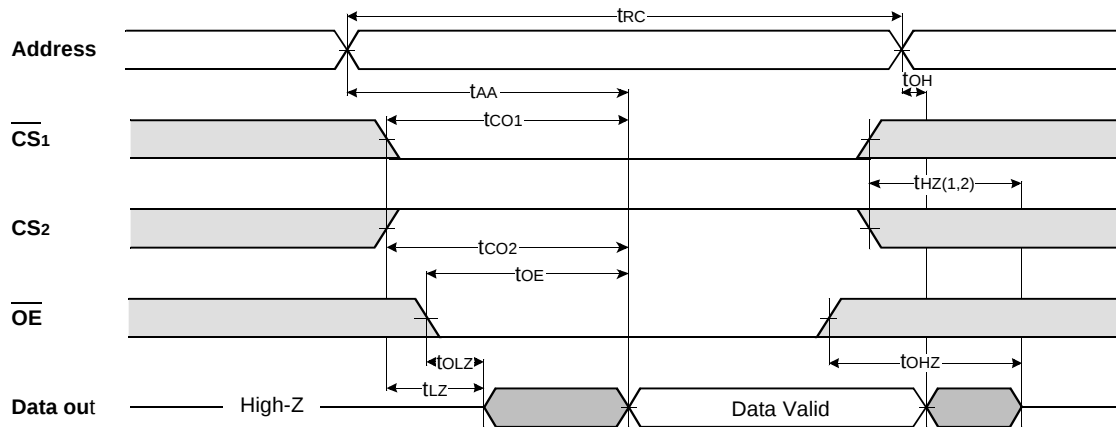
1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}, \overline{CS}_2 \geq V_{CC}-0.2\text{V} (\overline{CS}_1 \text{ controlled})$ or $\overline{CS}_2 \geq V_{CC}-0.2\text{V} (\overline{CS}_2 \text{ controlled})$.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}=\overline{OE}=V_{IL}$, $CS_2=\overline{WE}=V_{IH}$)



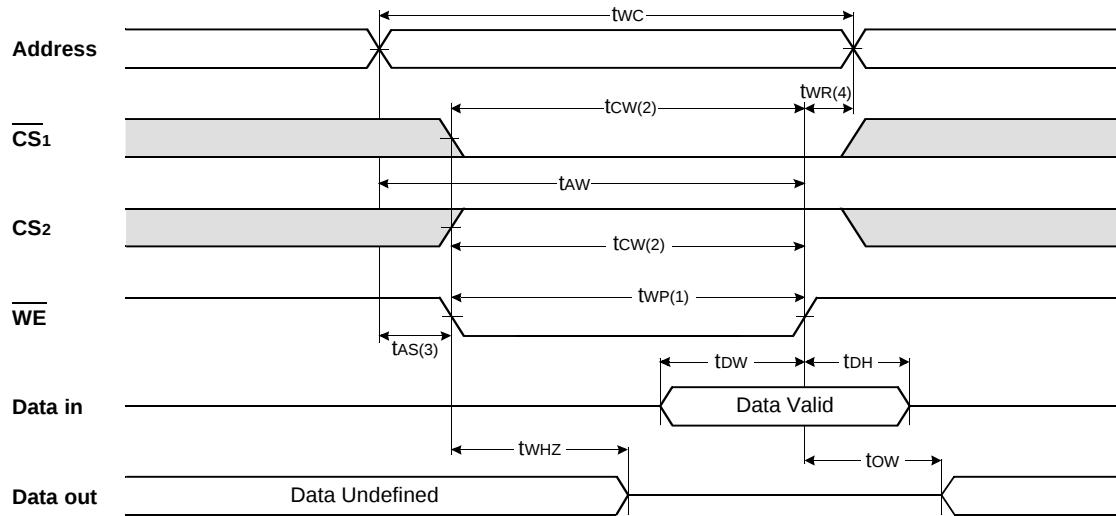
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



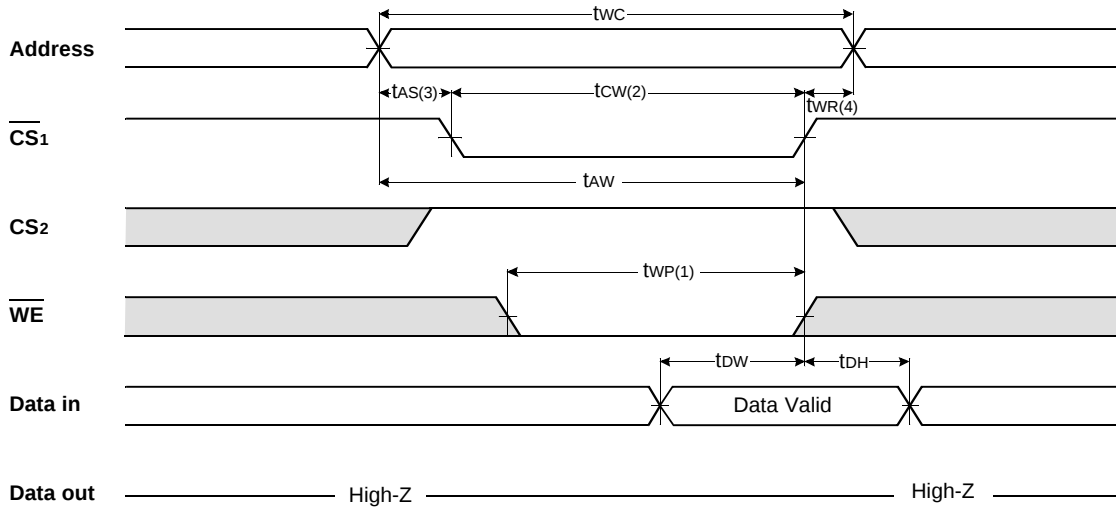
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



The diagram illustrates the timing relationships for the 28C02 EPROM. The signals shown are Address, CS1, CS2, WE, Data in, and Data out. The timing parameters are defined as follows:

- tWC**: Write Cycle time, from the start of the first address strobe to the start of the last address strobe.
- tAS(3)**: Address Strobe pulse width, the duration of the first address strobe.
- tCW(2)**: Chip Write time, the time from the start of the first address strobe to the start of the last address strobe.
- tWR(4)**: Word Strobe pulse width, the duration of the last address strobe.
- tAW**: Address Valid time, the time from the start of the first address strobe to the start of the last address strobe.
- tCW(2)**: Chip Write time, the time from the start of the first address strobe to the start of the last address strobe.
- tWP(1)**: Word Pulse time, the time from the start of the first address strobe to the start of the last address strobe.
- tdw**: Data Valid time, the time from the start of the last address strobe to the start of the last data strobe.
- tdH**: Data Hold time, the time from the start of the last data strobe to the start of the last address strobe.

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among CS_1 going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS_2 going to low.

Timing diagram for Data Retention Mode. The diagram shows the relationship between VCC, CS2, and VDR signals. VCC is high during normal operation and drops to 0.4V during Data Retention Mode. CS2 is high during normal operation and drops to 0.2V or lower during Data Retention Mode. VDR is high during normal operation and drops to 0.4V during Data Retention Mode. The duration of Data Retention Mode is indicated by a double-headed arrow. The time from VCC falling to CS2 falling is tSDR, and the time from CS2 rising to VDR rising is tRDR.

Preliminary CMOS SRAM

Unit: millimeters(inches)

THIN SMALL OUTLINE PACKAGE TYPE II (400F)

Top View:

- Pin 1 indicator circle at bottom-left corner.
- Pin numbers: #1, #22, #23, #44.
- Overall width: 11.76 ± 0.20 mm (0.463 ± 0.008 in).
- Overall length: 18.81 mm (0.741 in) MAX.
- Length to last pin: 18.41 ± 0.10 mm (0.725 ± 0.004 in).
- Pin pitch: 0.35 ± 0.10 mm (0.014 ± 0.004 in).
- Pin width: 0.80 mm (0.0315 in).
- Pin thickness: 0.05 mm MIN.
- Pin spacing from package edge: 0.02 mm.
- Pin thickness tolerance: 0.10 mm MAX.

Side View:

- Package height: 10.16 mm (0.400 in).
- Lead angle: $0^\circ - 8^\circ$.
- Lead thickness: 0.25 mm (0.010 in).
- Lead width: $0.45 - 0.75$ mm ($0.018 - 0.030$ in).
- Lead thickness tolerance: 0.50 mm (0.020 in).
- Lead angle tolerance: $+0.10$ / -0.05 degrees.
- Lead width tolerance: $+0.004$ / -0.002 mm.