Ordering number : EN4801A

CMOS LSI

SANYO

No. 4801A

LC75823E, 75823W

1/3 Duty General-Purpose LCD Drivers

CCB

Overview

The LC75823E and LC75823W are general-purpose LCD display drivers that can be used for frequency display in microprocessor-controlled radio receives and in other display applications. In addition to being able to directly drive up to 156 LCD segments.

Features

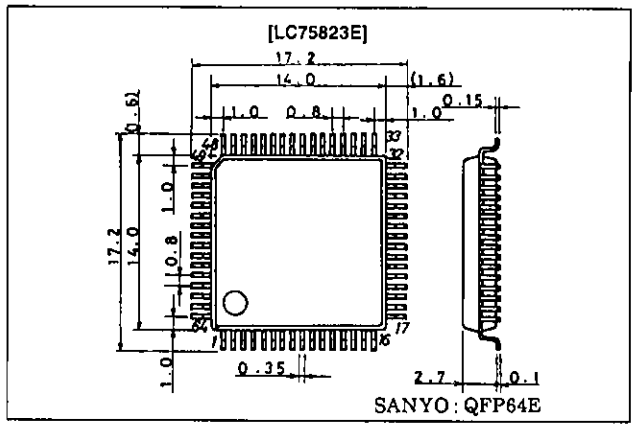
- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD drive of up to 156 segments under serial data control.
- Serial data input supports CCB* format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- High generality since display data is displayed directly without decoder intervention.
- The $\overline{INH}$ pin can force the display to the off state.
- The LCD drive bias voltage can be provided internally or externally.
- Power supply voltage: 4.5 to 6 V
- The LC75823E/W is a low-voltage version of LC75850E/W. (Pin compatible)

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

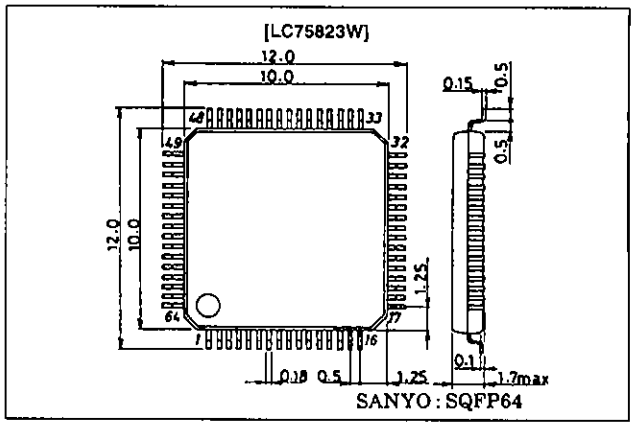
unit: mm

3159-QFP64E



unit: mm

3190-SQFP64



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +6.5	V
Input voltage	V_{IN} 1	CE, CL, DI, $\overline{INH}$	−0.3 to +6.5	V
	V_{IN} 2	OSC	−0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	OSC	−0.3 to V_{DD} + 0.3	V
Output current	I_{OUT} 1	S1 to S52	300	μA
	I_{OUT} 2	COM1 to COM3	3	mA
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

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Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input voltage	$V_{DD}1$	$V_{DD}1$		2/3 V_{DD}	6.0	V
	$V_{DD}2$	$V_{DD}2$		1/3 V_{DD}	6.0	V
Input high level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	4.0		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.7	V
Recommended external resistance	R_{OSC}	OSC		47		kΩ
Recommended external capacitance	C_{OSC}	OSC		1000		pF
Guaranteed oscillator range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	100			ns
Data hold time	t_{dh}	CL, DI: Figure 2	100			ns
CE wait time	t_{cp}	CE, CL: Figure 2	100			ns
CE setup time	t_{cs}	CE, CL: Figure 2	100			ns
CE hold time	t_{ch}	CE, CL: Figure 2	100			ns
High-level clock pulse width	$t_{\phi H}$	CL: Figure 2	100			ns
Low-level clock pulse width	$t_{\phi L}$	CL: Figure 2	100			ns
Rise time	t_r	CE, CL, DI: Figure 2		100		ns
Fall time	t_f	CE, CL, DI: Figure 2		100		ns
$\overline{INH}$ switching time	t2	$\overline{INH}$, CE:Figure 3	10			μs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$; V_I = 6 V			5	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$; V_I = 0 V	–5			μA
Oscillator frequency	f_{OSC}	OSC; R_{OSC} = 47 kΩ C_{OSC} = 1000 pF		38		kHz
Hysteresis width	V_H	CE, CL, DI, $\overline{INH}$; V_{DD} = 5 V	0.3			V
Output high level voltage	V_{OH} 1	S1 to S52; I_O = –20 μA	V_{DD} – 1.0			V
Output low level voltage	V_{OL} 1	S1 to S52; I_O = 20 μA			1.0	V
Output high level voltage	V_{OH} 2	COM1 to COM3; I_O = –100 μA	V_{DD} – 1.0			V
Output low level voltage	V_{OL} 2	COM1 to COM3; I_O = 100 μA			1.0	V
Intermediate level voltage*	V_{MID} 1	1/2 bias, COM1 to COM3; I_O = ±100 μA	1/2 V_{DD} ± 1.0			V
	V_{MID} 2	1/3 bias, COM1 to COM3; I_O = ±100 μA	2/3 V_{DD} ± 1.0			V
	V_{MID} 3	1/3 bias, COM1 to COM3; I_O = ±100 μA	1/3 V_{DD} ± 1.0			V
	V_{MID} 4	1/3 bias, S1 to S52; I_O = ±20 μA	2/3 V_{DD} ± 1.0			V
	V_{MID} 5	1/3 bias, S1 to S52; I_O = ±20 μA	1/3 V_{DD} ± 1.0			V
Supply current	I_{DD} 1	Power saving mode			5	μA
	I_{DD} 2	f = 38 kHz, 1/2 bias, V_{DD} = 5 V		400	800	μA
	I_{DD} 3	f = 38 kHz, 1/3 bias, V_{DD} = 5 V		300	600	μA
	I_{DD} 2	f = 38 kHz, 1/2 bias, V_{DD} = 6 V		650	1300	μA
	I_{DD} 3	f = 38 kHz, 1/3 bias, V_{DD} = 6 V		580	1200	μA

Note: * Except the bias voltage generation divider resistors that are built into $V_{DD}1$ and $V_{DD}2$. (See figure 1.)

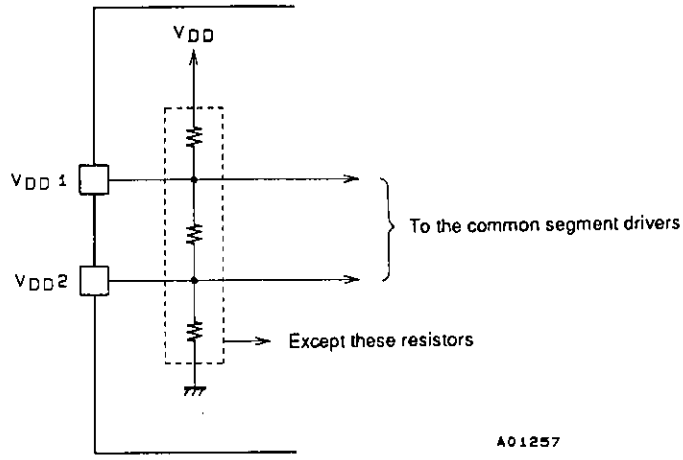
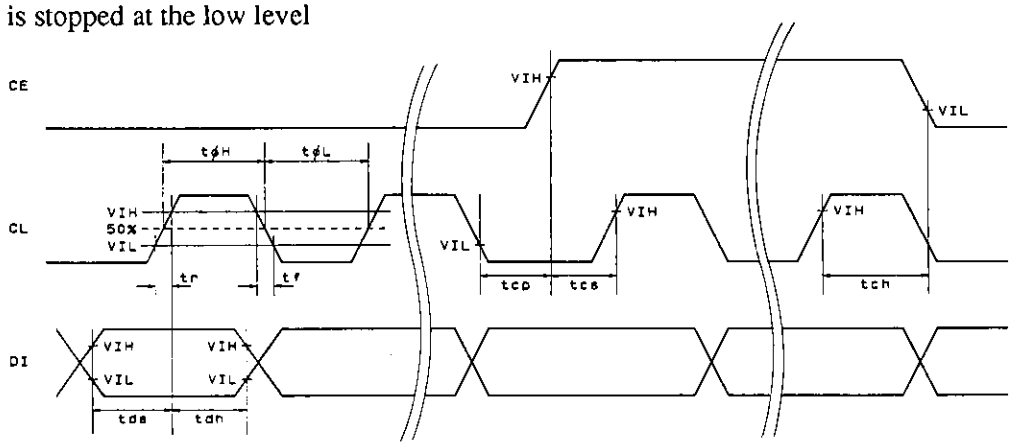


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

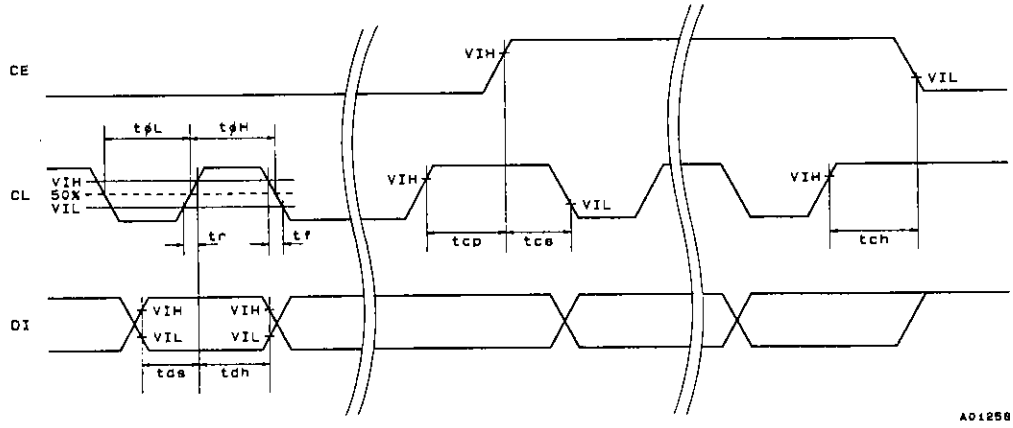
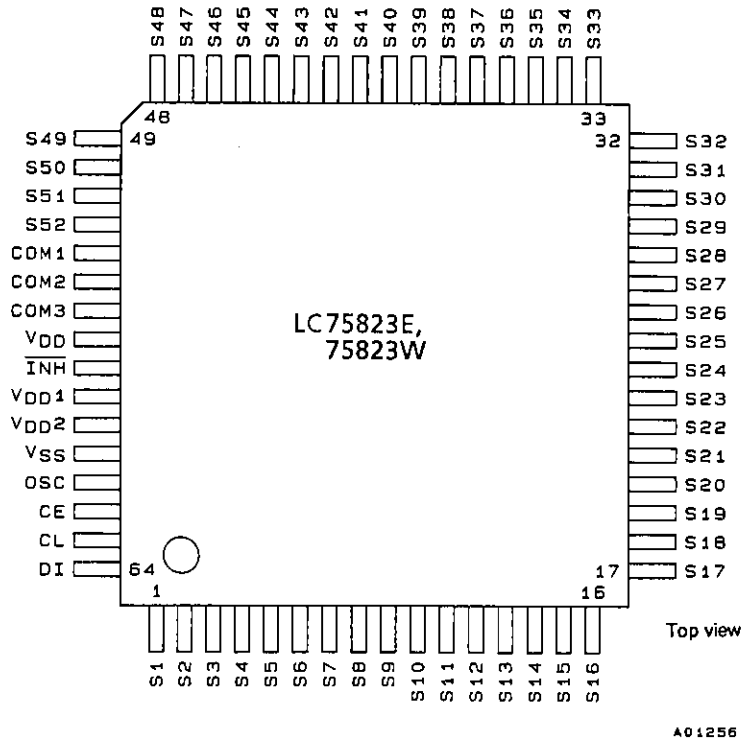
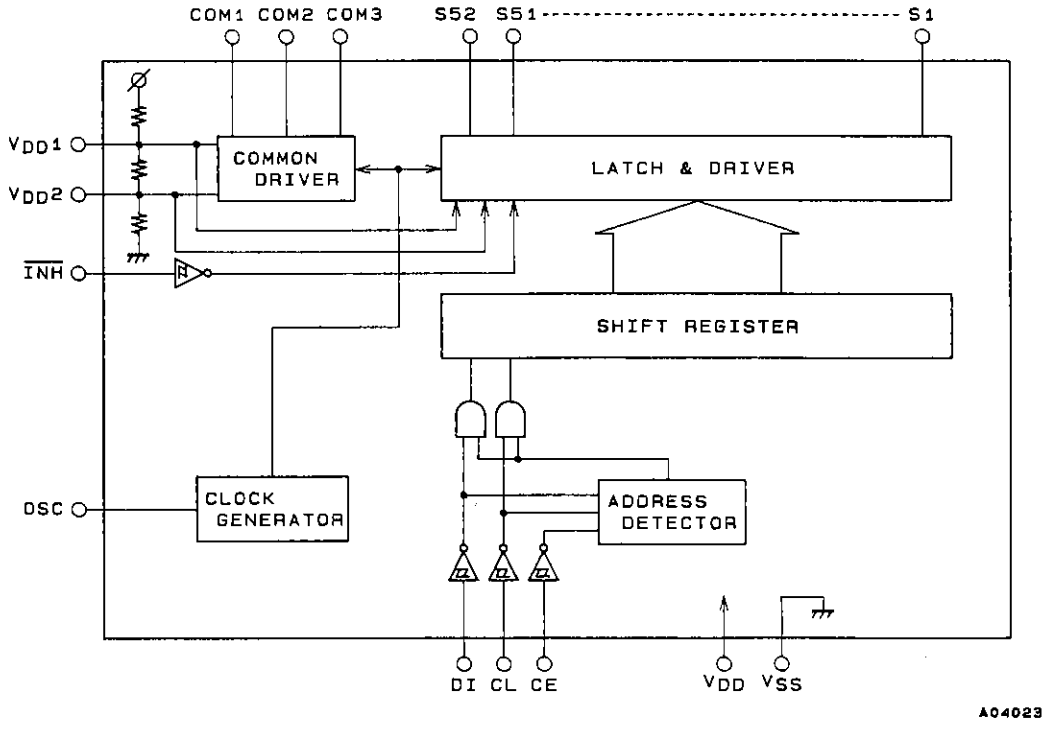


Figure 2

Pin Assignment



Block Diagram

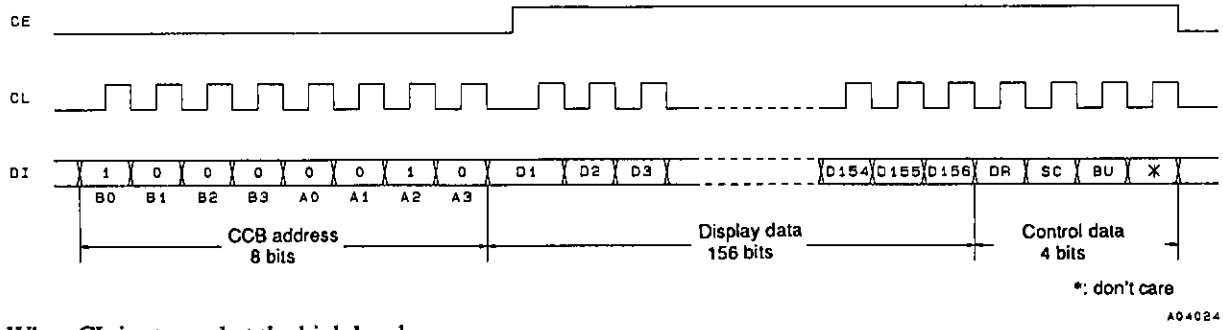


Pin Functions

Pin	Pin No.	Function		Active	I/O	Handling when unused
S1 to S52	1 to 52	Segment outputs for displaying the display data transferred by serial data input.		—	O	Open
COM1 COM2 COM3	53 54 55	Common driver outputs. The frame frequency f_O is given by: $f_O = (f_{OSC}/384)$ Hz.		—	O	Open
OSC	61	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.		—	I/O	V_{DD}
CE CL DI	62 63 64	Serial data transfer inputs. These pins are connected to the control microprocessor.	CE: chip enable CL: synchronization clock DI: transfer data	H ↑ —	I	GND
$\overline{INH}$	57	Display off control input •$\overline{INH}$ = low (V_{SS}).....Display forced off (S1 to S52, COM1 to COM3 = low) •$\overline{INH}$ = high (V_{DD}) .....Display on Note that serial data transfers can be performed when the display is forced off.		L	I	GND
$V_{DD}1$	58	Used for the 2/3 bias voltage when bias voltages are provided externally. Connect to $V_{DD}2$ when 1/2 bias is used.		—	I	Open
$V_{DD}2$	59	Used for the 1/3 bias voltage when bias voltages are provided externally. Connect to $V_{DD}1$ when 1/2 bias is used.		—	I	Open
V_{DD}	56	Power supply. Provide a voltage of between 4.5 and 6.0 V.		—	—	—
V_{SS}	60	Ground. Connect this pin to the system ground.		—	—	—

Serial Data Transfer Format

1. When CL is stopped at the low level



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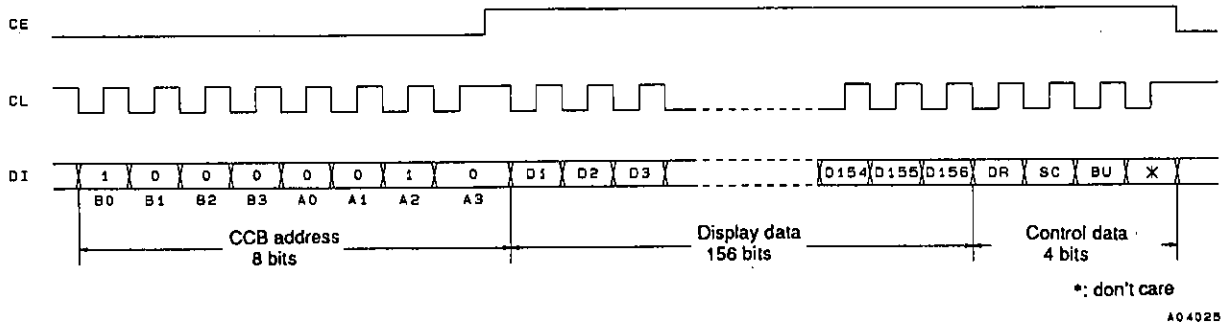
2. When CL is stopped at the high level



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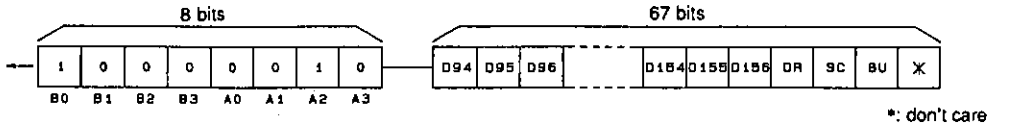
- CCB address.....41H
- D1 to D156.....Display data
  Dn (n = 1 to 156) = 1.....Display on
  Dn (n = 1 to 156) = 0.....Display off
- DR .....1/2-bias drive or 1/3-bias drive switching control data
- SC.....Segments on/off control data
- BU .....Normal mode/power-saving mode control data

Serial Data Transfer Examples

- When 63 segments are used
  63 bits of display data (D94 to D156) must be sent.



Control Data Functions

1. DR: 1/2-bias drive or 1/3-bias drive switching control data
   This control data bit selects either 1/2-bias drive or 1/3-bias drive.

DR	Drive type
0	1/2-bias drive
1	1/3-bias drive

2. SC: Segments on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

   However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

3. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power-saving mode. In this mode the OSC pin oscillator is stopped and the common and segment pins output V_{SS} levels.

Display Data to Segment Output Pin Correspondence

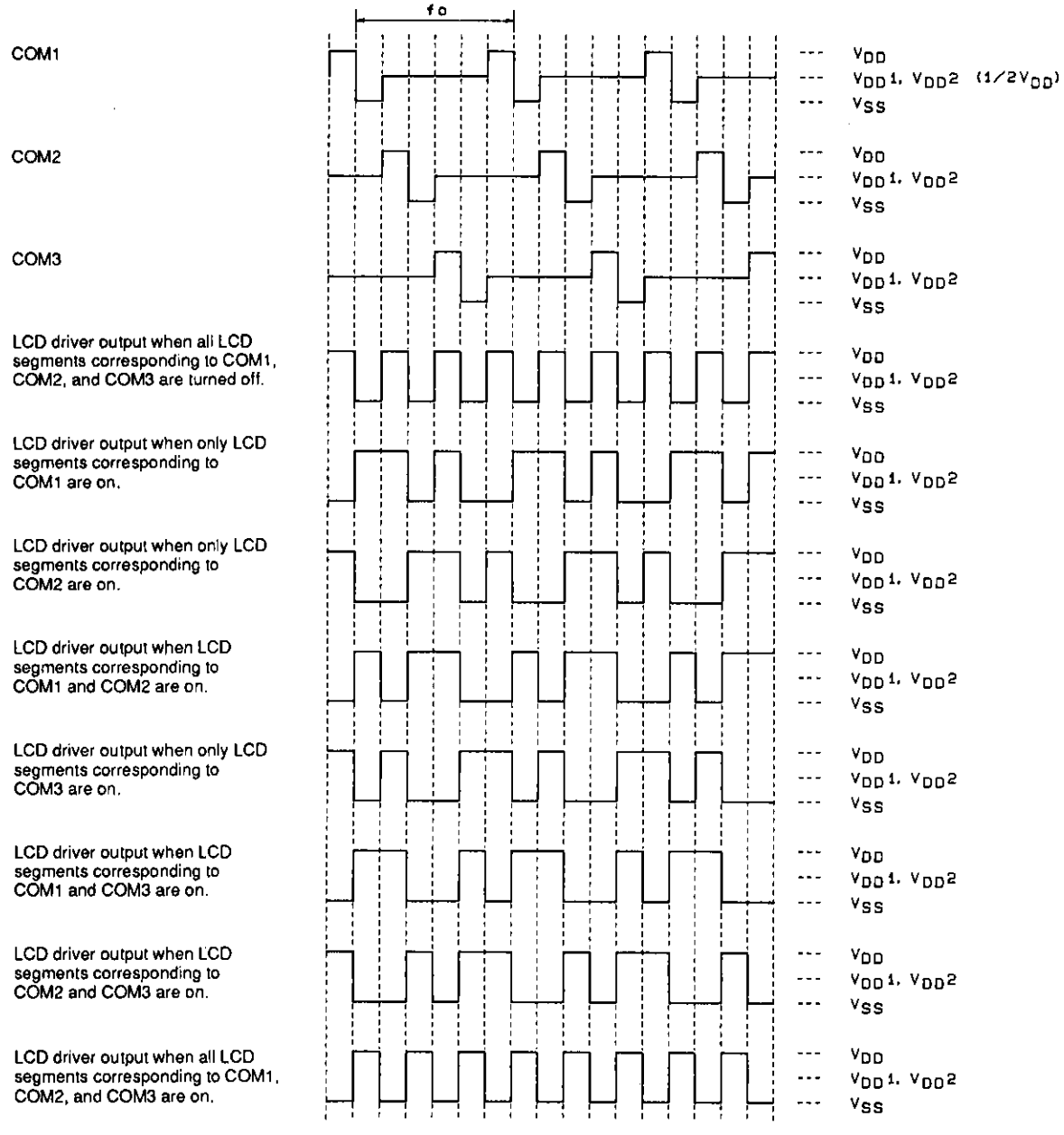
Segment output pin	COM3	COM2	COM1
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78

Segment output pin	COM3	COM2	COM1
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156

For example, the table below lists the segment output states for the S11 output pin.

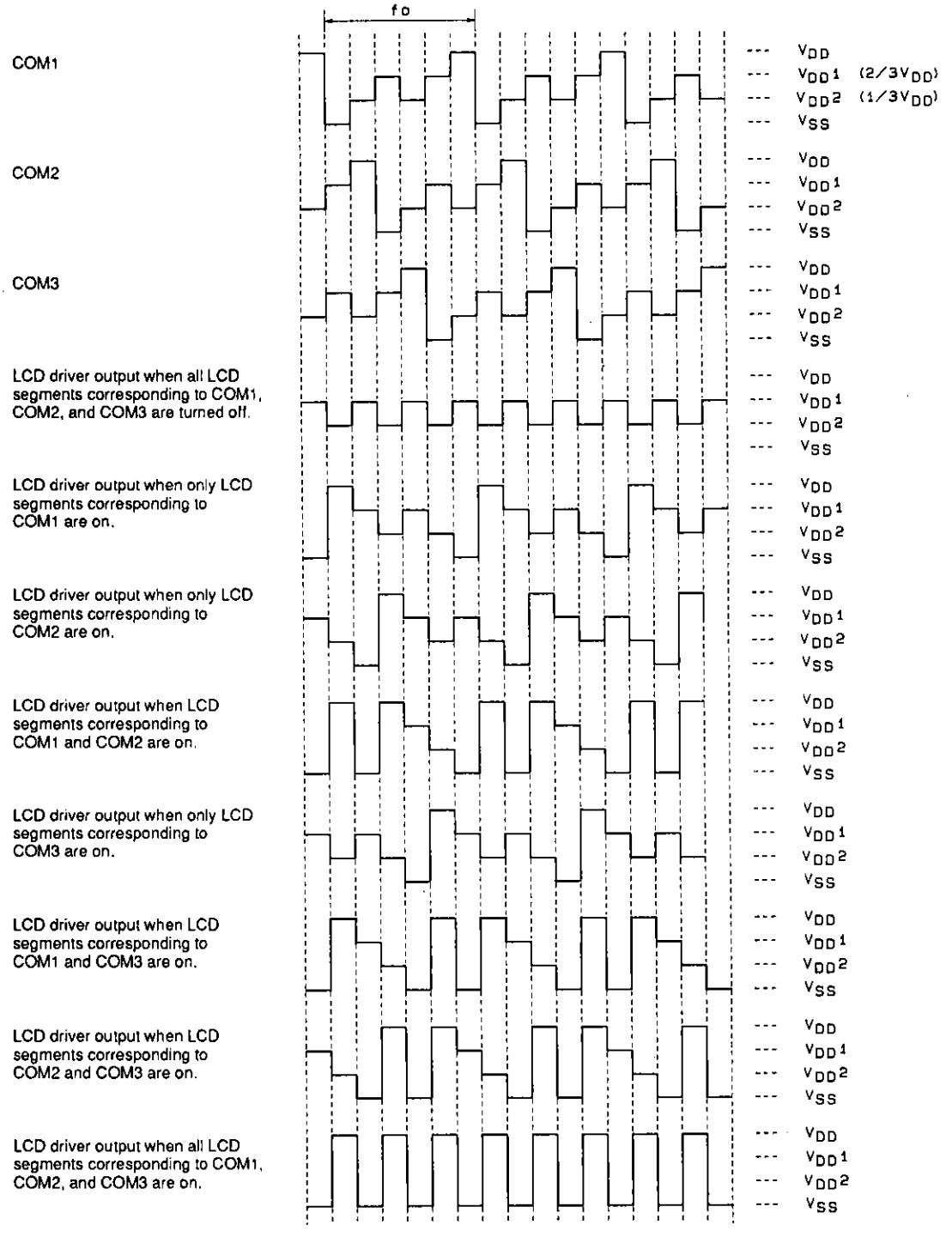
Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1 to COM3 are off.
0	0	1	The LCD segments corresponding to COM1 is on.
0	1	0	The LCD segments corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM1 and COM2 are on.
1	0	0	The LCD segments corresponding to COM3 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
1	1	1	The LCD segments corresponding to COM1 to COM3 are on.

1/2 Bias, 1/3 Duty Drive Technique



1/2 Bias, 1/3 Duty Waveforms

1/3 Bias, 1/3 Duty Drive Technique



1/3 Bias, 1/3 Duty Waveforms

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$\overline{\text{INH}}$ and Display Control

Since the LSI internal data (D1 to D156, DR, SC, and BU) is undefined when power is first applied, the display is off (S1 to S52, COM1 to COM3 = low) by setting the $\overline{\text{INH}}$ pin low at the same time as power is applied. Then, meaningless display at the power-on can be prevented by transferring serial data from the controller while the display is off and setting $\overline{\text{INH}}$ pin high after the transfer completes. (See Figure 3.)

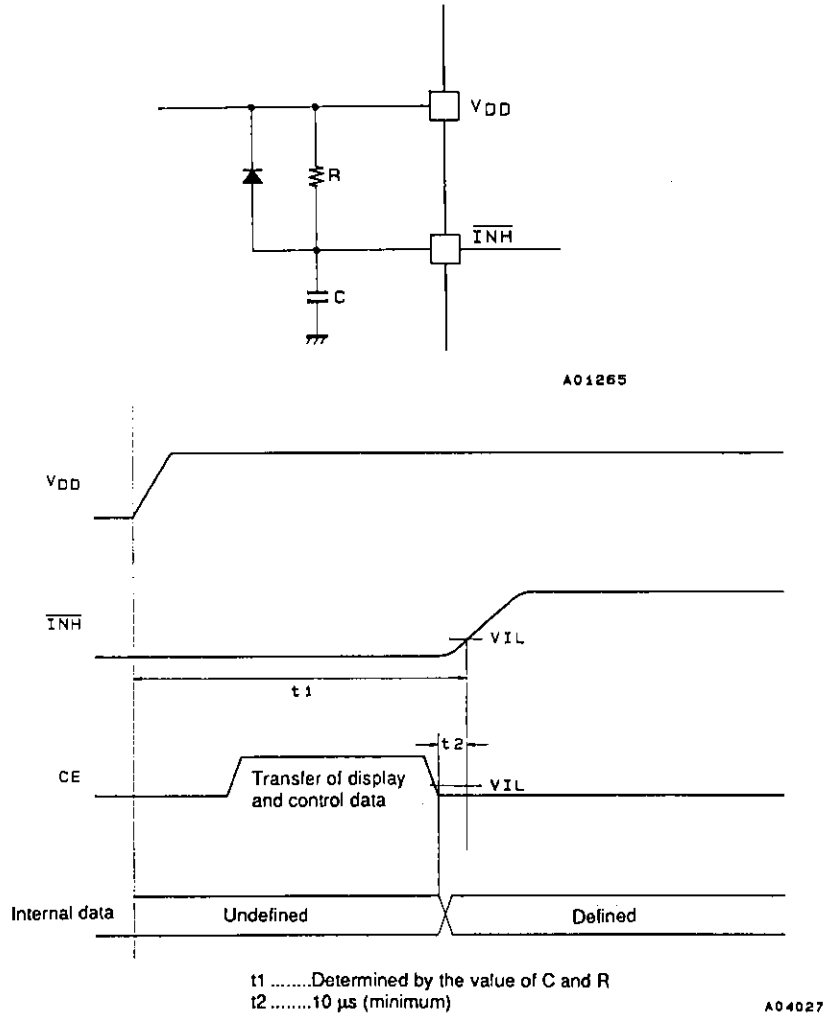
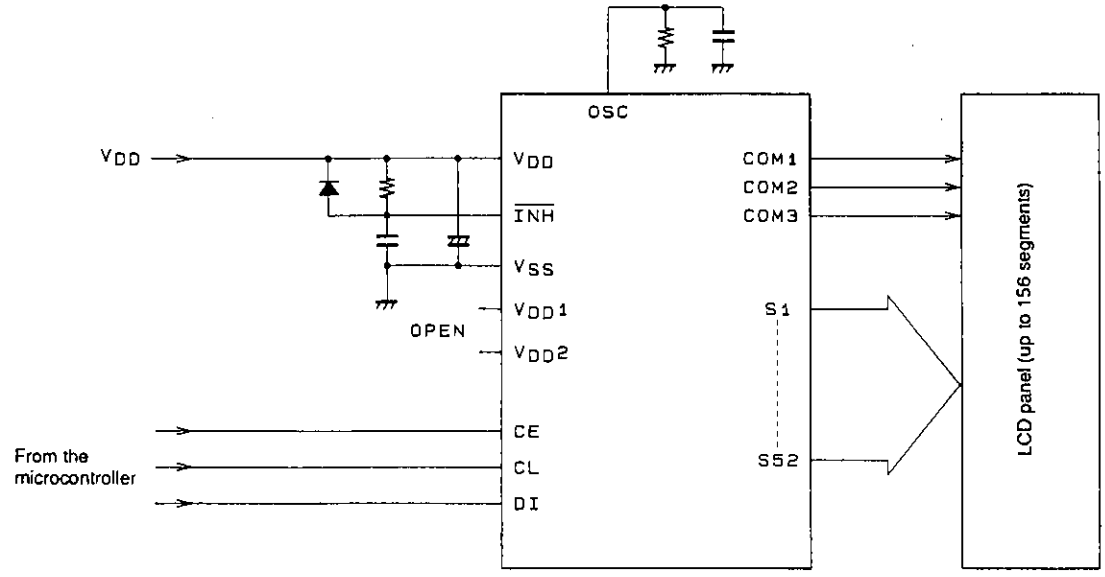


Figure 3

Sample Application Circuit 1

1/3 Bias (for use with small panels)



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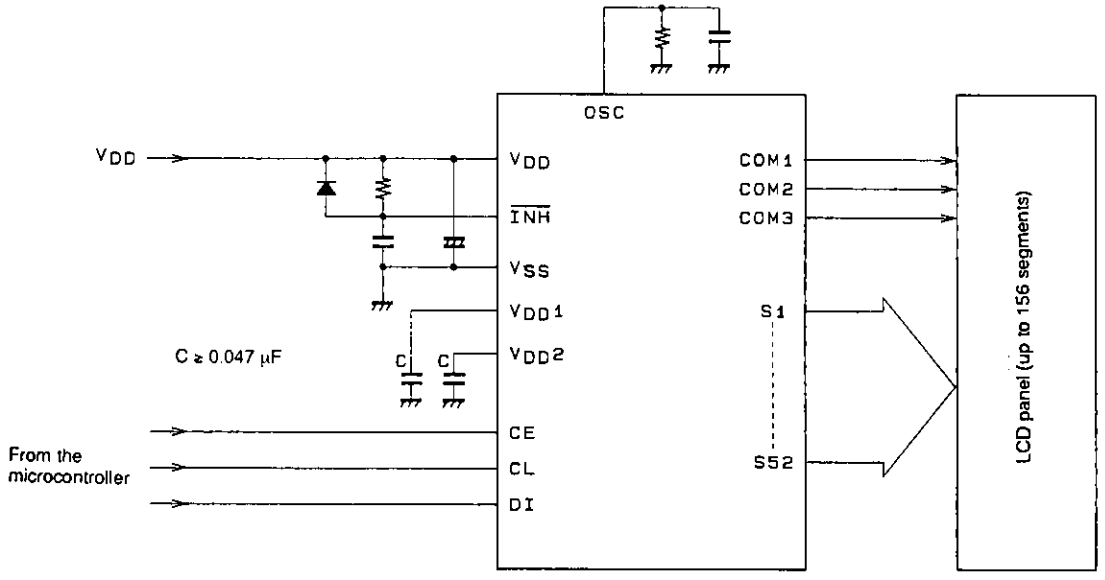
Sample Application Circuit 2

1/3 Bias (for use with normal size panels)



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Sample Application Circuit 3

1/3 Bias (for use with large panels)