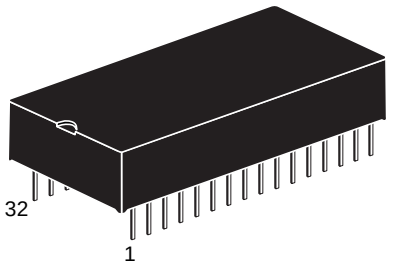
# M48Z129Y*
# M48Z129V

## 5.0V OR 3.3V, 1 Mbit (128 Kb x 8) ZEROPOWER® SRAM

### FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER
- MICROPROCESSOR POWER-ON RESET (RESET VALID EVEN DURING BATTERY BACK-UP MODE)
- BATTERY LOW PIN - PROVIDES WARNING OF BATTERY END-OF-LIFE
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES ($V_{PFD}$ = Power-fail Deselect Voltage):
  - M48Z129Y: $V_{CC}$ = 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
  - M48Z129V: $V_{CC}$ = 3.0 to 3.6V
    $2.7V \leq V_{PFD} \leq 3.0V$
- SELF-CONTAINED BATTERY IN THE CAPHAT™ DIP PACKAGE
- PIN and FUNCTION COMPATIBLE WITH JEDEC STANDARD 128K x 8 SRAMs

**Figure 1. 32-pin PMDIP Module**




PMDIP32 (PM)
Module

* Contact Local Sales Office

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## SUMMARY DESCRIPTION

The M48Z129Y/V ZEROPOWER® SRAM is a 1,048,576 bit non-volatile static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32-pin DIP Module. The M48Z129Y/V directly replaces industry standard 128K x 8 SRAM. It also provides the non-volatility of FLASH without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

**Figure 2. Logic Diagram**

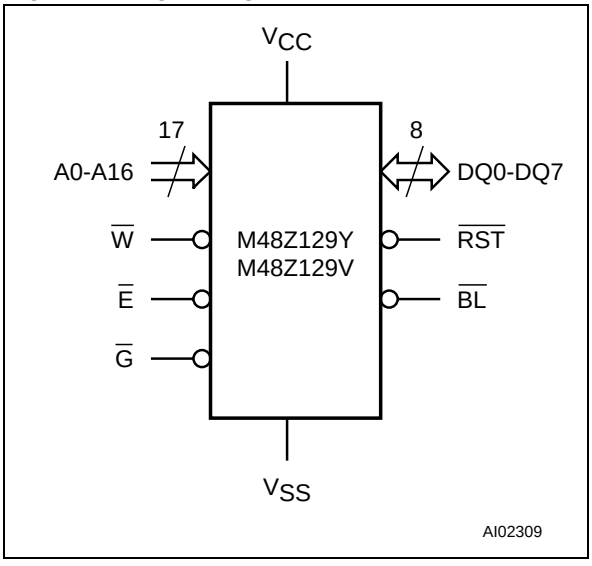



**Table 1. Signal Names**

| | |
|---|---|
| A0-A16 | Address Inputs |
| DQ0-DQ7 | Data Inputs / Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | WRITE Enable |
| $\overline{RST}$ | Reset Output (Open Drain) |
| $\overline{BL}$ | Battery Low Output (Open Drain) |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 3. DIP Connections**

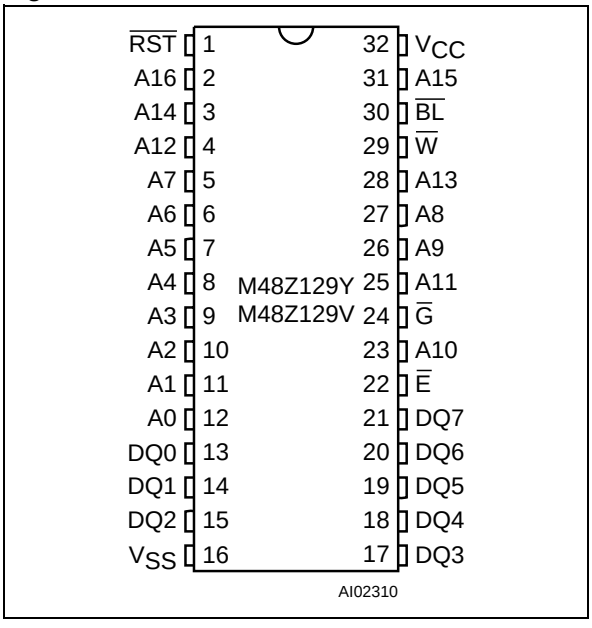
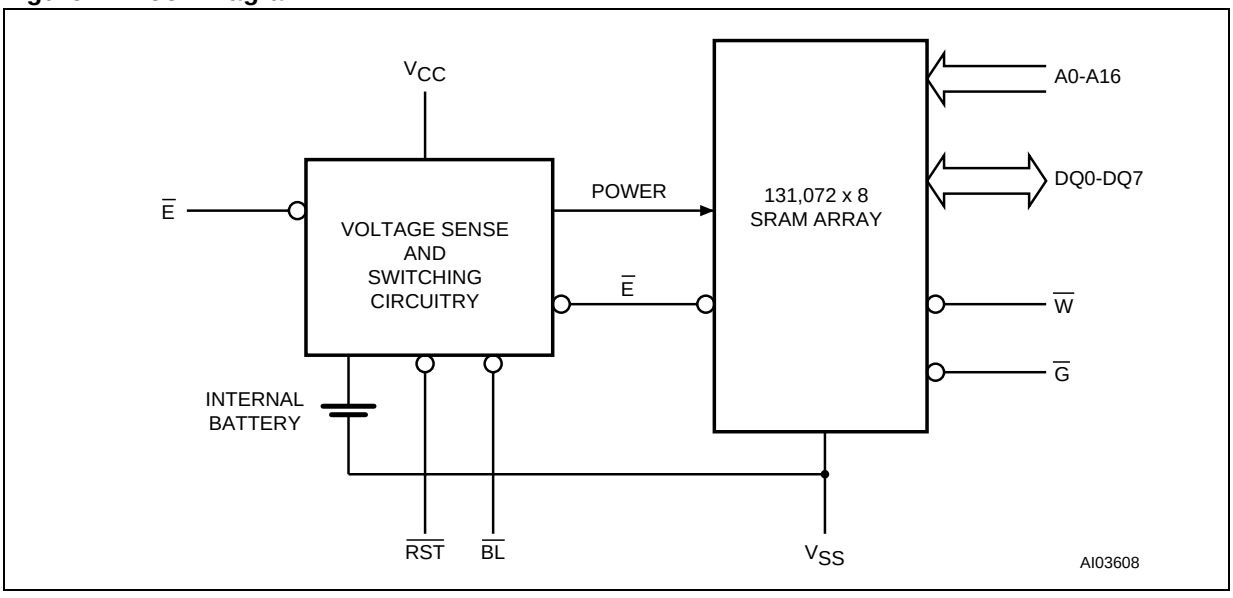


**Figure 4. Block Diagram**




## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$ Off, Oscillator Off) | –40 to 85 | °C |
| $T_{SLD}$(1) | Lead Solder Temperature for 10 seconds | 260 | °C |
| $V_{IO}$ | Input or Output Voltages | –0.3 to 7 | V |
| $V_{CC}$ | Supply Voltage | –0.3 to 7 | V |
| $I_O$ | Output Current | 20 | mA |
| $P_D$ | Power Dissipation | 1 | W |

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

***CAUTION:*** *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

## DC AND AC PARAMETERS

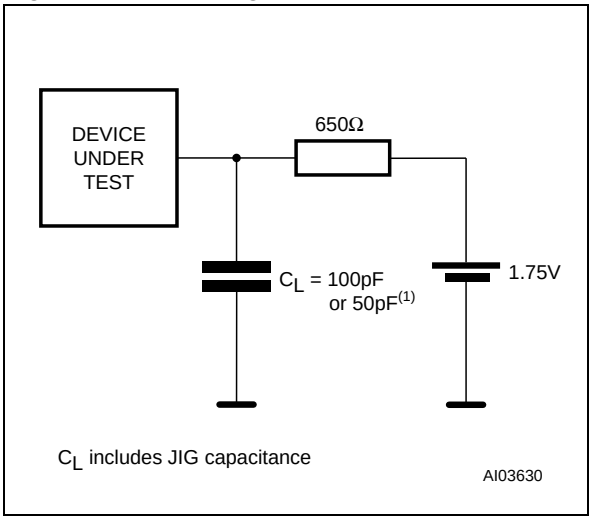
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. Operating and AC Measurement Conditions**

| Parameter | M48Z129Y | M48Z129V | Unit |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 4.5 to 5.5 | 3.0 to 3.6 | V |
| Ambient Operating Temperature ($T_A$) | 0 to 70 | 0 to 70 | °C |
| Load Capacitance ($C_L$) | 100 | 50 | pF |
| Input Rise and Fall Times | ≤ 5 | ≤ 5 | ns |
| Input Pulse Voltages | 0 to 3 | 0 to 3 | V |
| Input and Output Timing Ref. Voltages | 1.5 | 1.5 | V |

Note: Output Hi-Z is defined as the point where data is no longer driven.

**Figure 5. AC Testing Load Circuit**




Note: 1. 50pF for M48Z129V (3.3V).

**Table 4. Capacitance**

| Symbol | Parameter(1,2) | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF |
| $C_{IO}$(3) | Input / Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

**Table 5. DC Characteristics**

| Sym | Parameter | Test Condition(1) | M48Z129Y | | M48Z129V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –70 | | –85 | | |
| | | | Min | Max | Min | Max | |
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | ±1 | | ±1 | µA |
| $I_{LO}$(2) | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply Current | Outputs open | | 95 | | 50 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | 7 | | 4 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E} = V_{CC} - 0.2V$ | | 4 | | 3 | mA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | –0.3 | 0.6 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ + 0.3 | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1mA | 2.4 | | 2.2 | | V |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. Outputs deselected.

## OPERATION MODES

The M48Z129Y/V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When $V_{CC}$ is out of tolerance, the circuit write protects the SRAM, providing data security in the midst of unpredictable system operation. As $V_{CC}$ falls, the control circuitry automatically switches to the battery, maintaining data until valid power is restored.

**Table 6. Operating Modes**

| Mode | $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | DQ0-DQ7 | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.5 to 5.5V or 3.0to 3.6V | $V_{IH}$ | X | X | High Z | Standby |
| WRITE | | $V_{IL}$ | X | $V_{IL}$ | $D_{IN}$ | Active |
| READ | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Active |
| READ | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High Z | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min)(1) | X | X | X | High Z | CMOS Standby |
| Deselect | $\le V_{SO}$(1) | X | X | X | High Z | Battery Back-up Mode |

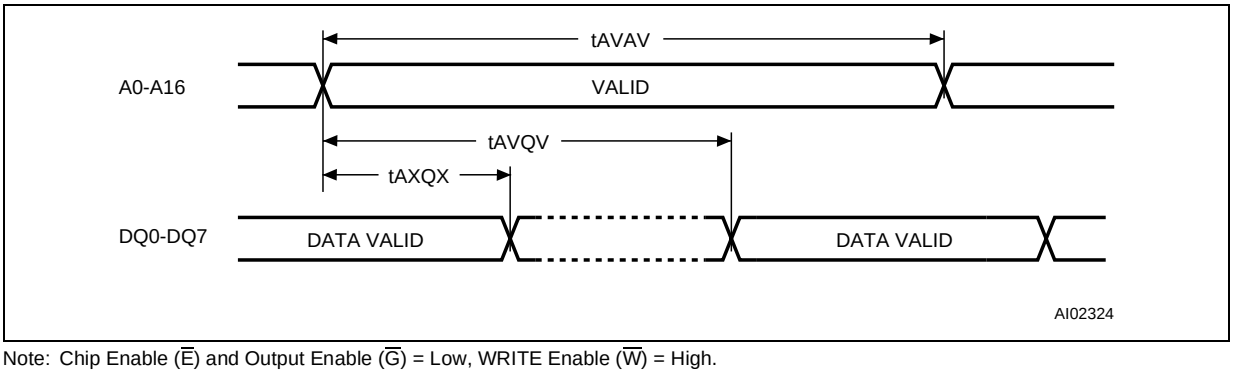
Note: X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage.
1. See Table 10, page 12 for details.

### READ Mode

The M48Z129Y/V is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within $t_{AVQV}$ (Address Access Time) after the last address input signal is stable, providing the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times ($t_{ELQV}$) or Output Enable Access Time ($t_{GLQV}$).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before $t_{AVQV}$, the data lines will be driven to an indeterminate state until $t_{AVQV}$. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for $t_{AXQX}$ (Output Data Hold Time) but will go indeterminate until the next Address Access.

**Figure 6. Address Controlled, READ Mode AC Waveforms**




Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = Low, WRITE Enable ($\overline{W}$) = High.

**Figure 7. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms**

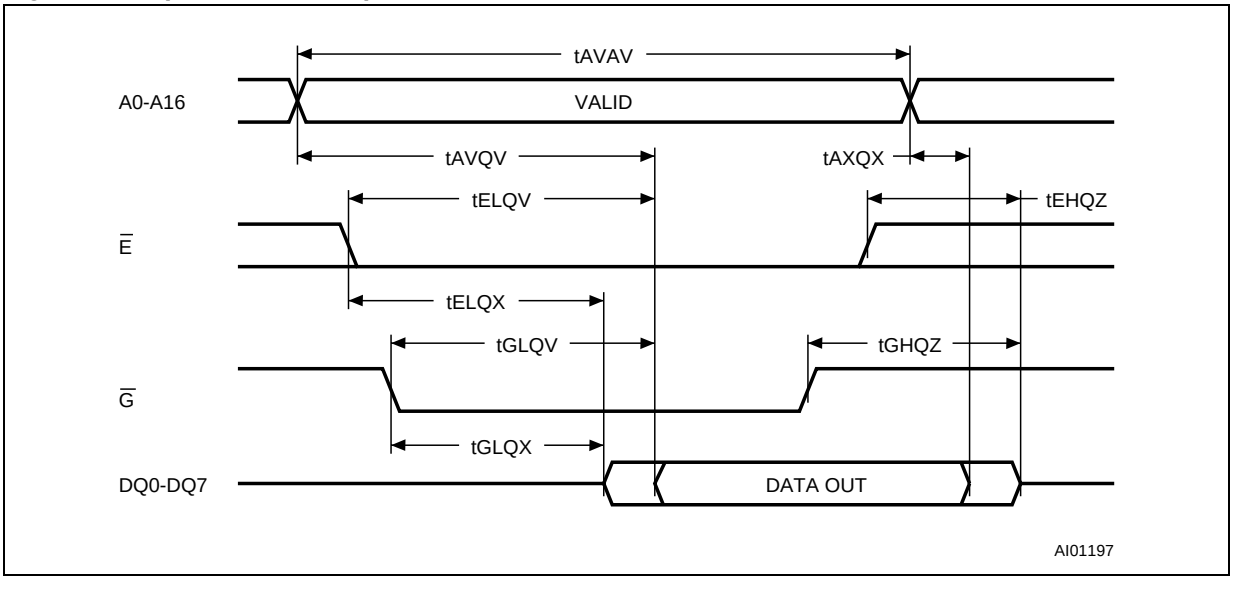


**Table 7. READ Mode AC Characteristics**

| Symbol | Parameter[1] | M48Z129Y | | M48Z129V | | Unit |
|---|---|---|---|---|---|---|
| | | –70 | | –85 | | |
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | READ Cycle Time | 70 | | 85 | | ns |
| $t_{AVQV}$ | Address Valid to Output Valid | | 70 | | 85 | ns |
| $t_{ELQV}$ | Chip Enable Low to Output Valid | | 70 | | 85 | ns |
| $t_{GLQV}$ | Output Enable Low to Output Valid | | 35 | | 45 | ns |
| $t_{ELQX}$[2] | Chip Enable Low to Output Transition | 5 | | 5 | | ns |
| $t_{GLQX}$[2] | Output Enable Low to Output Transition | 3 | | 5 | | ns |
| $t_{EHQZ}$[2] | Chip Enable High to Output Hi-Z | | 30 | | 40 | ns |
| $t_{GHQZ}$[2] | Output Enable High to Output Hi-Z | | 20 | | 25 | ns |
| $t_{AXQX}$ | Address Transition to Output Transition | 5 | | 5 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $C_L$ = 5pF (see Figure 5, page 5).

### WRITE Mode

The M48Z129Y/V is in the WRITE Mode whenever $\overline{W}$ (WRITE Enable) and $\overline{E}$ (Chip Enable) are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of $t_{EHAX}$ from Chip Enable or $t_{WHAX}$ from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid $t_{DVWH}$ prior to the end of WRITE and remain valid for $t_{WHDX}$ afterward. G should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and G a low on $\overline{W}$ will disable the outputs $t_{WLQZ}$ after $\overline{W}$ falls.

**Figure 8. WRITE Enable Controlled, WRITE Mode AC Waveform**

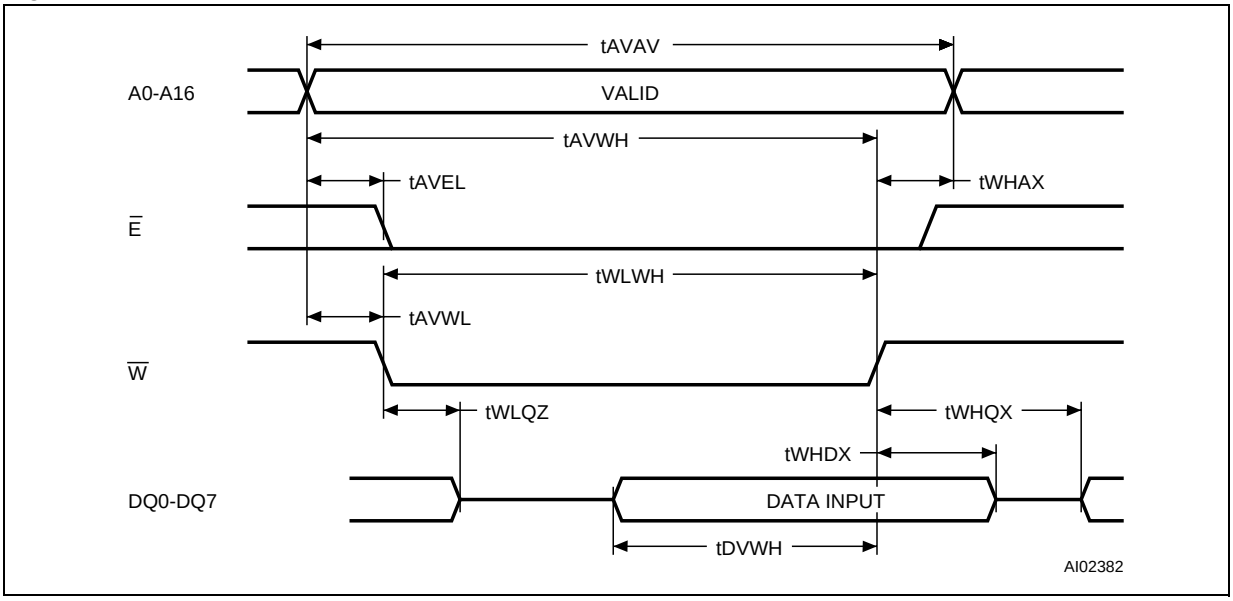



**Figure 9. Chip Enable Controlled, WRITE Mode AC Waveforms**

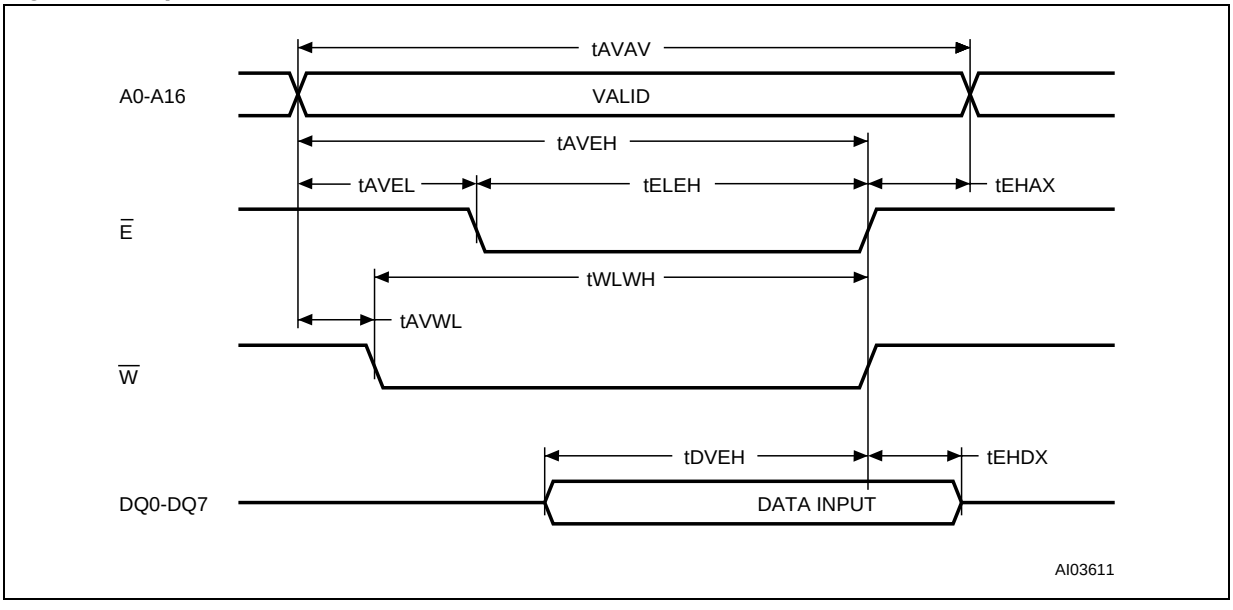


**Table 8. WRITE Mode AC Characteristics**

| Symbol | Parameter[1] | M48Z129Y | | M48Z129V | | Unit |
|---|---|---|---|---|---|---|
| | | –70 | | –85 | | |
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | WRITE Cycle Time | 70 | | 85 | | ns |
| $t_{AVWL}$ | Address Valid to WRITE Enable Low | 0 | | 0 | | ns |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | 0 | | ns |
| $t_{WLWH}$ | WRITE Enable Pulse Width | 55 | | 65 | | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 55 | | 75 | | ns |
| $t_{WHAX}$ | WRITE Enable High to Address Transition | 5 | | 5 | | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 15 | | 15 | | ns |
| $t_{DVWH}$ | Input Valid to WRITE Enable High | 30 | | 35 | | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 30 | | 35 | | ns |
| $t_{WHDX}$ | WRITE Enable High to Input Transition | 0 | | 0 | | ns |
| $t_{EHDX}$ | Chip Enable High to Input Transition | 10 | | 15 | | ns |
| $t_{WLQZ}$[2,3] | WRITE Enable Low to Output Hi-Z | | 25 | | 30 | ns |
| $t_{AVWH}$ | Address Valid to WRITE Enable High | 65 | | 75 | | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 65 | | 75 | | ns |
| $t_{WHQX}$[2,3] | WRITE Enable High to Output Transition | 5 | | 5 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $C_L$ = 5pF (see Figure 5, page 5).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

### Data Retention Mode

With valid $V_{CC}$ applied, the M48Z129Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when $V_{CC}$ falls between $V_{PFD}$ (max), $V_{PFD}$ (min) window. All outputs become high impedance and all inputs are treated as “Don’t care”.

**Note:** A power failure during a WRITE cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM’s content. At voltages below $V_{PFD}$(min), the memory will be in a write protected state, provided the $V_{CC}$ fall time is not less than $t_F$. The M48Z129Y/V may respond to transient noise spikes on $V_{CC}$ that cross into the deselect window during the time the device is sampling $V_{CC}$. Therefore, decoupling of the power supply lines is recommended.

When $V_{CC}$ drops below $V_{SO}$, the control circuit switches power to the internal battery, preserving data. The internal energy source will maintain data in the M48Z129Y/V for an accumulated period of at least 10 years at room temperature. As system power rises above $V_{SO}$, the battery is disconnected, and the power supply is switched to external $V_{CC}$. Deselect continues for $t_{REC}$ after $V_{CC}$ reaches $V_{PFD}$(max).

For more information on Battery Storage Life refer to the Application Note AN1012.

**Figure 10. Power Down/Up Mode AC Waveforms**

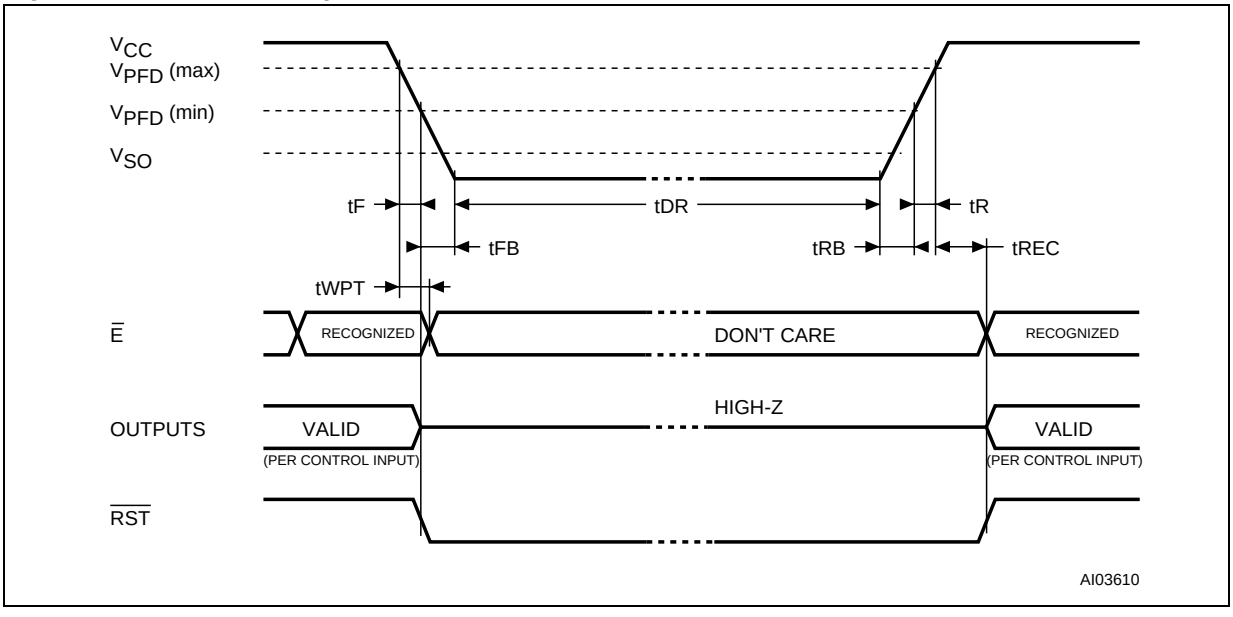


**Table 9. Power Down/Up AC Characteristics**

| Symbol | Parameter[1] | | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_F$[2] | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | | 300 | | µs |
| $t_{FB}$[3] | $V_{PFD}$ (min) to $V_{SS}$ $V_{CC}$ Fall Time | M48Z129Y | 10 | | µs |
| | | M48Z129V | 150 | | |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | | 10 | | µs |
| $t_{RB}$ | $V_{SS}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | | 1 | | µs |
| $t_{WPT}$ | Write Protect Time | M48Z129Y | 40 | 150 | µs |
| | | M48Z129V | 40 | 250 | |
| $t_{REC}$ | $V_{PFD}$ (max) to $\overline{RST}$ High | | 40 | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than tF may result in deselection/write protection not occurring until 200µs after $V_{CC}$ passes $V_{PFD}$ (min).
3. $V_{PFD}$ (min) to $V_{SS}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.

**Table 10. Power Down/Up Trip Points DC Characteristics**

| Symbol | Parameter[1,2] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage | M48Z129Y | 4.2 | 4.35 | 4.5 | V |
| | | M48Z129V | 2.7 | 2.9 | 3.0 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | M48Z129Y | | 3.0 | | V |
| | | M48Z129V | | 2.45 | | V |
| $t_{DR}$[3] | Expected Data Retention Time | | 10 | | | YEARS |

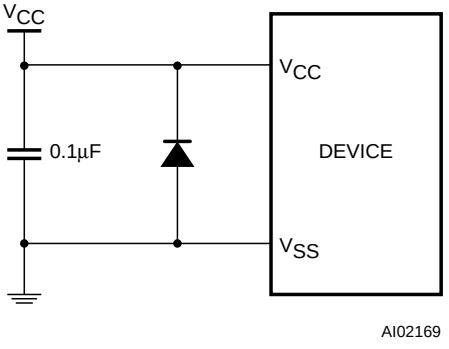
Note: 1. All voltages referenced to $V_{SS}$.
2. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
3. At 25°C, $V_{CC}$ = 0V.

### $V_{CC}$ Noise And Negative Going Transients

$I_{CC}$ transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the $V_{CC}$ bus. These transients can be reduced if capacitors are used to store energy which stabilizes the $V_{CC}$ bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 11) is recommended in order to provide the needed filtering.

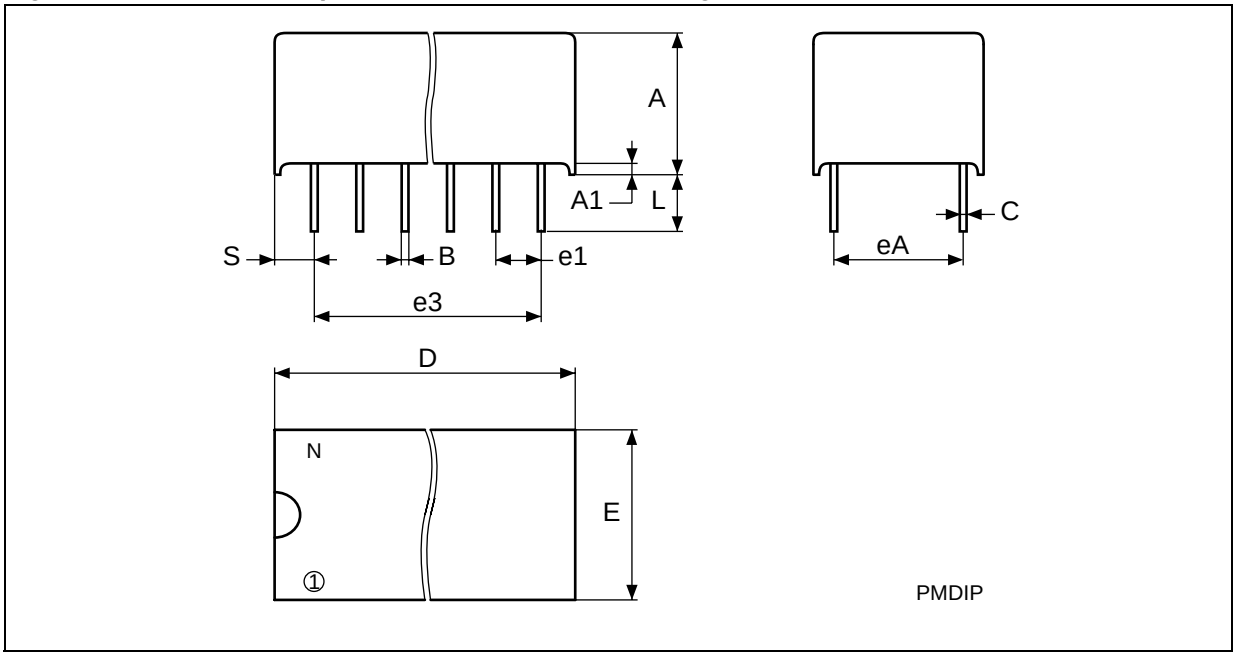
In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on $V_{CC}$ that drive it to values below $V_{SS}$ by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from $V_{CC}$ to $V_{SS}$ (cathode connected to $V_{CC}$, anode to $V_{SS}$). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Figure 11. Supply Voltage Protection**



## PACKAGE MECHANICAL INFORMATION

**Figure 12. PMDIP32 – 32-pin Plastic Module DIP, Package Outline**




Note: Drawing is not to scale.

**Table 11. PMDIP32 – 32-pin Plastic DIP, Package Mechanical Data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 9.27 | 9.52 | | 0.365 | 0.375 |
| A1 | | 0.38 | – | | 0.015 | – |
| B | | 0.43 | 0.59 | | 0.017 | 0.023 |
| C | | 0.20 | 0.33 | | 0.008 | 0.013 |
| D | | 42.42 | 43.18 | | 1.670 | 1.700 |
| E | | 18.03 | 18.80 | | 0.710 | 0.740 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | | 34.29 | 41.91 | | 1.350 | 1.650 |
| eA | | 14.99 | 16.00 | | 0.590 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| S | | 1.91 | 2.79 | | 0.075 | 0.110 |
| N | 32 | | | 32 | | |

## PART NUMBERING

### Table 12. Ordering Information Scheme

Example: M48Z 129Y –70 PM 1 TR

**Device Type**

M48Z

**Supply Voltage and Write Protect Voltage**

129Y[1] = $V_{CC}$ = 4.5 to 5.5V; 4.2V ≤ $V_{PFD}$ ≤ 4.5V

129V = $V_{CC}$ = 3.0 to 3.6V; 2.7V ≤ $V_{PFD}$ ≤ 3.0V

**Speed**

–70 = 70ns (M48Z129Y)

–85 = 85ns (M48Z129V)

**Package**

PM = PMDIP32

**Temperature Range**

1 = 0 to 70°C

**Shipping Method**

blank = Tubes

TR = Tape & Reel

Note: 1. Contact Local Sales Office

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest you.

## REVISION HISTORY

**Table 13. Document Revision History**

| Date | Rev. # | Revision Details |
|---|---|---|
| December 1999 | 1.0 | First Issue |
| 30-Mar-00 | 2.0 | From Preliminary Data to Data Sheet |
| 20-Jun-00 | 2.1 | $t_{GLQX}$ changed for M48Z129Y (Table 7) |
| 14-Sep-01 | 3.0 | Reformatted; Temperature information added to tables (Table 4, 5, 7, 8, 9, 10) |
| 29-May-02 | 3.1 | Add countries to disclaimer |
| 02-Apr-03 | 4.0 | v2.2 template applied; test condition updated (Table 10) |