M48Z58
M48Z58Y

5.0V, 64 Kbit (8 Kbit x 8) ZEROPOWER® SRAM

FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES:
  (V_{PFD} = Power-fail Deselect Voltage)
  - M48Z58: V_{CC} = 4.75 to 5.5V
    $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z58Y: 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
- SELF-CONTAINED BATTERY IN THE CAPHAT™ DIP PACKAGE
- PACKAGING INCLUDES A 28-LEAD SOIC and SNAPHAT® TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY
- PIN and FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K x 8 SRAMs
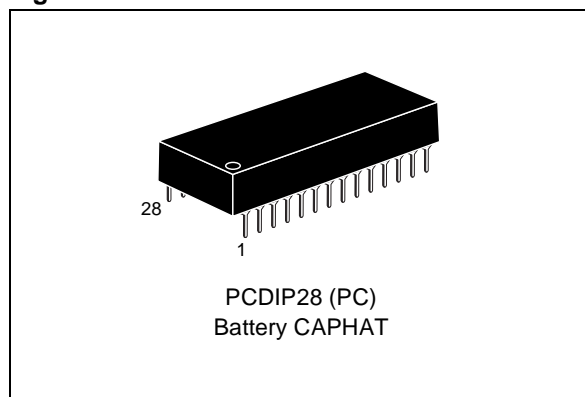
Figure 1. CAPHAT™ DIP Solution

PCDIP28 (PC)
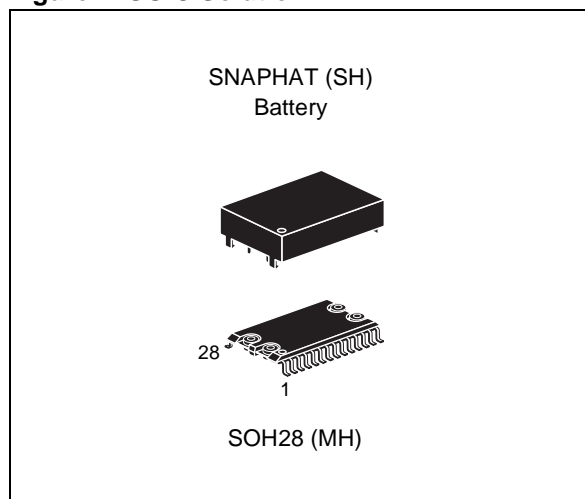Battery CAPHAT

Figure 2. SOIC Solution

SNAPHAT (SH)
Battery

SOH28 (MH)

TABLE OF CONTENTS

DESCRIPTION

The M48Z58/Y ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

The M48Z58/Y is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600mil DIP CAPHAT™ houses the M48Z58/Y silicon with a long life lithium button cell in a single package.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

For the 28-lead SOIC, the battery package (e.g., SNAPHAT) part number is "M4Z28-BR00SH" (see Table 16, page 17).

Figure 3. Logic Diagram
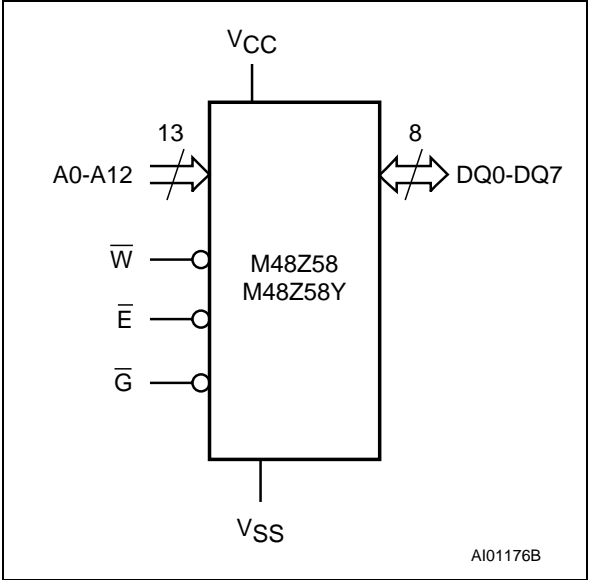
Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	WRITE Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 4. DIP Connections


```
        NC [ 1        28 ] VCC
       A12 [ 2        27 ] W̄
        A7 [ 3        26 ] NC
        A6 [ 4        25 ] A8
        A5 [ 5        24 ] A9
        A4 [ 6        23 ] A11
        A3 [ 7  M48Z58 22 ] Ḡ
        A2 [ 8  M48Z58Y 21 ] A10
        A1 [ 9        20 ] Ē
        A0 [ 10       19 ] DQ7
       DQ0 [ 11       18 ] DQ6
       DQ1 [ 12       17 ] DQ5
       DQ2 [ 13       16 ] DQ4
       VSS [ 14       15 ] DQ3
```
AI01177B
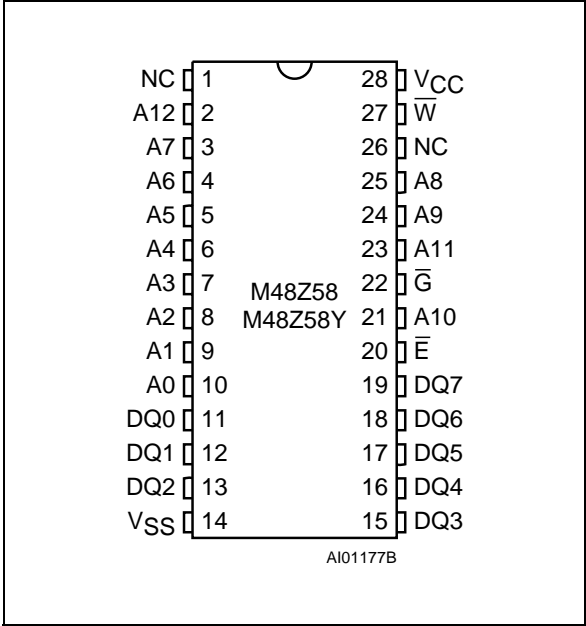
Figure 5. SOIC Connections


```
        NC ⊏ ①        28 ⊐ VCC
       A12 ⊏ 2        27 ⊐ W̄
        A7 ⊏ 3        26 ⊐ NC
        A6 ⊏ 4        25 ⊐ A8
        A5 ⊏ 5        24 ⊐ A9
        A4 ⊏ 6        23 ⊐ A11
        A3 ⊏ 7  M48Z58Y 22 ⊐ Ḡ
        A2 ⊏ 8        21 ⊐ A10
        A1 ⊏ 9        20 ⊐ Ē
        A0 ⊏ 10       19 ⊐ DQ7
       DQ0 ⊏ 11       18 ⊐ DQ6
       DQ1 ⊏ 12       17 ⊐ DQ5
       DQ2 ⊏ 13       16 ⊐ DQ4
       VSS ⊏ 14       15 ⊐ DQ3
```
AI01178B

Figure 6. Block Diagram

LITHIUM CELL

VOLTAGE SENSE AND SWITCHING CIRCUITRY

POWER

V_{PFD}

8K x 8 SRAM ARRAY

A0-A12

DQ0-DQ7

Ē

W̄

Ḡ

V_{CC}

V_{SS}

AI01394

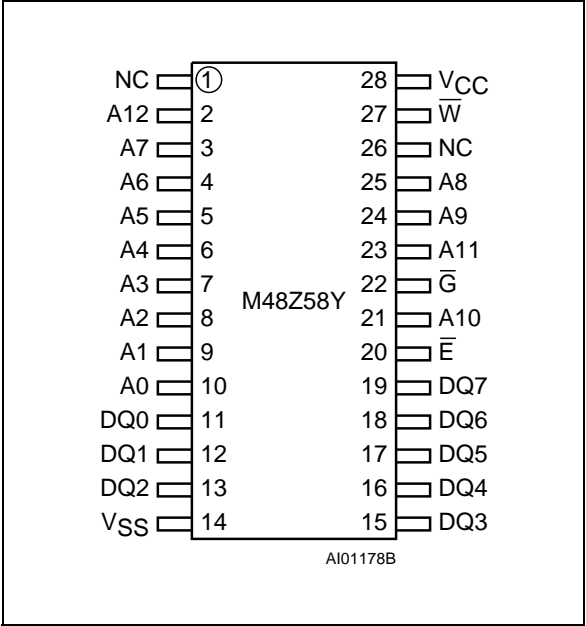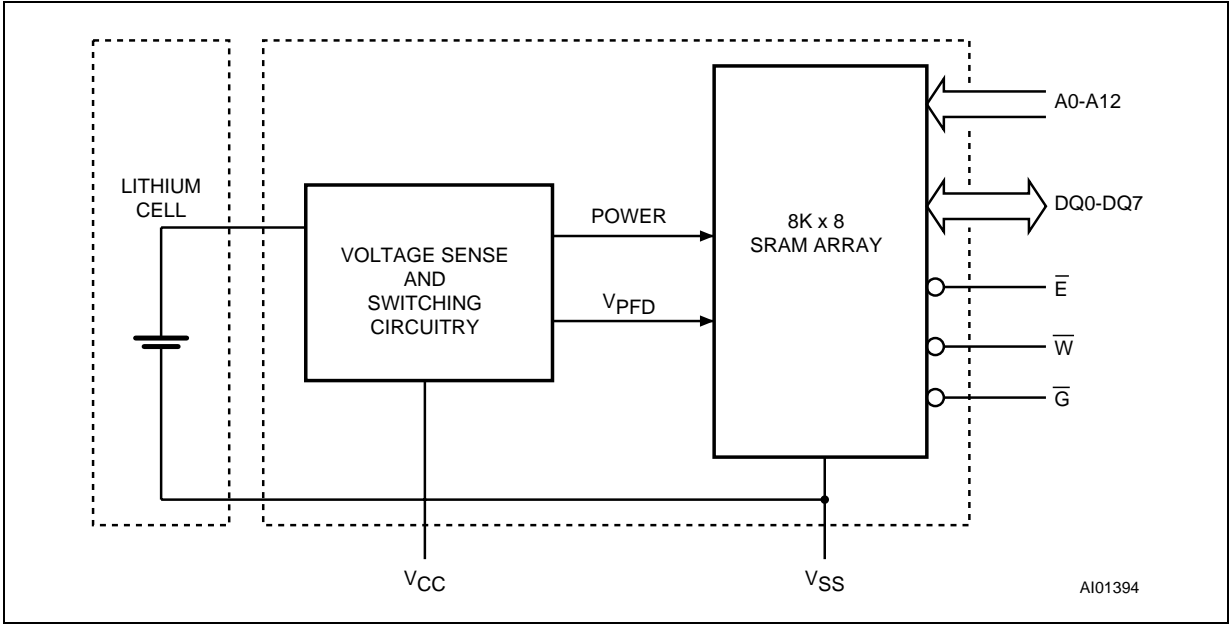**MAXIMUM RATING**

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Grade 1	0 to 70	°C
		Grade 6	−40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	SNAPHAT®	−40 to 85	°C
		SOIC	−55 to 125	°C
T_{SLD}[1,2]	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages		−0.3 to 7.0	V
V_{CC}	Supply Voltage		−0.3 to 7.0	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
2. For SO package: Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

CAUTION: Negative undershoots below −0.3V are not allowed on any pin while in the Battery Back-up mode.
Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter		M48Z58	M48Z58Y	Unit
Supply Voltage (V_{CC})		4.75 to 5.5V	4.5 to 5.5	V
Ambient Operating Temperature (T_A)	Grade 1	0 to 70	0 to 70	°C
	Grade 6	–40 to 85	–40 to 85	°C
Load Capacitance (C_L)		100	100	pF
Input Rise and Fall Times		≤ 5	≤ 5	ns
Input Pulse Voltages		0 to 3	0 to 3	V
Input and Output Timing Ref. Voltages		1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.
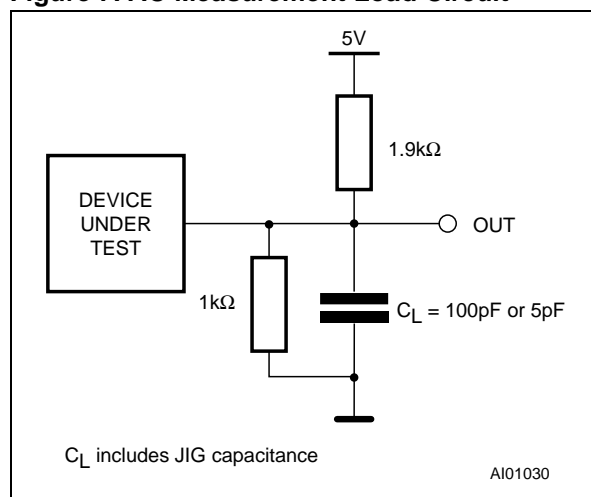
Figure 7. AC Measurement Load Circuit

C_L includes JIG capacitance

AI01030

Table 4. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		10	pF
C_{IO}[3]	Input / Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 5V. Sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition[1]	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}[2]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}[3]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per cycle.

OPERATING MODES

The M48Z58/Y also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below battery switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data until valid power returns.

Table 6. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5V or 4.5 to 5.5V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)[1]	X	X	X	High Z	CMOS Standby
Deselect	$\le V_{SO}$[1]	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.
1. See Table 10, page 12 for details.

READ Mode

The M48Z58/Y is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high, $\overline{E}$ (Chip Enable) is low. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Figure 8. READ Mode AC Waveforms
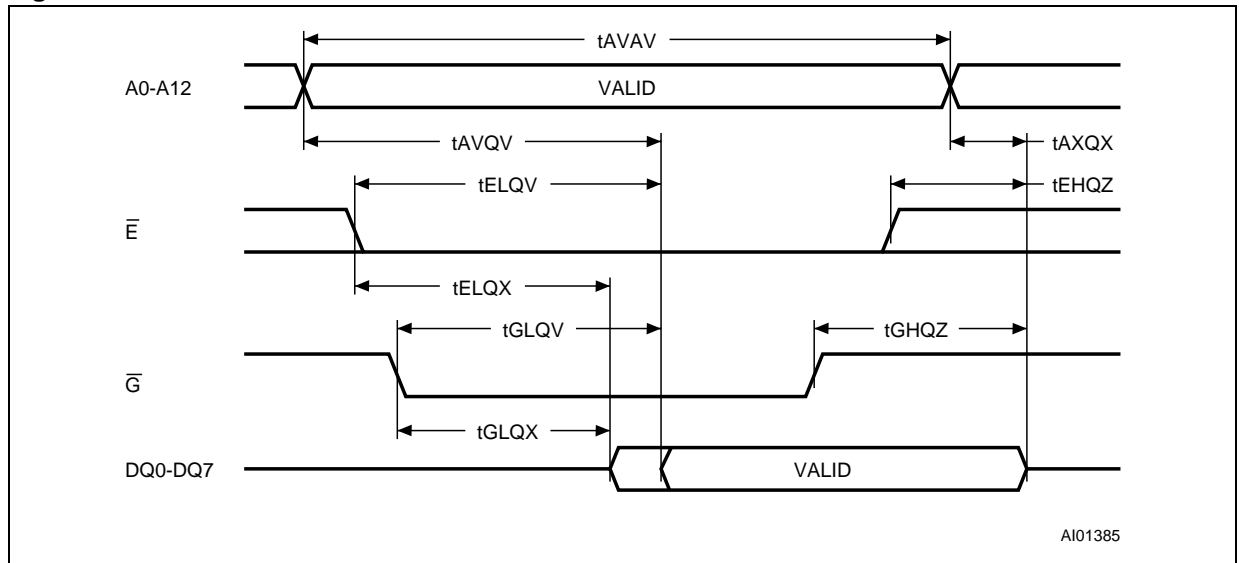
Note: WRITE Enable ($\overline{W}$) = High.

Table 7. READ Mode AC Characteristics

Symbol	Parameter[1]	M48Z58/Y		Unit
		Min	Max	
t_{AVAV}	READ Cycle Time	70		ns
t_{AVQV}	Address Valid to Output Valid		70	ns
t_{ELQV}	Chip Enable Low to Output Valid		70	ns
t_{GLQV}	Output Enable Low to Output Valid		35	ns
t_{ELQX}[2]	Chip Enable Low to Output Transition	5		ns
t_{GLQX}[2]	Output Enable Low to Output Transition	5		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		25	ns
t_{AXQX}	Address Transition to Output Transition	10		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 5pF (see Figure 7, page 6).

WRITE Mode

The M48Z58/Y is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

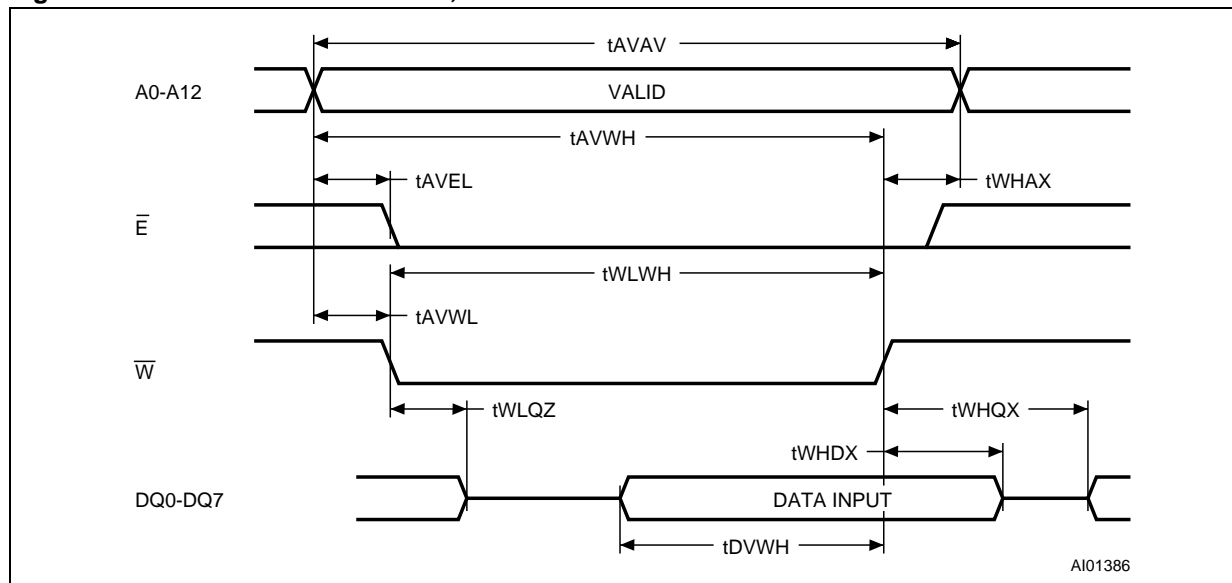**Figure 9. WRITE Enable Controlled, WRITE Mode AC Waveforms**

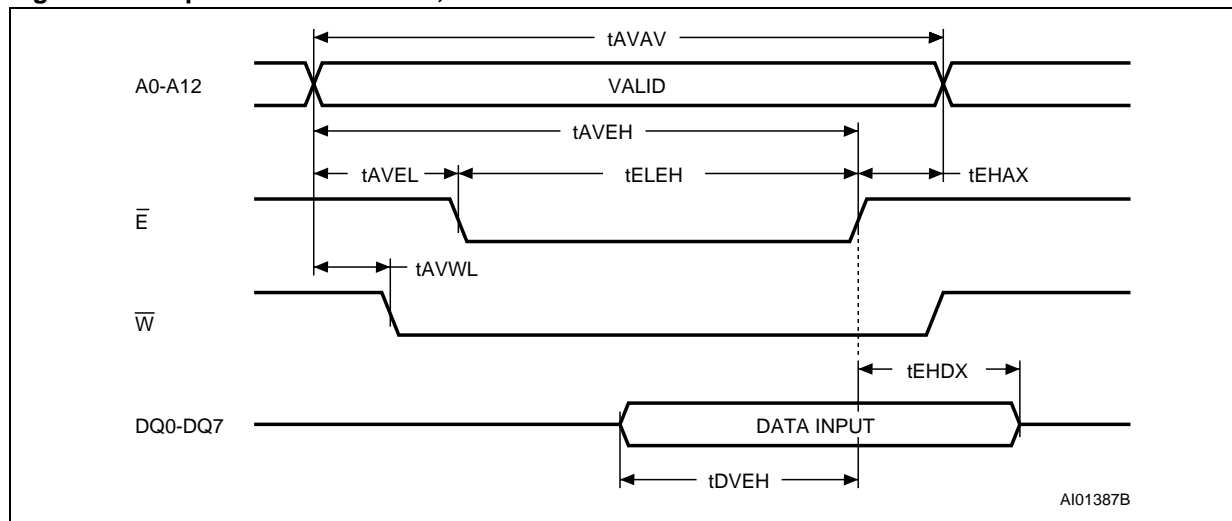**Figure 10. Chip Enable Controlled, WRITE Mode AC Waveforms**

Table 8. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M48Z58/Y		Unit
		Min	Max	
t_{AVAV}	WRITE Cycle Time	70		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	WRITE Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	WRITE Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to WRITE Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	WRITE Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to WRITE Enable High	60		ns
t_{AVEH}	Address Valid to Chip Enable High	60		ns
t_{WHQX}[2,3]	WRITE Enable High to Output Transition	5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 5pF (see Figure 7, page 6).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48Z58/Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as "Don't care."

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z58/Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. There-fore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z58/Y for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max).

For more information on Battery Storage Life refer to the Application Note AN1012.
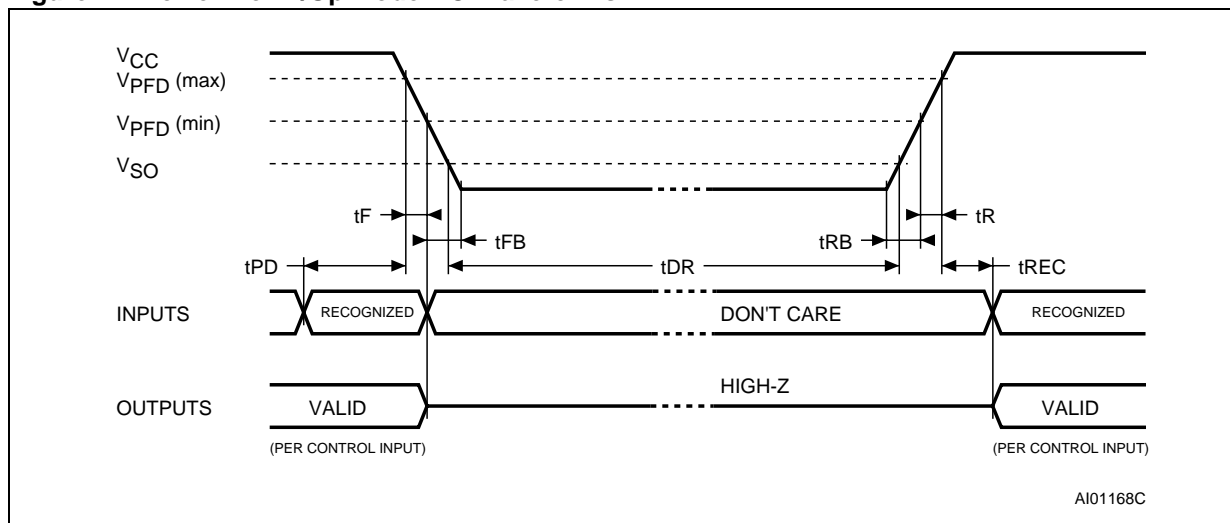
Figure 11. Power Down/Up Mode AC Waveforms

Table 9. Power Down/Up AC Characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}[4]	V_{PFD} (max) to Inputs Recognized	40	200	ms

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. t_{REC} (min) = 20ms for industrial temperature Grade (6) device.

Table 10. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter[1,2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z58	4.5	4.6	4.75	V
		M48Z58Y	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage			3.0		V
t_{DR}[3]	Expected Data Retention Time		10			YEARS

Note: 1. All voltages referenced to V_{SS}.
    2. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
    3. At 25°C, V_{CC} = 0V.

**V_{CC} Noise And Negative Going Transients**

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (see Figure 12) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

Figure 12. Supply Voltage Protection

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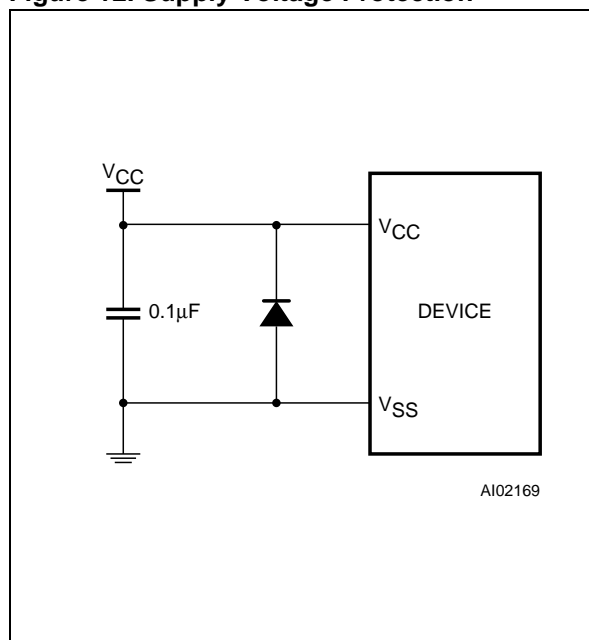
PACKAGE MECHANICAL INFORMATION

### Figure 13. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT™, Package Outline
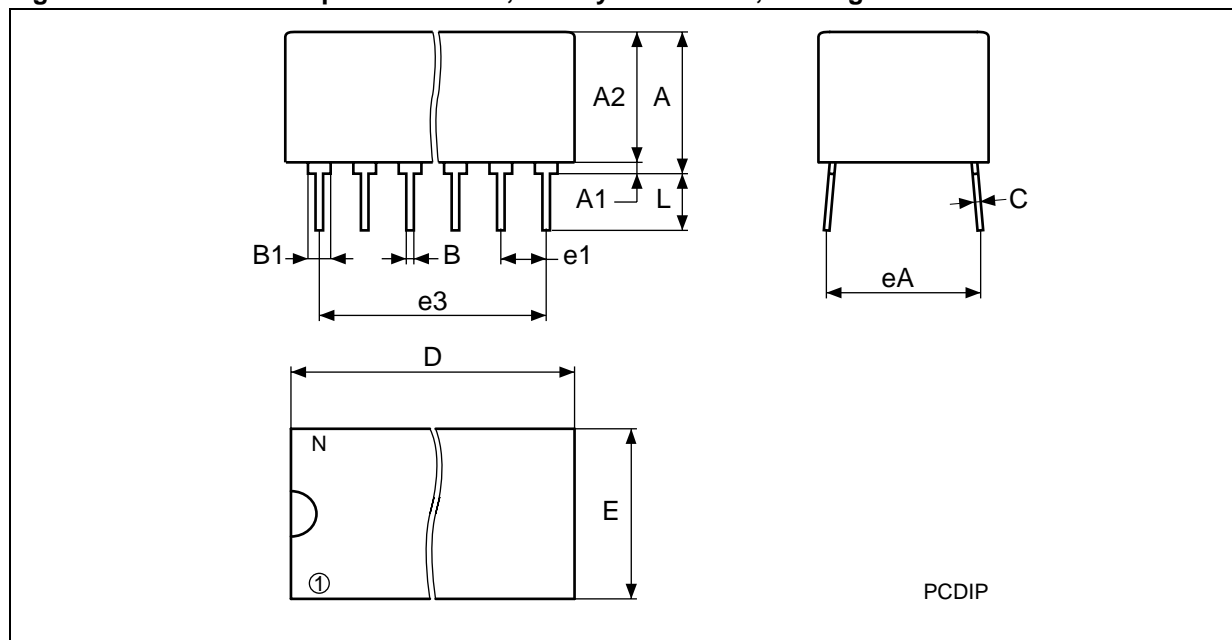
Note: Drawing is not to scale.

Table 11. PMDIP28 – 28-pin Plastic DIP, battery CAPHAT™, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

Figure 14. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Outline

SOH-A
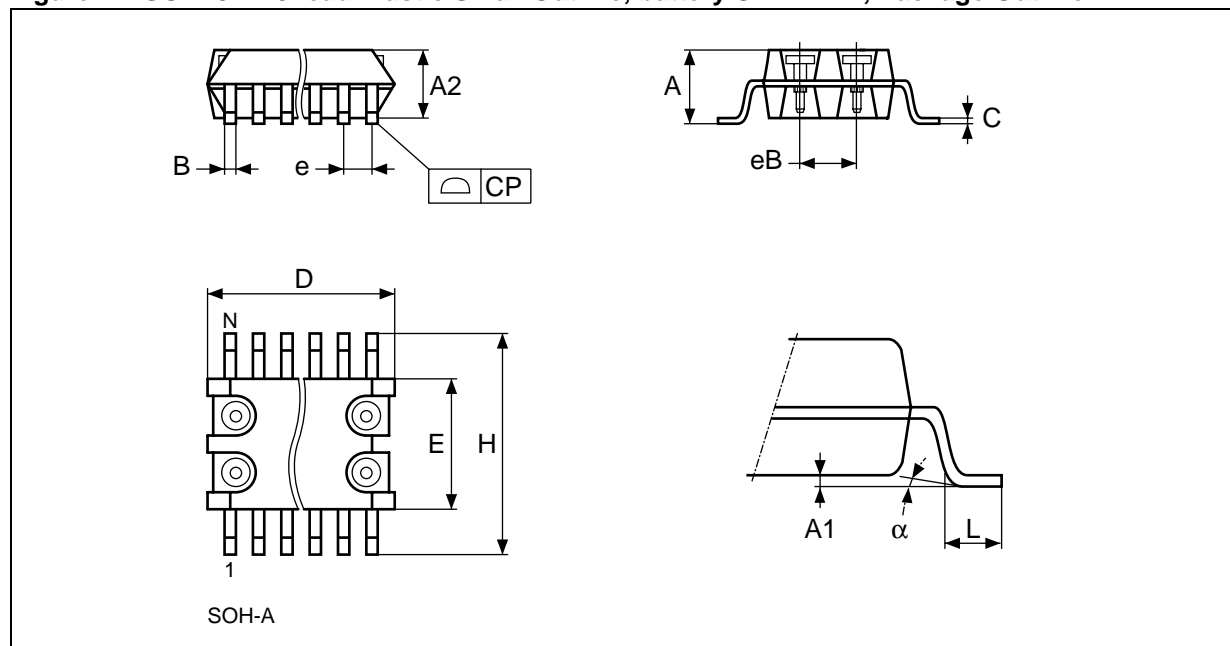
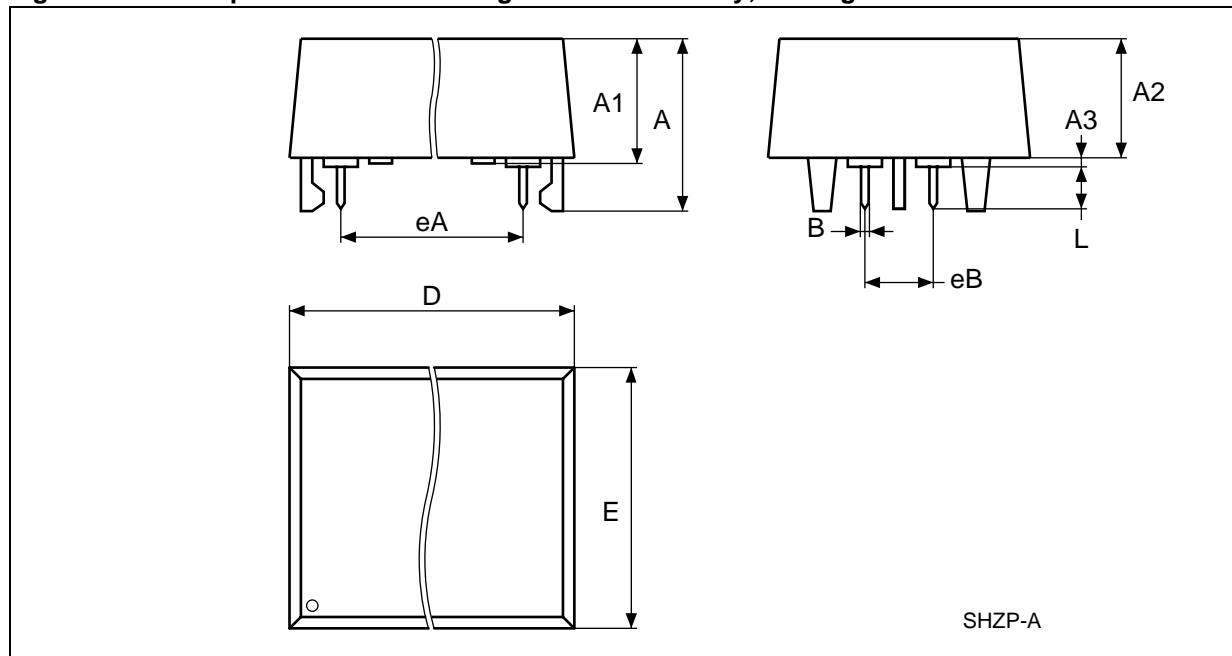Note: Drawing is not to scale.

Table 12. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inch		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

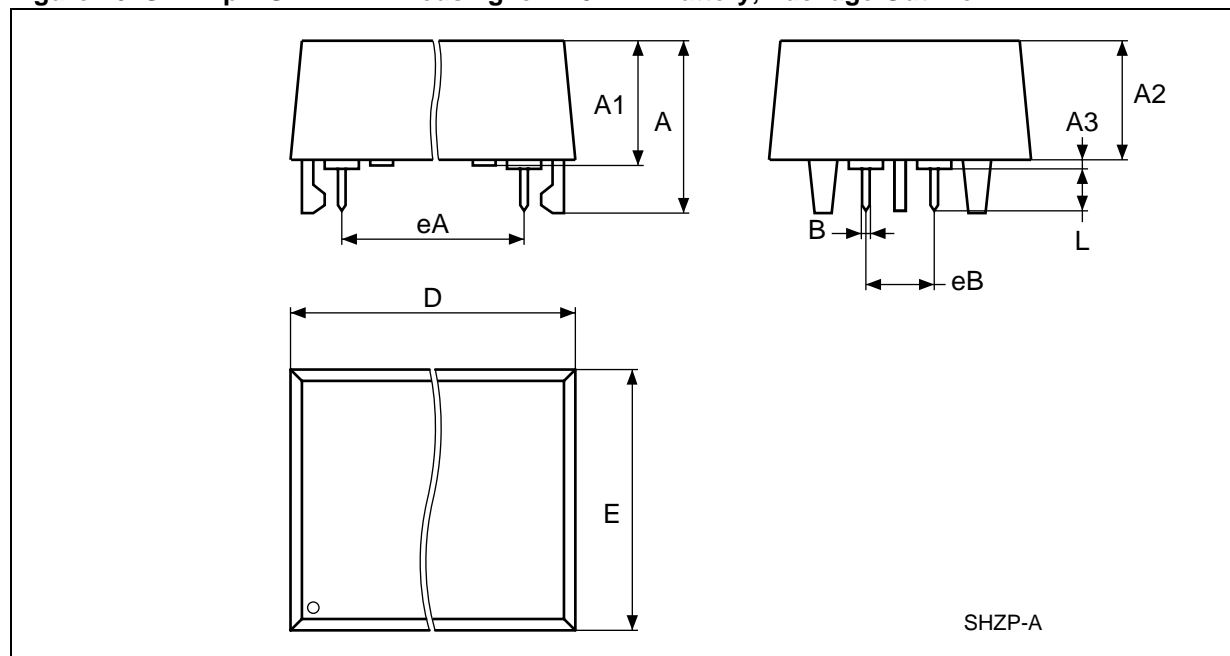**Figure 15. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Outline**

SHZP-A

Note: Drawing is not to scale.

Table 13. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 16. SH –4-pin SNAPHAT Housing for 120mAh Battery, Package Outline

SHZP-A

Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT Housing for 120mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

PART NUMBERING

Table 15. Ordering Information Scheme

Example: M48Z 58Y –70 MH 1 TR

Device Type

M48Z

Supply Voltage and Write Protect Voltage

$58^{(1)}$ = V_{CC} = 4.75 to 5.5V; V_{PFD} = 4.5 to 4.75V

58Y = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.2 to 4.5V

Speed

–70 = 70ns (for M48Z58/Y)

Package

PC = PCDIP28

$MH^{(2)}$ = SOH28

Temperature Range

1 = 0 to 70°C

6 = –40 to 85°C

Shipping Method for SOIC

blank = Tubes

TR = Tape & Reel

Note: 1. The M48Z58 part is offered with the PCDIP28 (i.e. CAPHAT™) package only.
2. The SOIC package (SOH28) requires the battery package (SNAPHAT®) which is ordered separately under the part number "M4Zxx-BR00SH" in plastic tube or "M4Zxx-BR00SHTR" in Tape & Reel form.

Caution: Do not place the SNAPHAT battery package "M4Zxx-BR00SH" in conductive foam as it will drain the lithium button-cell battery.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 16. SNAPHAT Battery Table

Part Number	Description	Package
M4Z28-BR00SH	Lithium Battery (48mAh) SNAPHAT	SH
M4Z32-BR00SH	Lithium Battery (120mAh) SNAPHAT	SH

REVISION HISTORY

Table 17. Revision History

Date	Rev. #	Revision Details
March 1999	1.0	First Issue
10-Feb-00	1.1	2-socket SOH and 2-pin SH packages removed
22-Feb-00	1.2	Data Retention Mode paragraph changed
14-Sep-01	2.0	Reformatted; added temperature information (Table 4, 5, 7, 8, 9, 10)
29-May-02	2.1	Modify reflow time and temperature footnotes (Table 2)
16-Sep-02	2.2	Remove footnote from Ordering Information (Table 15)
02-Apr-03	3.0	v2.2 template applied; test condition updated (Table 10)

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