

Quad Line Driver with Three-State Outputs

Motorola's Quad EIA–422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three–state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typical 15 ns)
- TTL Compatible
- Single 5.0 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

MC3487

QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

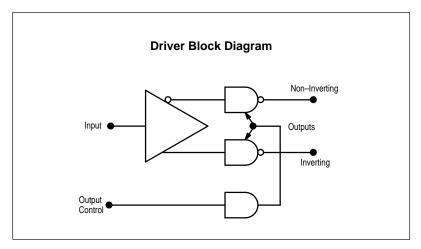
SEMICONDUCTOR TECHNICAL DATA

D SUFFIXPLASTIC PACKAGE
CASE 751B
(SO–16)





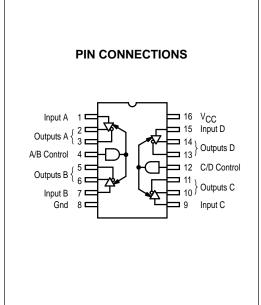
P SUFFIX
PLASTIC PACKAGE
CASE 648



TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
Н	Н	Н	<u>L</u>
L	Н	L	H
Х	L	Z	Z

- L = Low Logic State
- H = High Logic State
- X = Irrelevant
- Z = Third-State (High Impedance)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3487P	$T_A = 0 \text{ to } +70^{\circ}\text{C}$	Plastic DIP
MC3487D	1A = 0 10 +70 C	SO-16

MC3487

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	VCC	8.0	Vdc
Input Voltage	VI	5.5	Vdc
Operating Ambient Temperature Range	TA	0 to +70	°C
Operating Junction Temperature Range	TJ	150	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

 $\textbf{ELECTRICAL CHARACTERISTICS} \text{ (Unless otherwise noted, specifications apply } 4.75 \text{ V} \leqslant \text{V}_{CC} \leqslant 5.25 \text{ V} \text{ and } 0^{\circ}\text{C} \leqslant \text{T}_{A} \leqslant 70^{\circ}\text{C}.$ Typical values measured at VCC = 5.0 V, and TA = 25°C.)

Characteristic	Symbol	Min	Тур	Max	Unit
Input Voltage – Low Logic State	V _{IL}	-	_	0.8	Vdc
Input Voltage – High Logic State	VIH	2.0	_	_	Vdc
Input Current – Low Logic State (V _{IL} = 0.5 V)	IIL	_	-	- 400	μА
Input Current – High Logic State (V _{IH} = 2.7 V) (V _{IH} = 5.5 V)	IIH		- -	+ 50 + 100	μΑ
Input Clamp Voltage (I _{IK} = -18 mA)	VIK	_	-	- 1.5	V
Output Voltage – Low Logic State (I _{OL} = 48 mA)	VOL	-	_	0.5	V
Output Voltage – High Logic State (I _{OH} = -20 mA)	VOH	2.5	-	-	V
Output Short–Circuit Current (V _{IH} = 2.0 V, Note 1)	los	- 40	-	- 140	mA
Output Leakage Current – Hi–Z State (V _{IL} = 0.5 V, V _{IL} (Z) = 0.8 V) (V _{IH} = 2.7 V, V _{IL} (Z) = 0.8 V)	l _{OL(Z)}	- -	_ _	± 100 ± 100	μА
Output Leakage Current – Power OFF $(V_{OH} = 6.0 \text{ V}, V_{CC} = 0 \text{ V})$ $(V_{OL} = -0.25 \text{ V}, V_{CC} = 0 \text{ V})$	I _{OL(off)}	- -	_ _	+ 100 - 100	μА
Output Offset Voltage Difference (Note 2)	Vos-Vos	_	_	± 0.4	V
Output Differential Voltage (Note 2)	V _{OD}	2.0	-	-	V
Output Differential Voltage Difference (Note 2)	IΔV _{OD} I	-	-	± 0.4	V
Power Supply Current (Control Pins = Gnd, Note 3) (Control Pins = 2.0 V)	I _{CCX} I _{CC}	1 -	- -	105 85	mA

NOTES: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA–422 for exact test conditions.
3. Circuit in three–state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25° C, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	tpHL tpLH	_ _		20 20	ns
Output Transition Times – Differential High to Low Output Low to High Output	tTHL tTLH	_ _	- -	20 20	ns
Propagation Delay – Control to Output $ (R_L = 200 \ \Omega, \ C_L = 50 \ pF) $ $ (R_L = 200 \ \Omega, \ C_L = 50 \ pF) $ $ (R_L = \infty, \ C_L = 50 \ pF) $ $ (R_L = 200 \ \Omega, \ C_L = 50 \ pF) $	[†] PHZ(E) [†] PLZ(E) [†] PZH(E) [†] PZL(E)	- - - -	- - - -	25 25 30 30	ns

Figure 1. Three–State Enable Test Circuit and Waveforms

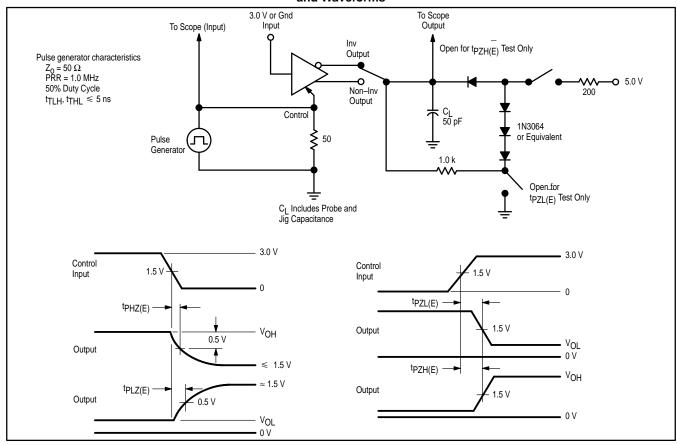


Figure 2. Propagation Delay Times Input to Output Waveforms and Test Circuit

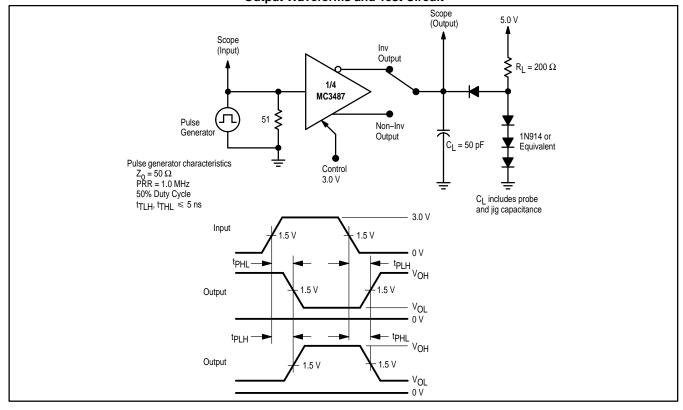


Figure 3. Output Transition Times Test Circuit and Waveforms

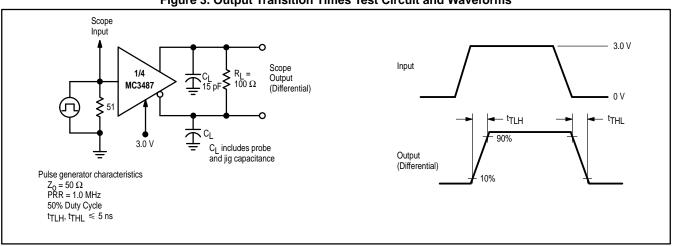


Figure 4. Output Current versus Output Voltage

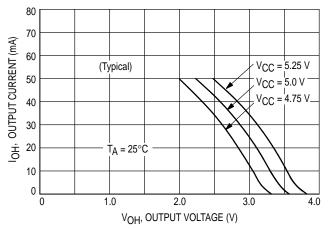
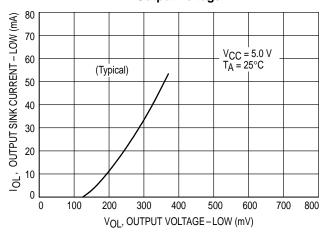
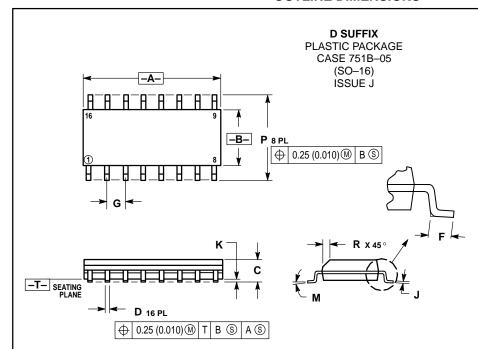


Figure 5. Output Sink Current versus
Output Voltage

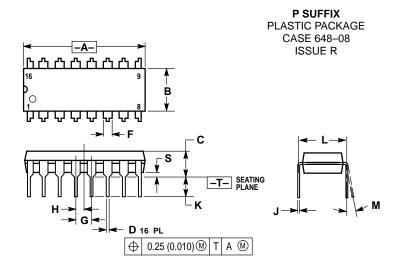


OUTLINE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL
 IN EXCESS OF THE D DIMENSION AT
 MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27 BSC		0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
М	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.010	



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- Y14.5M, 1982.

 CONTROLLING DIMENSION: INCH.

 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10 °	0°	10 °
S	0.020	0.040	0.51	1.01

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