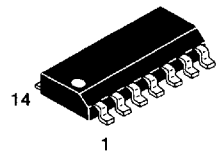
Monolithic Diode Arrays

Surface Mount Diode Arrays

MMAD130
MMAD1103
MMAD1105
MMAD1107
MMAD1109

These diode arrays are multiple diode junctions fabricated by a planar process and mounted in integrated circuit packages for use in high–current, fast–switching core–driver applications. These arrays offer many of the advantages of integrated circuits such as high–density packaging and improved reliability. These advantages result from such factors as fewer glass–to–metal seals.

- Designed for Use in Computers and Peripheral Equipment
- Applications Include:
  - Magnetic Cores
  - Thin–Film Memories
  - Plated–Wire Memories
  - Decoding or Encoding Applications



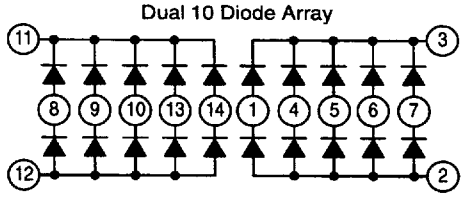
CASE 751A–03
SO–14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Voltage	V_{RM}	50	Vdc
Steady–State Reverse Voltage	V_R	50	Vdc
Peak Forward Current 25°C	I_{FM}	500	mAdc
Continuous Forward Current	I_F	400	mAdc
Power Dissipation Derating Factor	P_D	500 4.0	mW mW/°C
Operating Temperature	T_A	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

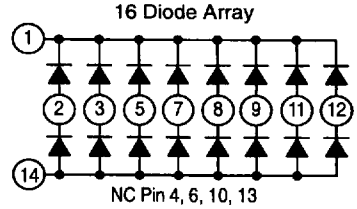
SO–14 PIN DIAGRAM

1
Dual 10 Diode Array



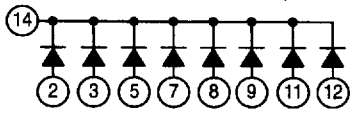
MMAD130

2
16 Diode Array



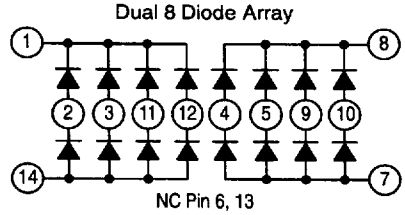
NC Pin 4, 6, 10, 13
MMAD1103

3
8 Diode Array
(Common Cathode)



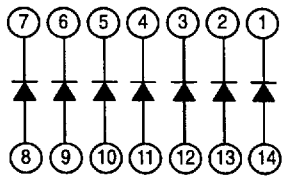
NC Pin 1, 4, 6, 10, 13
MMAD1105

4
Dual 8 Diode Array



NC Pin 6, 13
MMAD1107

5
7 Diode Array
(Independent)



MMAD1109

Thermal Clad is a trademark of the Bergquist Company

REV 1

MOTOROLA

Device	Description	Diagram
MMAD130	Dual 10 Diode Array	1
MMAD1103	16 Diode Array	2
MMAD1105	8 Diode Array Common Cathode	3
MMAD1107	Dual 8 Diode Array	4
MMAD1109	7 Diode Array	5

ELECTRICAL CHARACTERISTICS (@ 25°C Free–Air Temperature)

Characteristic	Symbol	Limit		Unit
		Min	Max	
Reverse Breakdown Voltage(1) (I_R = 10 μAdc)	$V_{(BR)}$	50	—	Vdc
Static Reverse Current (V_R = 40 Vdc)	I_R	—	0.1	μAdc
Static Forward Voltage (I_F = 100 mAdc)	V_F	—	1.2	Vdc
(I_F = 500 mAdc)(2)		—	1.6	
Peak Forward Voltage(3) (I_F = 500 mAdc)	V_{FM}	—	5.0	Vdc

SWITCHING CHARACTERISTICS (@ 25°C Free–Air Temperature)

Characteristic	Symbol	Typical Value	Unit
Forward Recovery Time (I_F = 500 mAdc)	t_{fr}	20	ns
Reverse Recovery Time (I_F = 200 mA, I_{RM} = 200 mA, R_L = 100 Ω, i_{rr} = 20 mA)	t_{rr}	8.0	ns

NOTES:
1. This parameter must be measured using pulse techniques. PW = 100 μs, duty cycle ≤ 20%.
2. This parameter is measured using pulse techniques. PW = 300 μs, duty cycle ≤ 2.0%. Read time is 90 μs from the leading edge of the pulse.
3. The initial instantaneous value is measured using pulse techniques. PW = 150 ns, duty cycle ≤ 2.0%, pulse rise time ≤ 10 ns. The total capacitance shunting the diode is 19 pF maximum and the equipment bandwidth is 80 MHz.

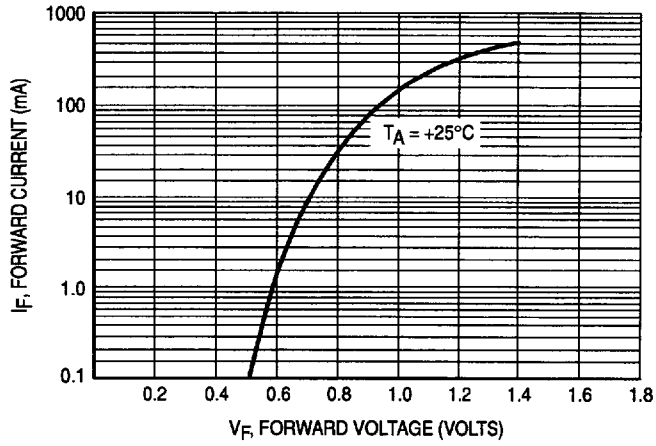


Figure 1. Typical Characteristics Static Forward Voltage

TEST PROCEDURE FOR MULTIPLE DIODES

1.0. REVERSE BIAS TESTING

1.1. LEAKAGE

Regardless of device configuration type, when testing any reverse bias condition, the forcing power supply must be applied only to the uncommon terminal of the pair. As in Figure 1, this would be pins 1 and 14. This can be referred as the high side of the test circuit. The low side of the test circuit must be connected to the common terminal of the pair which in most testers is where the current measurement is taken. This method is used to eliminate the possibility of degrading the diode in that pair which is not under test. Diode arrays with multiple pairs such as the MMAD1103, also have leakage paths in the die between common terminals of the pairs. To isolate the device under test so that the leakage from the other pairs in the package do not affect the test result, the leakage current from the common terminals of the pairs not under test must be shunted to measurement common. Figure 1 shows the test configuration for both of these cases.

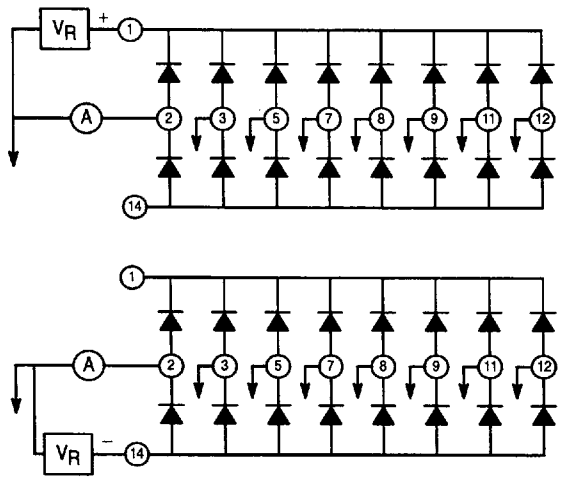


Figure 1

1.2. BREAKDOWN

It is not recommended to test breakdown on these devices due to the possibility of degrading the device. Breakdown may be checked on a curve tracer but extreme caution should be used.

2.0. FORWARD BIAS TESTING

Diode arrays are designed with the pairs in parallel; therefore, care must be taken to prevent the other diodes in the array from affecting the measured value of the diode under test. Figure 2 illustrates the proper technique to measure only the correct value of the diode under test.

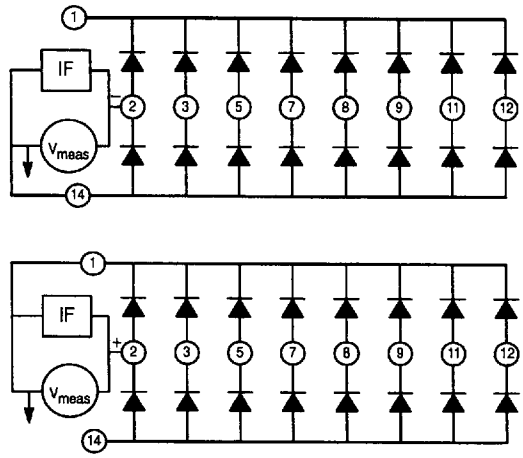


Figure 2

2.1. KELVIN CONNECTION

To achieve the best possible accuracy when testing bias currents over 10 mA, Kelvin connection to the leads of the device under test is mandatory. True Kelvin connection dictates that two test connections are made directly to the leads of the device. One is for power which is the bias supply, and the other is for sense which is for the measurement circuit. Kelvin connections are used to eliminate the effects of the connection resistance between the lead of the device and the contacts of the test handler and/or hand fixture. Figure 3 is an example of Kelvin connection.

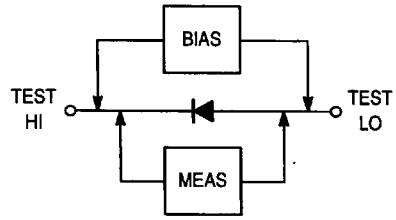


Figure 3

2.2. PULSE TESTING

When testing bias currents over 10 mA, pulse testing should be used to minimize thermal drift of the measured value. The pulse width of a pulse test is approximately 300 μs to 380 μs.

3.0. TESTING PROTOCOL

3.1. TEST TYPES

When testing in sequence all of the electrical characteristics, all reverse bias conditions should be tested before the forward bias conditions are tested.

3.2. BIASING MAGNITUDES

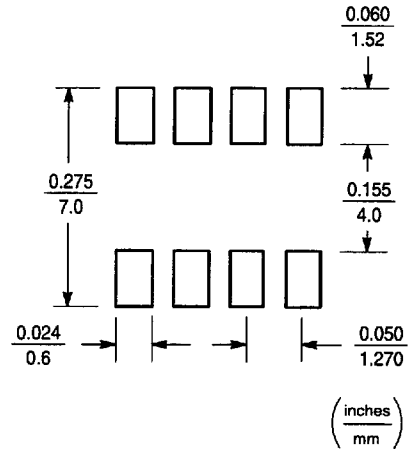
Tests of the same test type should be grouped together with the bias conditions in ascending order. For example:

V_F @ 10 mA < 0.6 V
V_F @ 50 mA < 0.8 V
V_F @ 100 mA < 1 V
V_F @ 500 mA < 1.5 V

INFORMATION FOR USING THE SO–14 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SO–14

SO–14 POWER DISSIPATION

The power dissipation of the SO–14 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SO–14 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is .5 watts.

$$P_D = \frac{150°C - 25°C}{250°C/W} = .5 \text{ watts}$$

The 250°C/W for the SO–14 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of .5 watts. There are other alternatives to achieving higher power dissipation from the SO–14 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

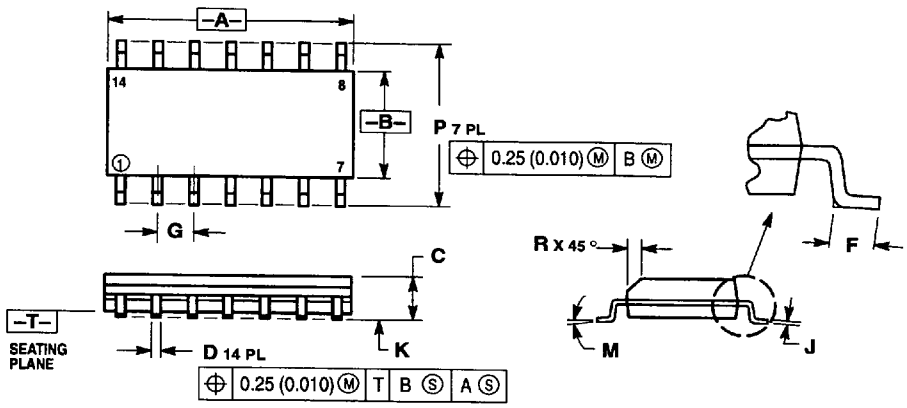
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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ISSUE F