SLAS541 – JUNE 2007

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption:**
  - **Active Mode: 365 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.9 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Three-Channel Internal DMA**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature**
- **Dual 12-Bit D/A Converters With Synchronization**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers**
- **On-Chip Comparator**
- **Four Universal Serial Communication Interface (USCI) Modules With:**
  - **Enhanced UART Supporting Auto-Baudrate Detection (LIN)**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**
  - **I²C™**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Brownout Detector**
- **Bootstrap Loader**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Family Members† Include:**
  - **MSP430F2416: 92KB+256B Flash Memory, 4KB RAM**
  - **MSP430F2417: 92KB+256B Flash Memory, 8KB RAM**
  - **MSP430F2418: 116KB+256B Flash Memory, 8KB RAM**
  - **MSP430F2419: 120KB+256B Flash Memory, 4KB RAM**
  - **MSP430F2616: 92KB+256B Flash Memory, 4KB RAM**
  - **MSP430F2617: 92KB+256B Flash Memory, 8KB RAM**
  - **MSP430F2618: 116KB+256B Flash Memory, 8KB RAM**
  - **MSP430F2619: 120KB+256B Flash Memory, 4KB RAM**
- **Available in 80-Pin Quad Flat Pack (QFP) and 64-Pin QFP (See Available Options)**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144**

† The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 modules and the DMA controller are not implemented.

PRODUCT PREVIEW

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1μs.

The MSP430F261x/241x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, dual 12-bit D/A converter, four universal serial communication interface (USCI) modules, DMA, and up to 64 I/O pins. The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 and the DMA modules are not implemented.

Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

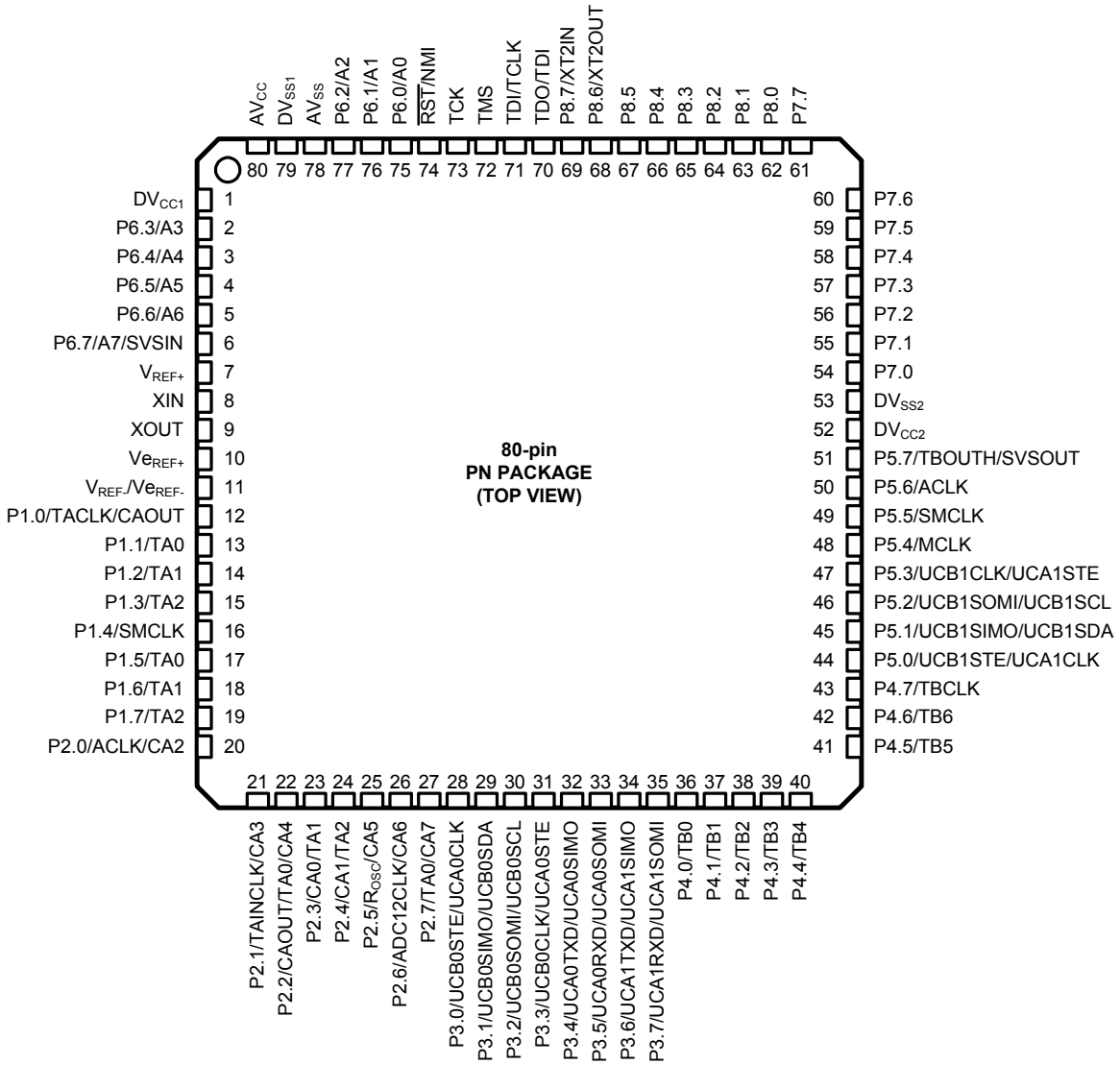
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 80-PIN LQFP (PN)	PLASTIC 64-PIN LQFP (PM)
–40°C to 105°C	MSP430F2416TPN†	MSP430F2416TPM†
	MSP430F2417TPN†	MSP430F2417TPM†
	MSP430F2418TPN†	MSP430F2418TPM†
	MSP430F2419TPN†	MSP430F2419TPM†
	MSP430F2616TPN†	MSP430F2616TPM†
	MSP430F2617TPN†	MSP430F2617TPM†
	MSP430F2618TPN†	MSP430F2618TPM†
	MSP430F2619TPN†	MSP430F2619TPM†

† Product Preview

PRODUCT PREVIEW

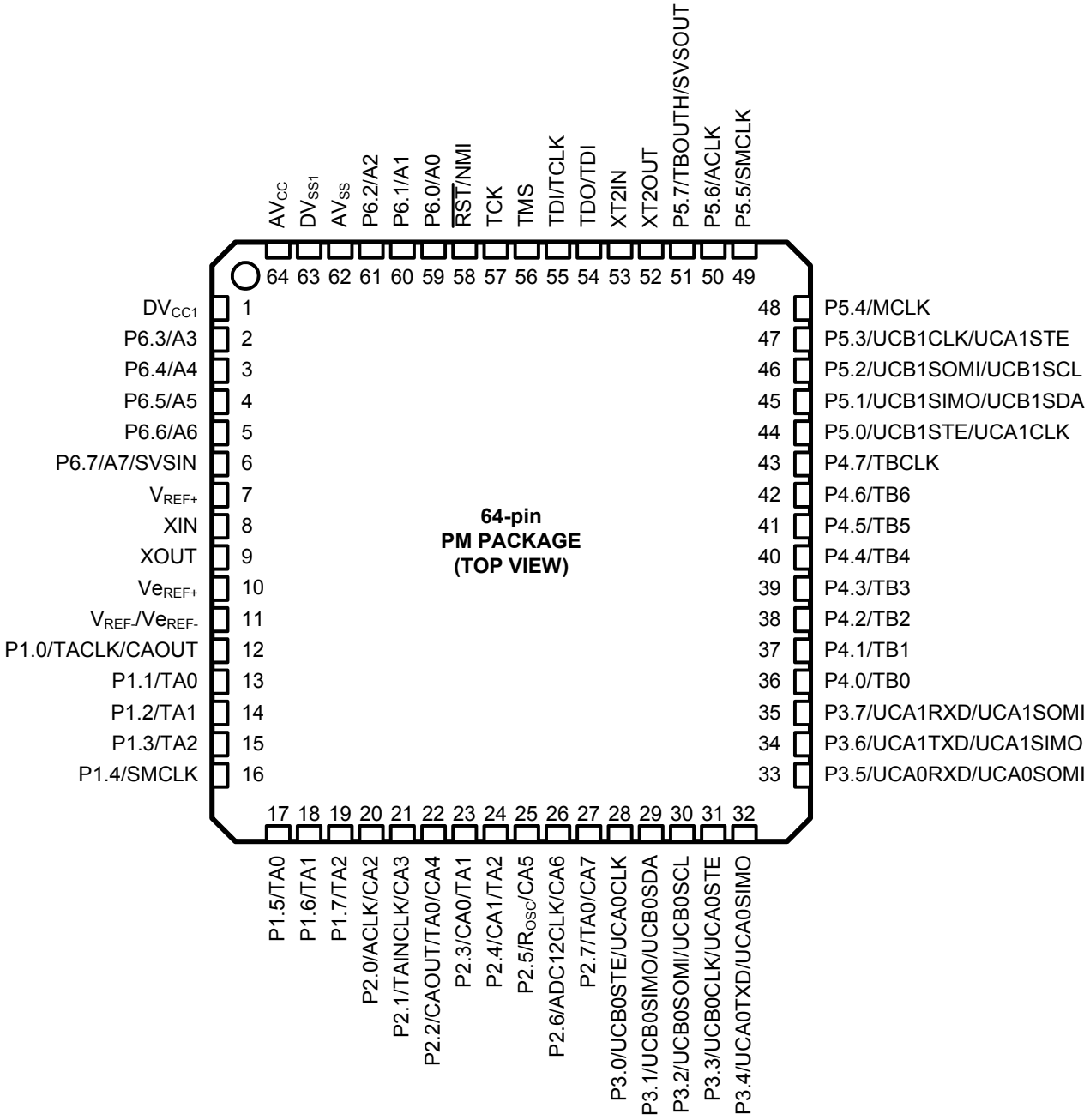
pin designation – MSP430F241x, 80-pin package



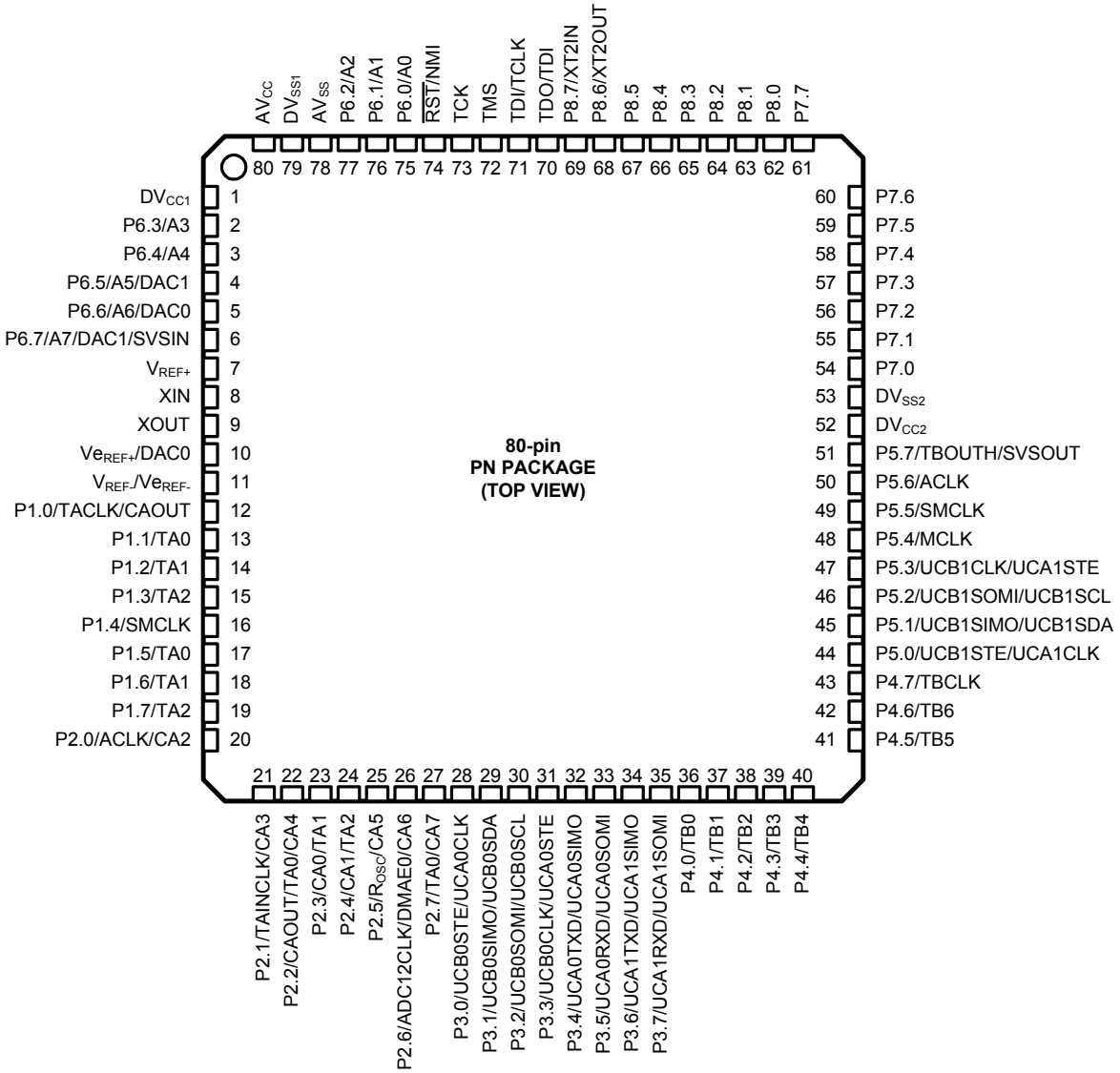
PRODUCT PREVIEW

PRODUCT PREVIEW

pin designation – MSP430F241x, 64-pin package



pin designation – MSP430F261x, 80-pin package



PRODUCT PREVIEW

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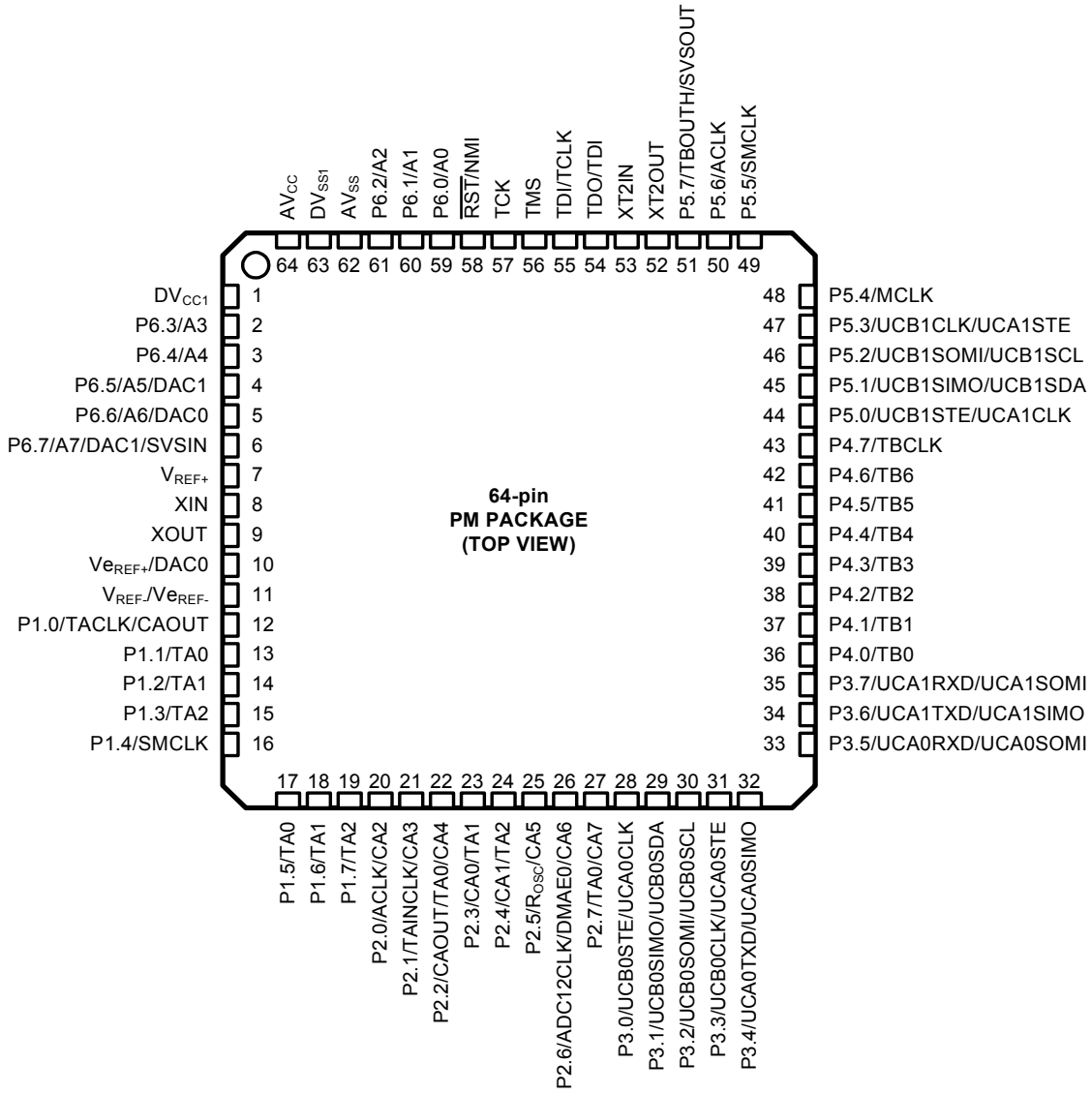
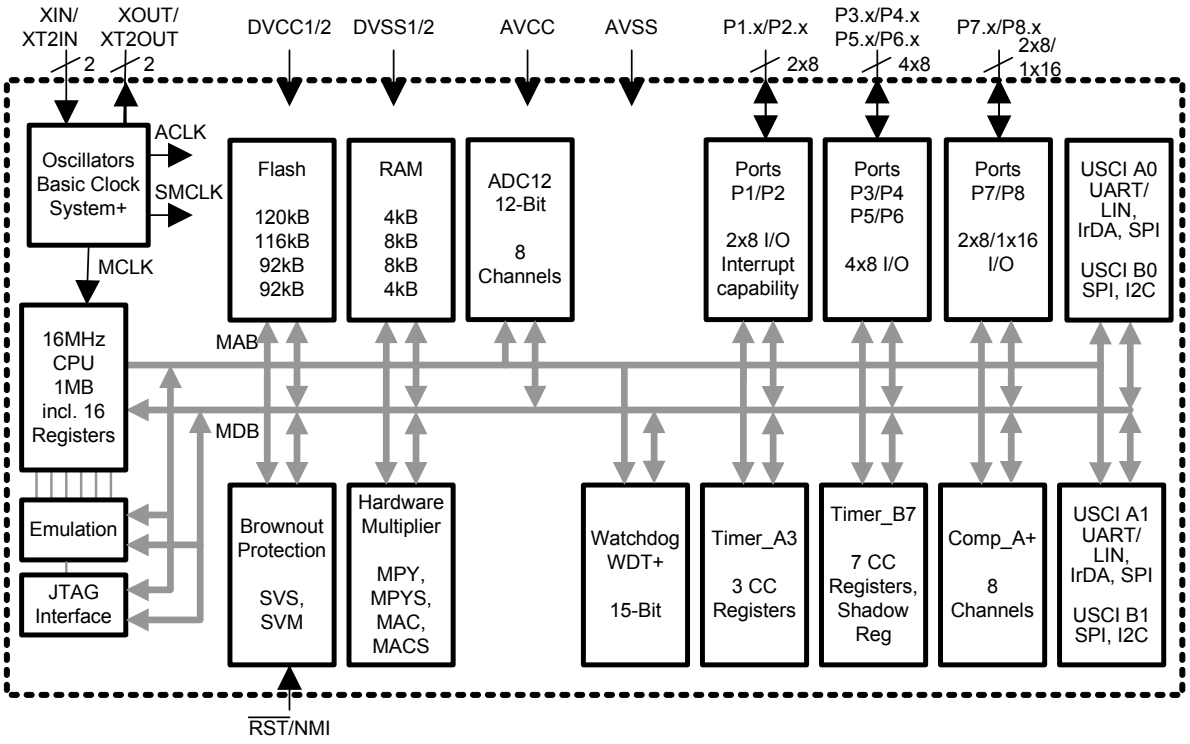
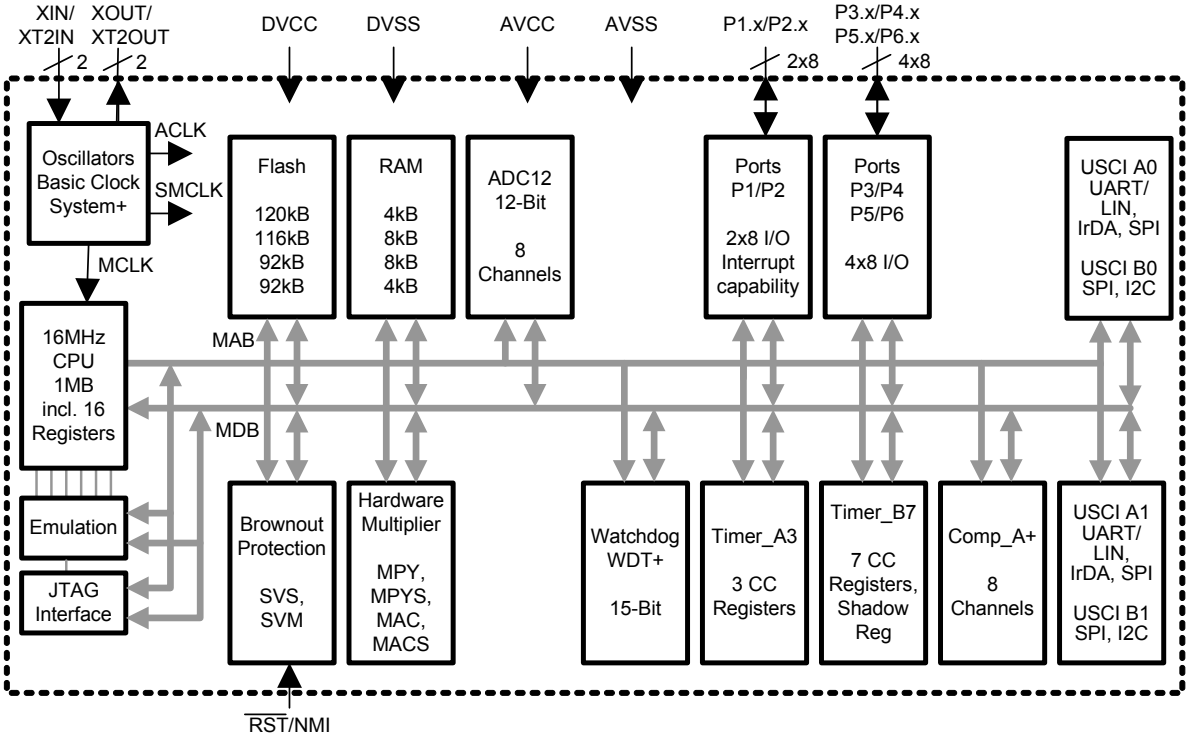
pin designation – MSP430F261x, 64-pin package



functional block diagram – MSP430F241x, 80-pin package



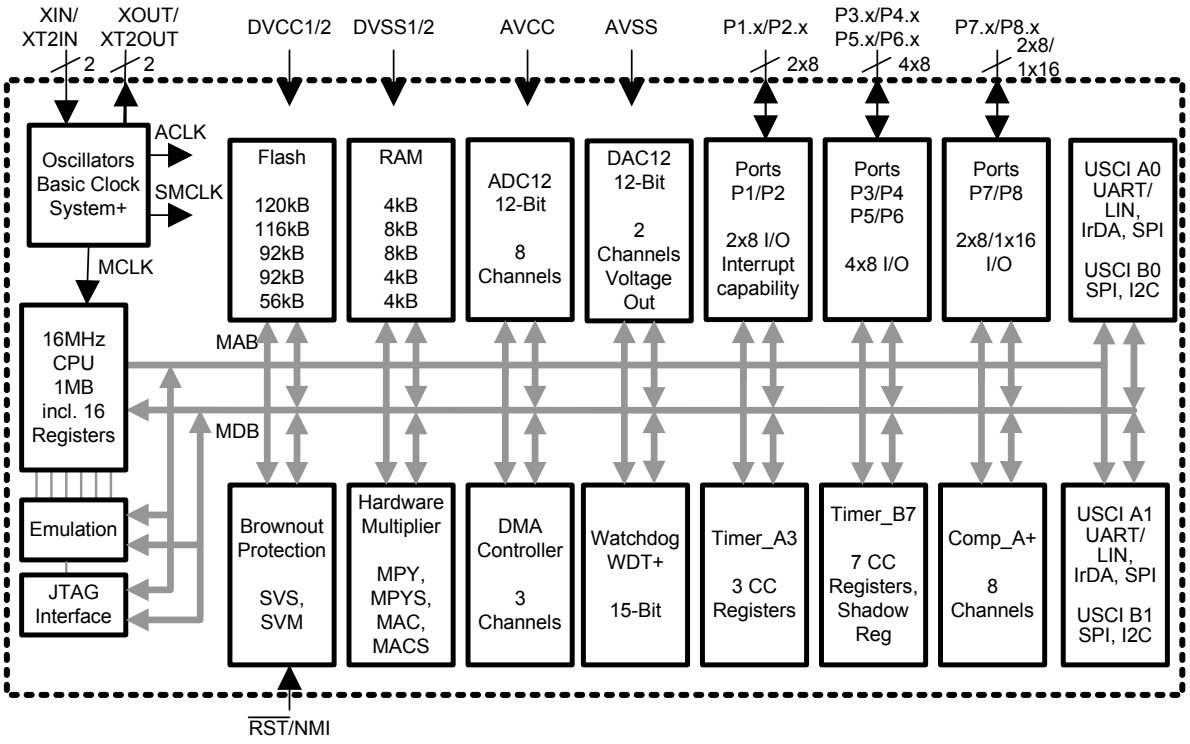
functional block diagram – MSP430F241x, 64-pin package



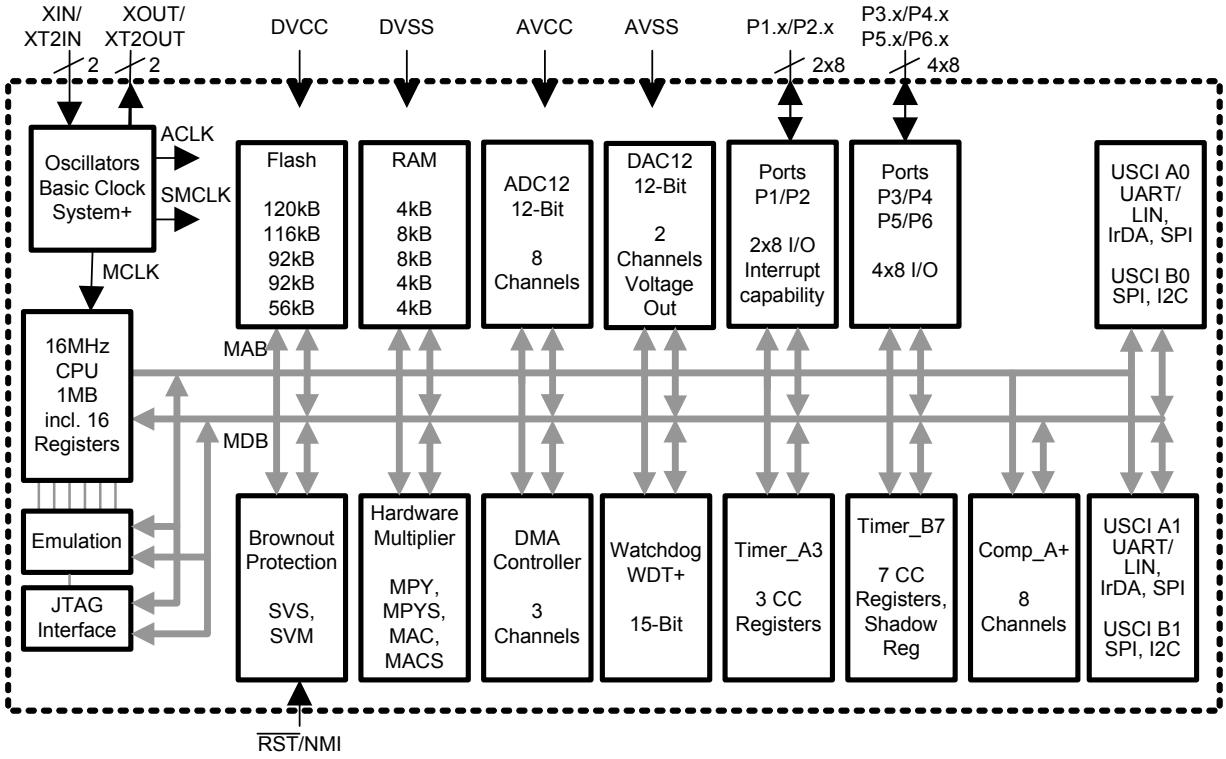
PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram – MSP430F261x, 80-pin package



functional block diagram – MSP430F261x, 64-pin package



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	64-Pin NO.	80-Pin NO.		
AV_{CC}	64	80		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62	78		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC1}	1	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	63	79		Digital supply voltage, negative terminal. Supplies all digital parts.
DV_{CC2}		52		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS2}		53		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/ CAOUT	12	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input/Comparator_A output
P1.1/TA0	13	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	20	I/O	General-purpose digital I/O pin/ACLK output/Comparator_A input
P2.1/TAINCLK/ CA3	21	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/ TA0/CA4	22	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc/CA5	25	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input
P2.6/ADC12CLK/ DMAE0†/CA6	26	26	I/O	General-purpose digital I/O pin/conversion clock – 12-bit ADC/DMA channel 0 external trigger/Comparator_A input
P2.7/TA0/CA7	27	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	28	I/O	General-purpose digital I/O pin/USCI B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA	29	29	I/O	General-purpose digital I/O pin/USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	30	I/O	General-purpose digital I/O pin/USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/ UCA0STE	31	31	I/O	General-purpose digital I/O/USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	32	32	I/O	General-purpose digital I/O pin/USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	33	I/O	General-purpose digital I/O pin/USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/ UCA1SIMO	34	32	I/O	General-purpose digital I/O pin/USCI A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	33	I/O	General-purpose digital I/O pin/USCIA1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output

† MSP430F261x devices only

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	64-Pin NO.	80-Pin NO.		
P4.2/TB2	38	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	39	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	40	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	41	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	42	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0/UCB1STE/ UCA1CLK	44	44	I/O	General-purpose digital I/O pin/USCI B1 slave transmit enable/USCI A1 clock input/output
P5.1/UCB1SIMO/ UCB1SDA	45	45	I/O	General-purpose digital I/O pin/USCI B1slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/ UCB1SCL	46	46	I/O	General-purpose digital I/O pin/USCI B1slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/ UCA1STE	47	47	I/O	General-purpose digital I/O/USCI B1 clock input/output, USCI A1 slave transmit enable
P5.4/MCLK	48	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output
P5.6/ACLK	50	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH/ SVSOUT	51	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance – Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	75	I/O	General-purpose digital I/O pin/analog input a0 – 12-bit ADC
P6.1/A1	60	76	I/O	General-purpose digital I/O pin/analog input a1 – 12-bit ADC
P6.2/A2	61	77	I/O	General-purpose digital I/O pin/analog input a2 – 12-bit ADC
P6.3/A3	2	2	I/O	General-purpose digital I/O pin/analog input a3 – 12-bit ADC
P6.4/A4	3	3	I/O	General-purpose digital I/O pin/analog input a4 – 12-bit ADC
P6.5/A5/DAC1†	4	4	I/O	General-purpose digital I/O pin/analog input a5 – 12-bit ADC/DAC12.1 output
P6.6/A6/DAC0†	5	5	I/O	General-purpose digital I/O pin/analog input a6 – 12-bit ADC/DAC12.0 output
P6.7/A7/DAC1†/ SVSIN	6	6	I/O	General-purpose digital I/O pin/analog input a7 – 12-bit ADC/DAC12.1 output/SVS input
P7.0		54	I/O	General-purpose digital I/O pin
P7.1		55	I/O	General-purpose digital I/O pin
P7.2		56	I/O	General-purpose digital I/O pin
P7.3		57	I/O	General-purpose digital I/O pin
P7.4		58	I/O	General-purpose digital I/O pin
P7.5		59	I/O	General-purpose digital I/O pin
P7.6		60	I/O	General-purpose digital I/O pin
P7.7		61	I/O	General-purpose digital I/O pin
P8.0		62	I/O	General-purpose digital I/O pin
P8.1		63	I/O	General-purpose digital I/O pin
P8.2		64	I/O	General-purpose digital I/O pin
P8.3		65	I/O	General-purpose digital I/O pin
P8.4		66	I/O	General-purpose digital I/O pin
P8.5		67	I/O	General-purpose digital I/O pin

† MSP430F261x devices only

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	64-Pin NO.	80-Pin NO.		
P8.6/XT2OUT		68	O	General-purpose digital I/O pin/Output terminal of crystal oscillator XT2
P8.7/XT2IN		69	I	General-purpose digital I/O pin/Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52		O	Output terminal of crystal oscillator XT2
XT2IN	53		I	Input port for crystal oscillator XT2
$\overline{\text{RST}}$/NMI	58	74	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	73	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start
TDI/TCLK	55	71	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	70	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	72	I	Test mode select. TMS is used as an input port for device programming and test.
Ve_{REF+}/DAC0†	10	10	I	Input for an external reference voltage/DAC12.0 output
V_{REF+}	7	7	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/Ve_{REF-}	11	11	I	Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	9	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.

† MSP430F261x devices only

PRODUCT PREVIEW

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g. CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0x0FFFF to 0x0FFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (0x0FFFE) contains 0x0FFFF (e.g. flash is not programmed) the CPU enters LPM4 after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash Key Violation PC out of range (see Note 1)	PORIFG WDTIFG RSTIFG KEYV (see Note 2)	Reset	0x0FFFE	31, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 & 4)	(Non)maskable (Non)maskable (Non)maskable	0x0FFFC	30
Timer_B7	TBCCR0 CCIFG (see Note 3)	Maskable	0x0FFFA	29
Timer_B7	TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 2 & 3)	Maskable	0x0FFF8	28
Comparator_A+	CAIFG	Maskable	0x0FFF6	27
Watchdog timer+	WDTIFG	Maskable	0x0FFF4	26
Timer_A3	TACCR0 CCIFG (see Note 3)	Maskable	0x0FFF2	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG (see Note 2 & 3)	Maskable	0x0FFF0	24
USCIA0/B0 Receive	UCA0RXIFG, UCB0RXIFG (see Note 2)	Maskable	0x0FFEE	23
USCIA0/B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Note 2)	Maskable	0x0FFEC	22
ADC12	ADC12IFG (see Notes 2 & 3)	Maskable	0x0FFEA	21
			0x0FFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 & 3)	Maskable	0x0FFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 & 3)	Maskable	0x0FFE4	18
USCIA1/B1 Receive	UCA1RXIFG, UCB1RXIFG (see Note 2)	Maskable	0x0FFE2	17
USCIA1/B1 Transmit	UCA1TXIFG, UCB1TXIFG (see Note 2)	Maskable	0x0FFE0	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG (see Notes 2 & 3)	Maskable	0x0FFDE	15
DAC12	DAC12_0IFG, DAC12_1IFG (see Notes 2 & 3)	Maskable	0x0FFDC	14
Reserved (see Note 5 & 6)	Reserved		0x0FFDA ... 0x0FFC0	13 ... 0, lowest

NOTES:
1. A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x00000 to 0x001FF) or from within unused address ranges.
2. Multiple source flags.
3. Interrupt flags are located in the module.
4. Non-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
5. The address 0x0FFBE is used as bootstrap loader security key (BSLSKEY).
   A 0x0AA55 at this location disables the BSL completely.
   A zero disables the erasure of the flash if an invalid password is supplied.
6. The interrupt vectors at addresses 0x0FFDA to 0x0FFC0 are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

Interrupt Enable register 1

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as general-purpose timer.
OFIE	Oscillator-fault-interrupt enable
NMIIE	Nonmaskable-interrupt enable
ACCVIE	Flash memory access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

Interrupt Enable register 2

UCA0RXIE	USCI_A0 receive–interrupt enable
UCA0TXIE	USCI_A0 transmit–interrupt enable
UCB0RXIE	USCI_B0 receive–interrupt enable
UCB0TXIE	USCI_B0 transmit–interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

Interrupt Flag register 1

WDTIFG Set on watchdog-timer overflow or security key violation.
Reset on V_{CC} power-on, or a reset condition at the $\overline{RST}$/NMI pin in reset mode

OFIFG Flag set on oscillator fault

PORIFG Power–On interrupt flag. Set on V_{CC} power–up.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode.
Reset on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					UCB0TX IFG	UCB0RX IFG	UCA0TX IFG	UCA0RX IFG
					rw-1	rw-0	rw-1	rw-0

Interrupt Flag register 2

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

Legend	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1)	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device.

PRODUCT PREVIEW

memory organization (MSP430F241x, MSP430F261x)

		MSP430F2416 MSP430F2616	MSP430F2417 MSP430F2617
Memory Main: interrupt vector Main: code memory	Size Flash Flash	92KB 0x0FFFF – 0x0FFC0 0x18FFF – 0x02100	92KB 0x0FFFF – 0x0FFC0 0x19FFF – 0x03100
RAM (Total) Extended Mirrored	Size Size Size	4kB 0x020FF – 0x01100 2kB 0x020FF – 0x01900 2kB 0x018FF – 0x01100	8kB 0x030FF – 0x01100 6kB 0x030FF – 0x01900 2kB 0x018FF – 0x01100
Information memory	Size Flash	256 Byte 0x010FF – 0x01000	256 Byte 0x010FF – 0x01000
Boot memory	Size ROM	1KB 0x00FFF – 0x00C00	1KB 0x00FFF – 0x00C00
RAM (mirrored at 0x18FF – 0x01100)	Size	2KB 0x009FF – 0x00200	2KB 0x009FF – 0x00200
Peripherals	16-bit 8-bit 8-bit SFR	0x001FF – 0x00100 0x000FF – 0x00010 0x0000F – 0x00000	0x001FF – 0x00100 0x000FF – 0x00010 0x0000F – 0x00000

		MSP430F2618 MSP430F2418	MSP430F2619 MSP430F2419
Memory Main: interrupt vector Main: code memory	Size Flash Flash	116KB 0x0FFFF – 0x0FFC0 0x1FFFF – 0x03100	120KB 0x0FFFF – 0x0FFC0 0x1FFFF – 0x02100
RAM (Total) Extended Mirrored	Size Size Size	8kB 0x030FF – 0x01100 6kB 0x030FF – 0x01900 2kB 0x018FF – 0x01100	4kB 0x020FF – 0x01100 2kB 0x020FF – 0x01900 2kB 0x018FF – 0x01100
Information memory	Size Flash	256 Byte 0x010FF – 0x01000	256 Byte 0x010FF – 0x01000
Boot memory	Size ROM	1KB 0x00FFF – 0x00C00	1KB 0x00FFF – 0x00C00
RAM (mirrored at 0x18FF – 0x01100)	Size	2KB 0x009FF – 0x00200	2KB 0x009FF – 0x00200
Peripherals	16-bit 8-bit 8-bit SFR	0x001FF – 0x00100 0x000FF – 0x00010 0x0000F – 0x00000	0x001FF – 0x00100 0x000FF – 0x00010 0x0000F – 0x00000

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	PM, RTD Package Pins
Data Transmit	13 - P1.1
Data Receive	22 - P2.2

PRODUCT PREVIEW

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide*, TI literature number SLAU144.

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430x241x and MSP43x261x family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high frequency crystal, or a very low power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

calibration data stored in information memory segment A

Calibration data is stored for both the DCO and for ADC12 organized in a tag-length-value structure.

Tags used by the ADC calibration tags			
Name	**Address**	**Value**	**Description**
DCO_30	0x10F6	0x01	DCO frequency calibration at VCC = 3.0 V and T_A = 30°C at calibration
ADC12_1	0x10DA	0x10	ADC12_1 calibration tag
EMPTY	-	0xFE	Identifier for empty memory areas

Labels used by the ADC calibration tags			
Label	**Condition at calibration / description**	**Size**	**Address offset**
ADC_25T85	INCHx = 0x1010; REF2_5 = 1, T_A = 85°C	word	0x000E
ADC_25T30	INCHx = 0x1010; REF2_5 = 1, T_A = 30°C	word	0x000C
ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C	word	0x000A
ADC_15T85	INCHx = 0x1010; REF2_5 = 0, T_A = 85°C	word	0x0008
ADC_15T30	INCHx = 0x1010; REF2_5 = 0, T_A = 30°C	word	0x0006
ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C	word	0x0004
ADC_OFFSET	External Vref = 1.5V, T_A = 30°C	word	0x0002
ADC_GAIN_FACTOR	External Vref = 1.5V, T_A = 30°C	word	0x0000
CALBC1_1MHz	-	byte	0x0007
CALBC1_1MHz	-	byte	0x0006
CALBC1_8MHz	-	byte	0x0005
CALBC1_8MHz	-	byte	0x0004
CALBC1_12MHz	-	byte	0x0003
CALBC1_12MHz	-	byte	0x0002
CALBC1_16MHz	-	byte	0x0001
CALDCO_16MHz	-	byte	0x0000

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are up to eight 8-bit I/O ports implemented—ports P1 through P8:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
- Ports P7/P8 can be accessed word wise.

watchdog timer+

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

USCI

The universal serial communicating interface (USCI) modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I^2C and asynchronous combination protocols like UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI A module provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

The USCI B module provides support for SPI (3 or 4 pin) and I^2C.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections					
Input Pin Number	**Device Input Signal**	**Module Input Name**	**Module Block**	**Module Output Signal**	**Output Pin Number**
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	V_{CC}			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DV_{SS}	GND			23 - P2.3
	DV_{CC}	V_{CC}			ADC12 (internal)
					DAC12_0 (internal)
					DAC12_1 (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DV_{SS}	GND			24 - P2.4
	DV_{CC}	V_{CC}			

timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3/B7 Signal Connections[†]					
Input Pin Number	**Device Input Signal**	**Module Input Name**	**Module Block**	**Module Output Signal**	**Output Pin Number**
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	$\overline{\text{TBCLK}}$	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			DAC_0(internal)
	DV_{SS}	GND			DAC_1(internal)
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog–to–digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

peripheral file map

PERIPHERAL FILE MAP			
DMA†	DMA channel 2 transfer size	DMA2SZ	0x01F2
	DMA channel 2 destination address	DMA2DA	0x01EE
	DMA channel 2 source address	DMA2SA	0x01EA
	DMA channel 2 control	DMA2CTL	0x01E8
	DMA channel 1 transfer size	DMA1SZ	0x01E6
	DMA channel 1 destination address	DMA1DA	0x01E2
	DMA channel 1 source address	DMA1SA	0x01DE
	DMA channel 1 control	DMA1CTL	0x01DC
	DMA channel 0 transfer size	DMA0SZ	0x01DA
	DMA channel 0 destination address	DMA0DA	0x01D6
	DMA channel 0 source address	DMA0SA	0x01D2
	DMA channel 0 control	DMA0CTL	0x01D0
	DMA module interrupt vector word	DMAIV	0x0126
	DMA module control 1	DMACTL1	0x0124
	DMA module control 0	DMACTL0	0x0122
DAC12†	DAC12_1 data	DAC12_1DAT	0x01CA
	DAC12_1 control	DAC12_1CTL	0x01C2
	DAC12_0 data	DAC12_0DAT	0x01C8
	DAC12_0 control	DAC12_0CTL	0x01C0
ADC12	Interrupt-vector-word register	ADC12IV	0x01A8
	Inerrupt-enable register	ADC12IE	0x01A6
	Inerrupt-flag register	ADC12IFG	0x01A4
	Control register 1	ADC12CTL1	0x01A2
	Control register 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C
	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion memory 0	ADC12MEM0	0x0140

† MSP430F261x devices only

PERIPHERAL FILE MAP (CONTINUED)			
ADC12 (continued)	ADC memory-control register15	ADC12MCTL15	0x008F
	ADC memory-control register14	ADC12MCTL14	0x008E
	ADC memory-control register13	ADC12MCTL13	0x008D
	ADC memory-control register12	ADC12MCTL12	0x008C
	ADC memory-control register11	ADC12MCTL11	0x008B
	ADC memory-control register10	ADC12MCTL10	0x008A
	ADC memory-control register9	ADC12MCTL9	0x0089
	ADC memory-control register8	ADC12MCTL8	0x0088
	ADC memory-control register7	ADC12MCTL7	0x0087
	ADC memory-control register6	ADC12MCTL6	0x0086
	ADC memory-control register5	ADC12MCTL5	0x0085
	ADC memory-control register4	ADC12MCTL4	0x0084
	ADC memory-control register3	ADC12MCTL3	0x0083
	ADC memory-control register2	ADC12MCTL2	0x0082
	ADC memory-control register1	ADC12MCTL1	0x0081
	ADC memory-control register0	ADC12MCTL0	0x0080
Timer_B7	Capture/compare register 6	TBCCR6	0x019E
	Capture/compare register 5	TBCCR5	0x019C
	Capture/compare register 4	TBCCR4	0x019A
	Capture/compare register 3	TBCCR3	0x0198
	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare register 2	TACCR2	0x0176
	Capture/compare register 1	TACCR1	0x0174
	Capture/compare register 0	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E

PERIPHERAL FILE MAP (CONTINUED)			
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed + accumulate/operand1	MACS	0x0136
	Multiply + accumulate/operand1	MAC	0x0134
	Multiply signed/operand1	MPYS	0x0132
	Multiply unsigned/operand1	MPY	0x0130
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I^2C Interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I^2C slave address	UCB0SA	0x011A
	USCI B0 I^2C own address	UCB0OA	0x0118
USCI A1/B1	USCI A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI A1 receive buffer	UCA1RXBUF	0x00D6
	USCI A1 status	UCA1STAT	0x00D5
	USCI A1 modulation control	UCA1MCTL	0x00D4
	USCI A1 baud rate control 1	UCA1BR1	0x00D3
	USCI A1 baud rate control 0	UCA1BR0	0x00D2
	USCI A1 control 1	UCA1CTL1	0x00D1
	USCI A1 control 0	UCA1CTL0	0x00D0
	USCI A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI A1 IrDA transmit control	UCA1IRTCLT	0x00CE

PERIPHERAL FILE MAP (CONTINUED)			
USCI A1/B1 (continued)	USCI B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI B1 receive buffer	UCB1RXBUF	0x00DE
	USCI B1 status	UCB1STAT	0x00DD
	USCI B1 I^2C Interrupt enable	UCB1CIE	0x00DC
	USCI B1 baud rate control 1	UCB1BR1	0x00DB
	USCI B1 baud rate control 0	UCB1BR0	0x00DA
	USCI B1 control 1	UCB1CTL1	0x00D9
	USCI B1 control 0	UCB1CTL0	0x00D8
	USCI B1 I^2C slave address	UCB1SA	0x017E
	USCI B1 I^2C own address	UCB1OA	0x017C
	USCI A1/B1 interrupt enable	UC1IE	0x0006
	USCI A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059
Basic Clock	Basic clock system control3	BCSCTL3	0x0053
	Basic clock system control2	BCSCTL2	0x0058
	Basic clock system control1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port PA†	Port PA resistor enable	PAREN	0x0014
	Port PA selection	PASEL	0x003E
	Port PA direction	PADIR	0x003C
	Port PA output	PAOUT	0x003A
	Port PA input	PAIN	0x0038
Port P8†	Port P8 resistor enable	P8REN	0x0015
	Port P8 selection	P8SEL	0x003F
	Port P8 direction	P8DIR	0x003D
	Port P8 output	P8OUT	0x003B
	Port P8 input	P8IN	0x0039
Port P7†	Port P7 resistor enable	P7REN	0x0014
	Port P7 selection	P7SEL	0x003E
	Port P7 direction	P7DIR	0x003C
	Port P7 output	P7OUT	0x003A
	Port P7 input	P7IN	0x0038
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030

† 80-pin devices only

PERIPHERAL FILE MAP (CONTINUED)			
Port P4	Port P4 selection	P4SEL	0x001F
	Port P4 resistor enable	P4REN	0x0011
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag2	IFG2	0x0003
	SFR interrupt flag1	IFG1	0x0002
	SFR interrupt enable2	IE2	0x0001
	SFR interrupt enable1	IE1	0x0000

Data Sheet Revision History

Literature Number	Summary
SLAS541	Initial Product Preview release

PACKAGING INFORMATION

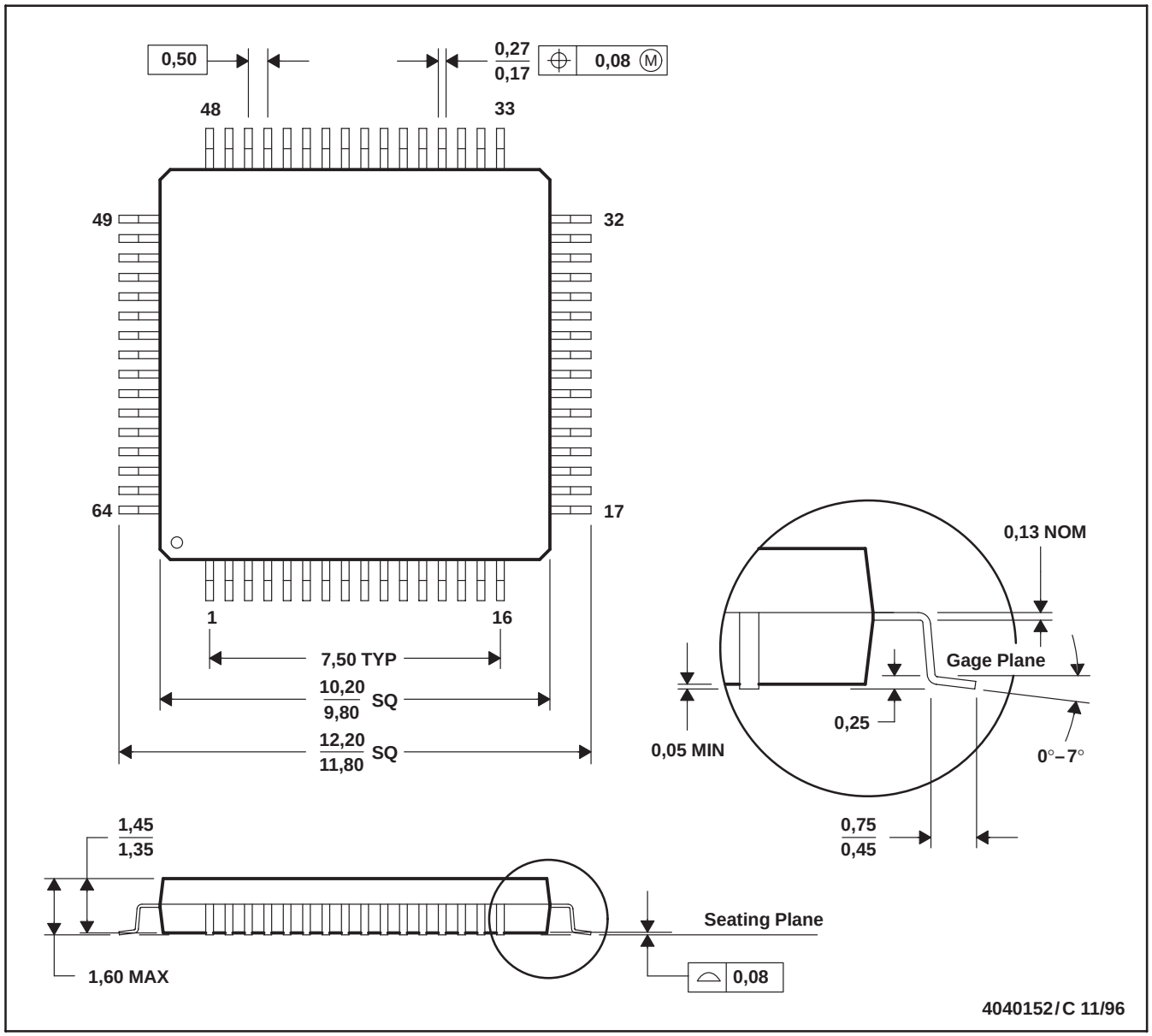
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MSP430F2416TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2416TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2417TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2417TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2418TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2418TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2419TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2419TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2616TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2616TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2617TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2617TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2618TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2618TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F2619TPM	PREVIEW	LQFP	PM	64	50	TBD	Call TI	Call TI
MSP430F2619TPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

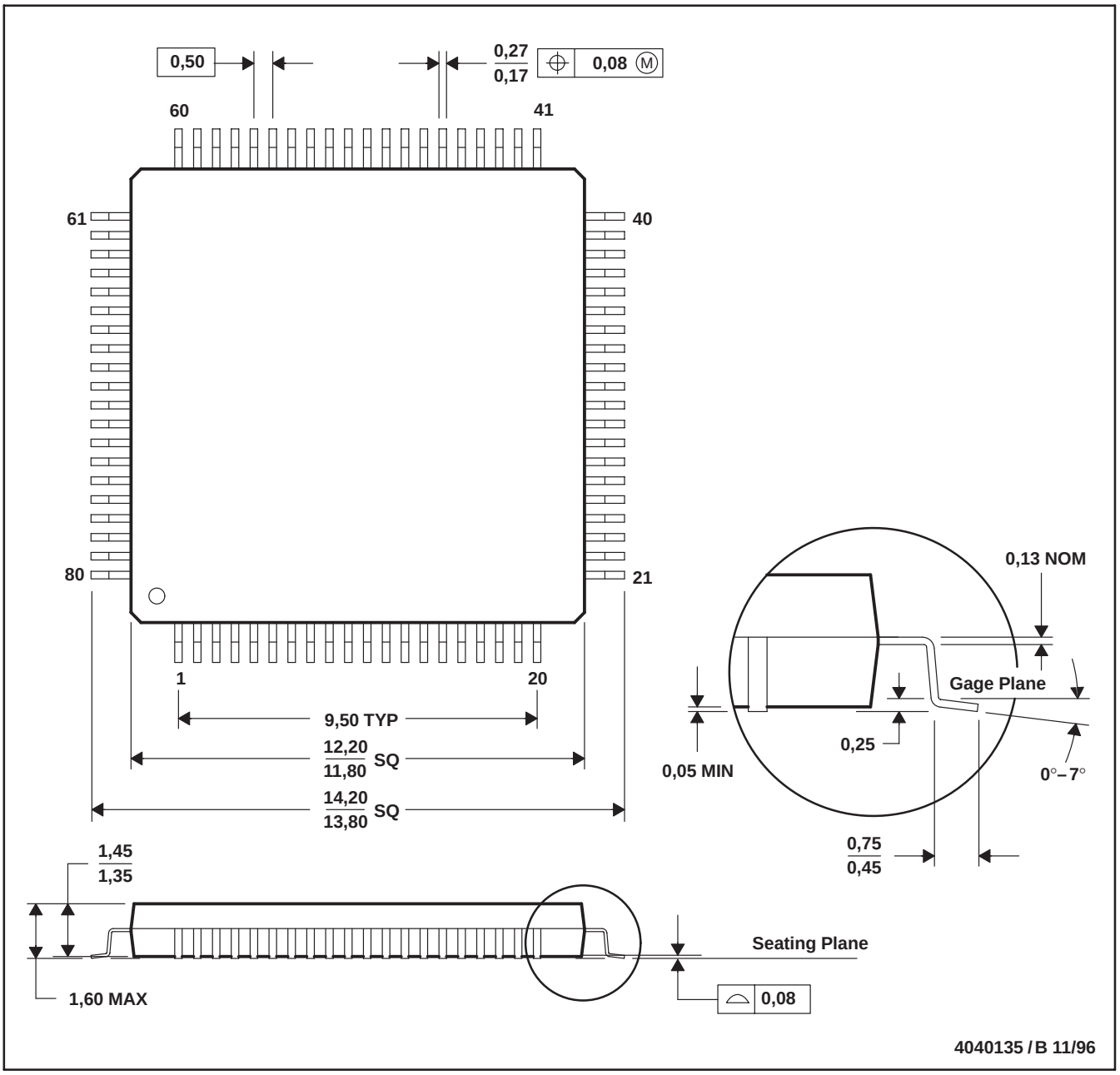
PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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