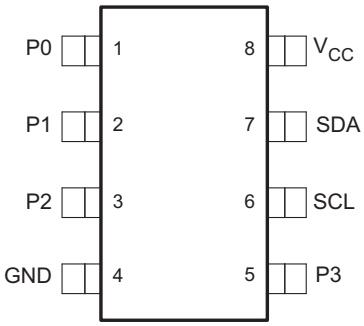
PCA9536
REMOTE 4-BIT I²C AND SMBus I/O EXPANDER WITH CONFIGURATION REGISTERS

SCPS125E–APRIL 2006–REVISED OCTOBER 2007

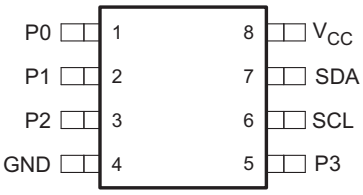
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Low Standby Current Consumption of 1 µA Max**
- **I²C to Parallel Port Expander**
- **Operating Power-Supply Voltage Range of 2.3 V to 5.5 V**
- **5-V Tolerant I/O Ports**
- **400-kHz Fast I²C Bus**
- **Input/Output Configuration Register**
- **Polarity Inversion Register**
- **Internal Power-On Reset**
- **No Glitch on Power Up**
- **Power-Up With All Channels Configured as Inputs**
- **Noise Filter on SCL/SDA Inputs**
- **Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

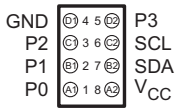
D PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	PCA9536YZPR	7CH
	SOIC – D	Reel of 2500	PCA9536DR	PD536
			PCA9536DRG4	
		Tube of 75	PCA9536D	
			PCA9536DG4	
		Reel of 250	PCA9536DT	
	VSSOP – DGK	Reel of 2500	PCA9536DGKR	7C_
			PCA9536DGKRG4	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This 4-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface [serial clock (SCL), serial data (SDA)].

The PCA9536 features 4-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to V_{CC}. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. If no signals are applied externally to the PCA9536, the voltage level is 1, or high, because of the internal pullup resistors. The data for each input or output is stored in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

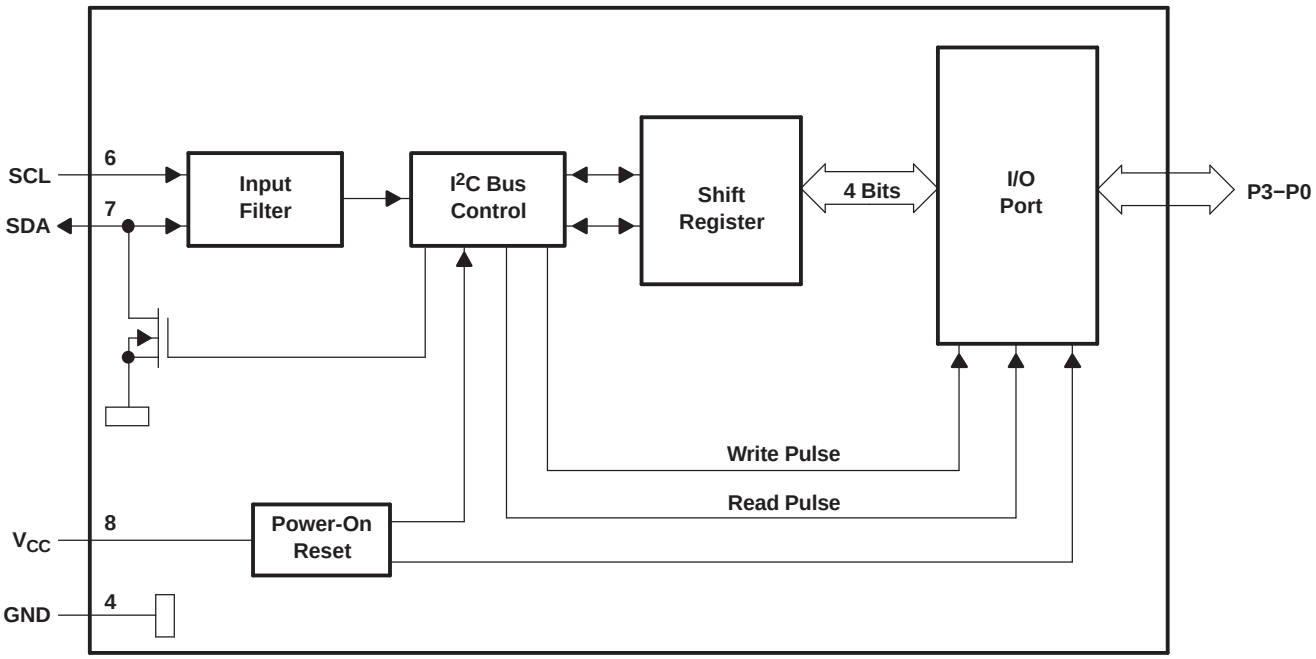
The system master can reset the PCA9536 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I^2C/SMBus state machine.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.

TERMINAL FUNCTIONS

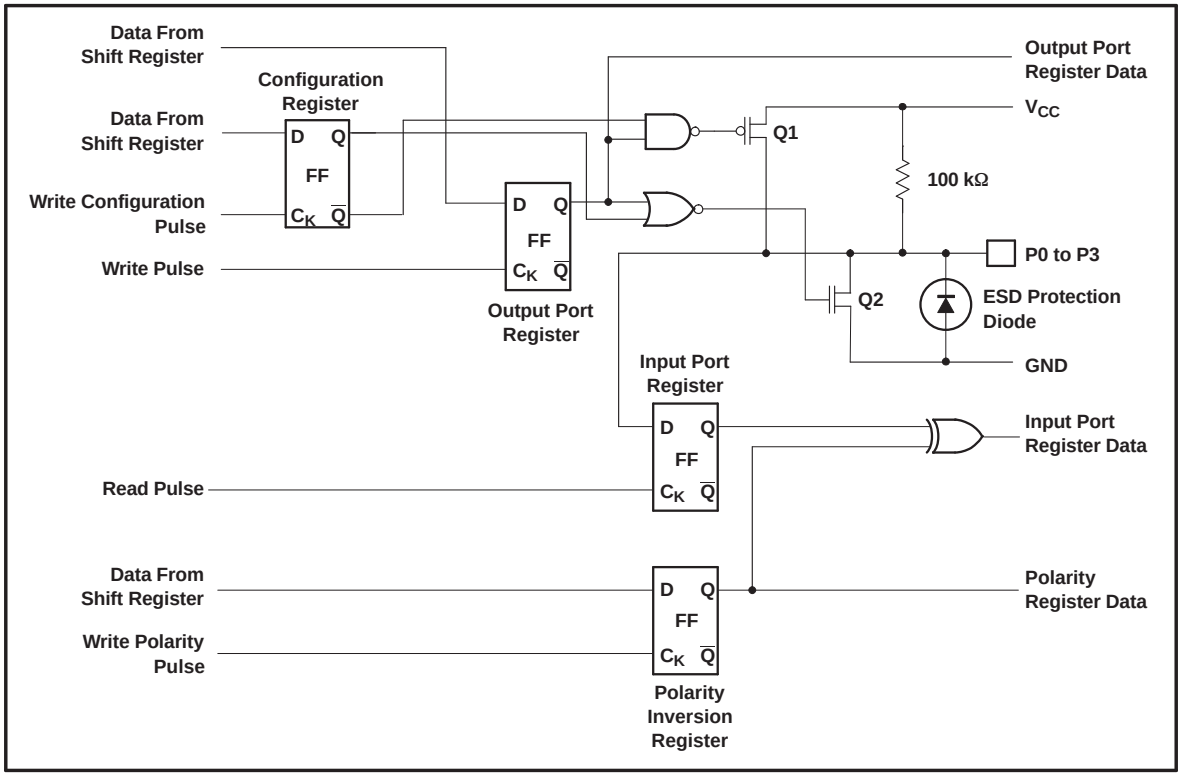
NO.	NAME	DESCRIPTION
1	P0	P-port input/output. Push-pull design structure.
2	P1	P-port input/output. Push-pull design structure.
3	P2	P-port input/output. Push-pull design structure.
4	GND	Ground
5	P3	P-port input/output. Push-pull design structure.
6	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
7	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
8	V_{CC}	Supply voltage

LOGIC DIAGRAM



A. All I/Os are set to inputs at reset.

SIMPLIFIED SCHEMATIC OF P0 TO P3



A. At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pullup (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

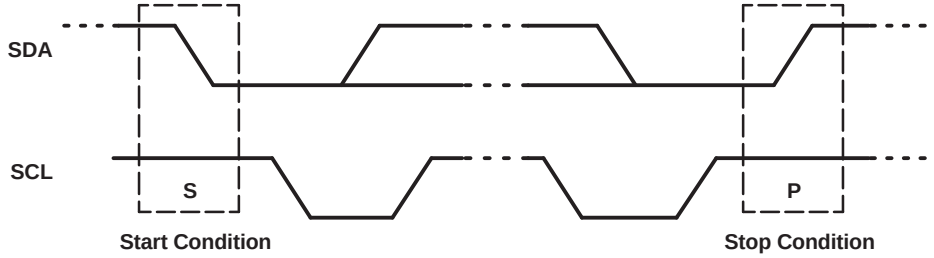


Figure 1. Definition of Start and Stop Conditions

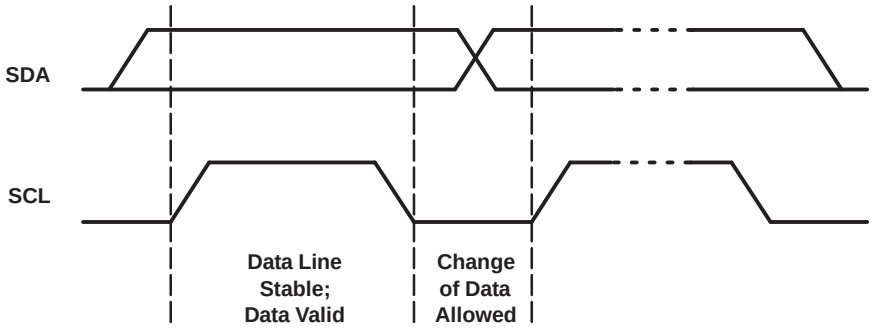


Figure 2. Bit Transfer

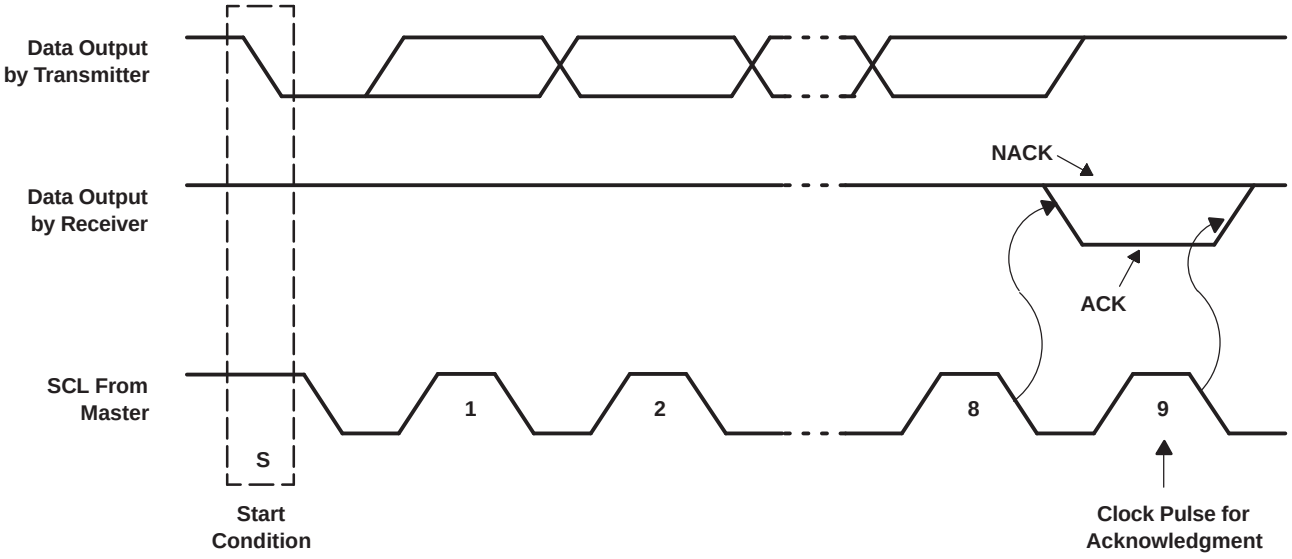


Figure 3. Acknowledgment on the I²C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	H	L	L	L	L	L	H	R/$\overline{W}$
Px I/O data bus	Does not affect operation of the PCA9536				P3	P2	P1	P0
	P7	P6	P5	P4				

Device Address

Figure 4 shows the address byte of the PCA9536.

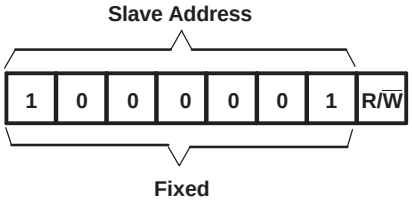


Figure 4. PCA9536 Address

The slave address equates to 65 (decimal) and 41 (hexadecimal).

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9536. Two bits of this data byte state the operation (read or write) and the internal register (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

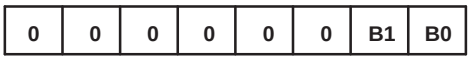


Figure 5. Control Register Bits

Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	1111 XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to instruct the I²C device that the Input Port register will be accessed next.

Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	Not Used							
DEFAULT	1	1	1	1	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
	Not Used							
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9536 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released and the PCA9536 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Bus Transactions

Data is exchanged between the master and PCA9536 through write and read commands.

Writes

Data is transmitted to the PCA9536 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see Figure 6 and Figure 7).

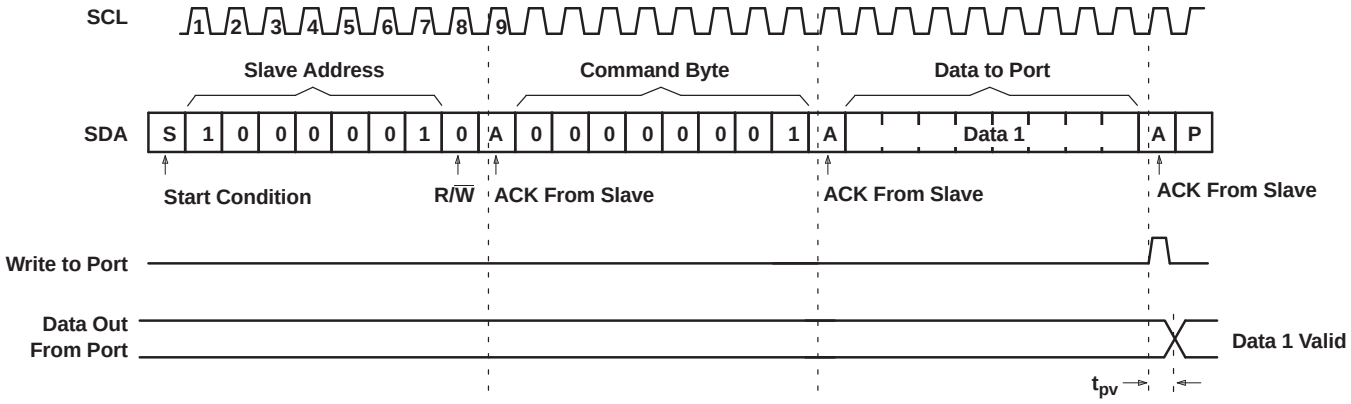


Figure 6. Write to Output Port Register

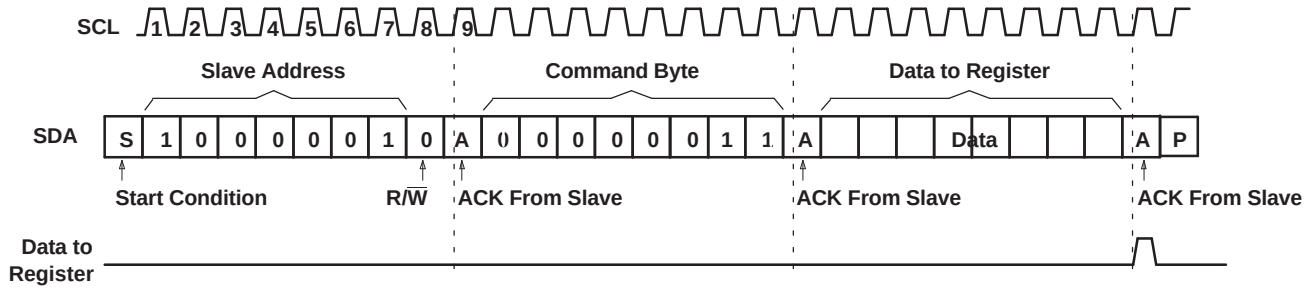


Figure 7. Write to Configuration or Polarity Inversion Registers

Reads

The bus master first must send the PCA9536 address with the LSB set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9536 (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

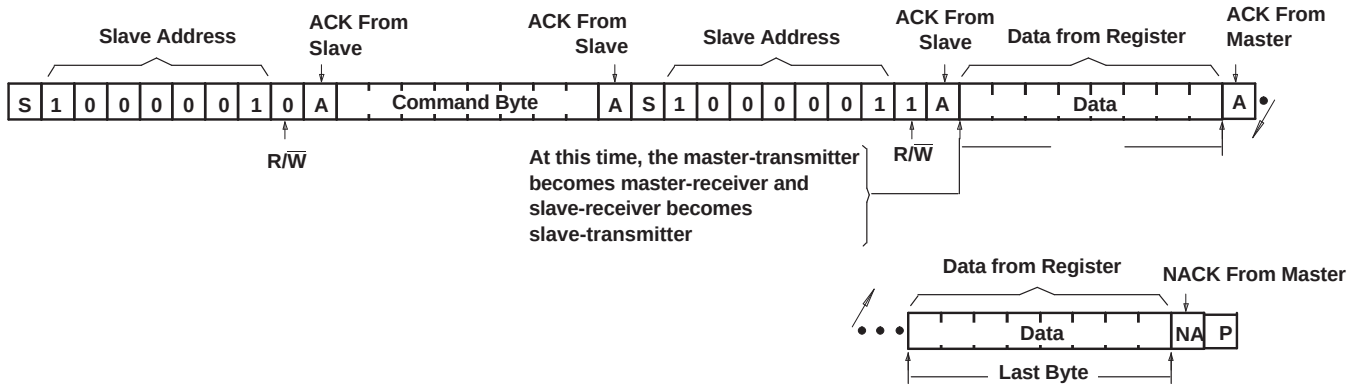
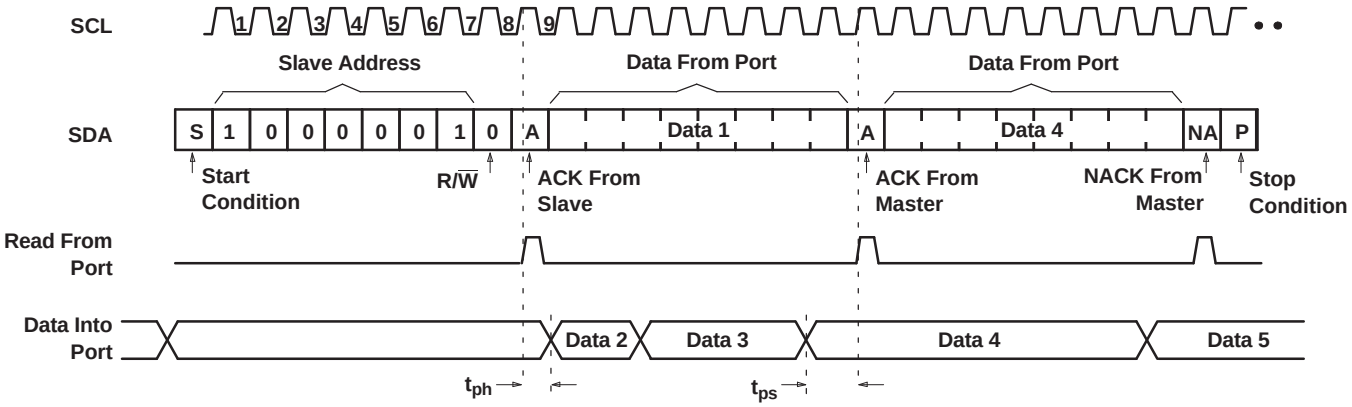


Figure 8. Read From Register



A. This figure assumes that the command byte previously has been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart, and the slave address call between the initial slave address call and actual data transfer from the P-port (see Figure 8).

Figure 9. Read Input Port Register

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–200	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance(3)	D package		97	°C/W
		DGK package		172	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		P3–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		P3–P0	–0.5	0.8	
I_{OH}	High-level output current	P3–P0		–10	mA
I_{OL}	Low-level output current	P3–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		mA
	P-port(3)	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	32		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	44		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
I_{IH}	P-port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P-port	V_I = GND	2.3 V to 5.5 V			–100	µA
I_{CC}	Operating mode	$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 400 kHz	5.5 V		73	150	µA
			3.6 V		9	50	
			2.7 V		7	30	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 100 kHz	5.5 V		14	25	
			3.6 V		9	20	
			2.7 V		6	15	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		225	350	
			3.6 V		175	250	
			2.7 V		125	200	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			0.35	mA
		Every LED I/O at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			0.4	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5	6.5	pF
	P-port				7.5	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be limited externally to a maximum of 25 mA, and the P-port (P3–P0) must be limited to a maximum current of 100 mA.

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 10)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}	I²C spike time		50		50	ns
t_{sds}	I²C serial-data setup time	250		100		ns
t_{sdh}	I²C serial-data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold time	4		0.6		µs
t_{sps}	I²C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		1		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		0.9	µs
C_b	I²C bus capacitive load		400		400	pF

(1) C_b = Total capacitive load of one bus in pF

Switching Characteristics

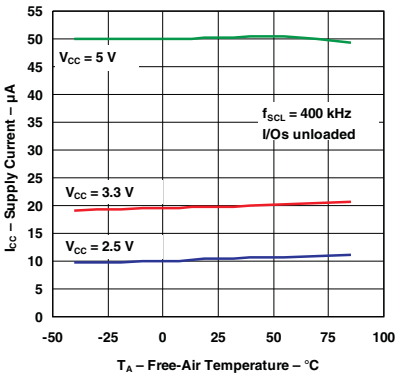
over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{pv}	Output data valid	SCL	P3–P0		200		200	ns
t_{ps}	Input data setup time	P-port	SCL	100		100		ns
t_{ph}	Input data hold time	P-port	SCL	1		1		µs

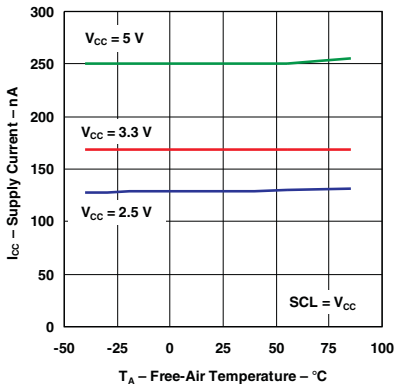
TYPICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

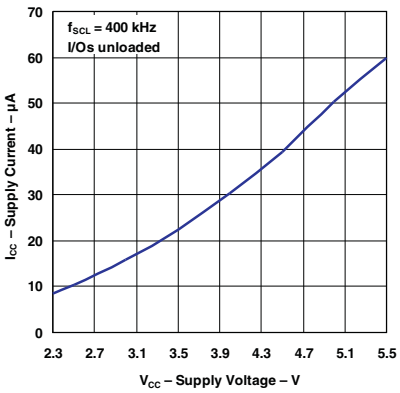
SUPPLY CURRENT VS TEMPERATURE



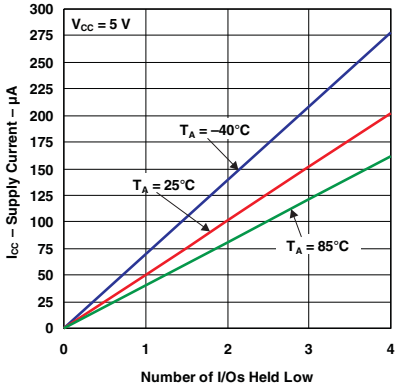
QUIESCENT SUPPLY CURRENT VS TEMPERATURE



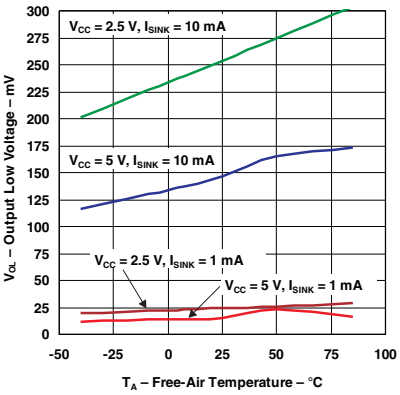
SUPPLY CURRENT VS SUPPLY VOLTAGE



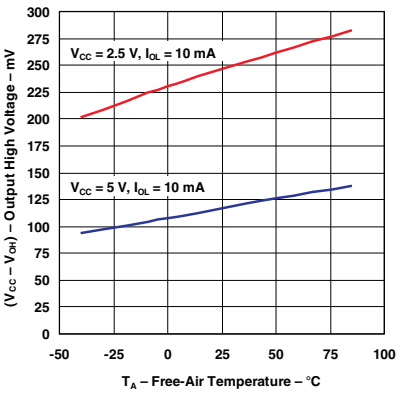
SUPPLY CURRENT VS NUMBER OF I/Os HELD LOW



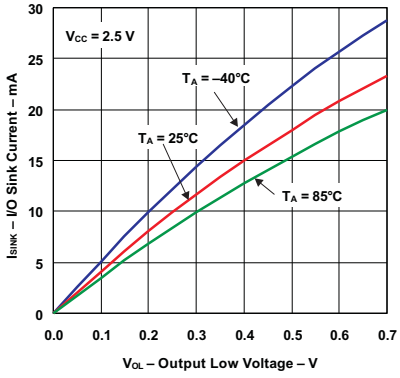
I/O OUTPUT LOW VOLTAGE VS TEMPERATURE



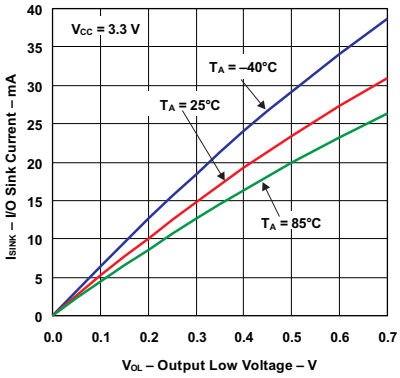
I/O OUTPUT HIGH VOLTAGE VS TEMPERATURE



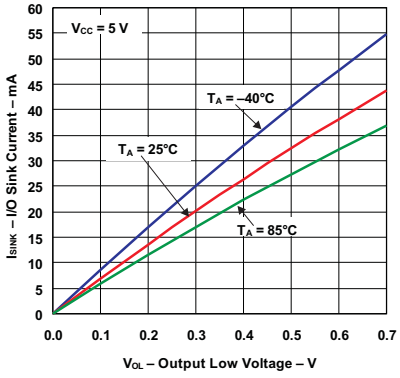
I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



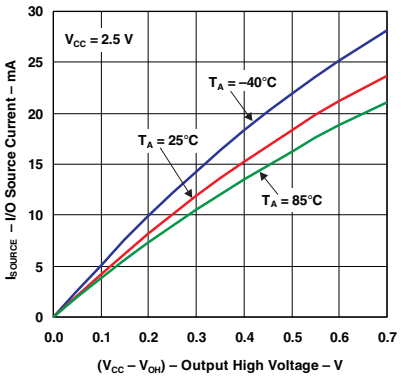
I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



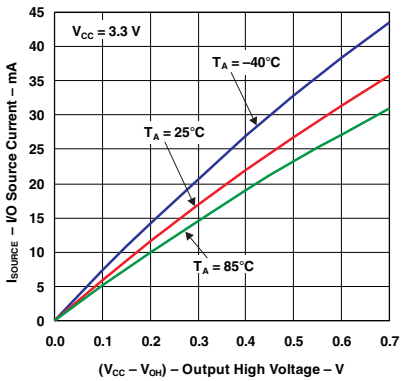
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

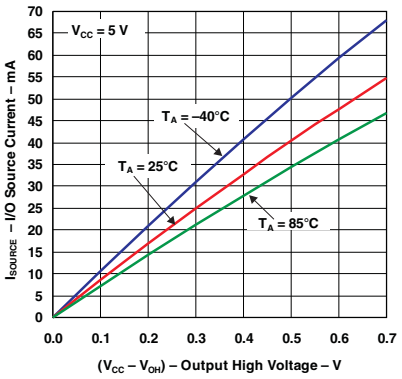
I/O SOURCE CURRENT VS OUTPUT HIGH VOLTAGE



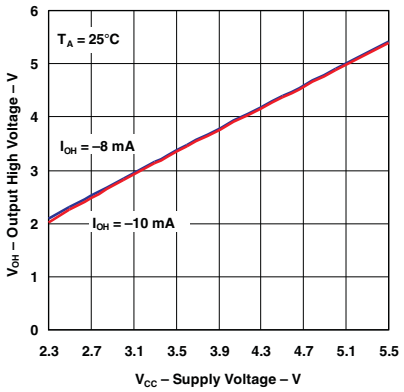
I/O SOURCE CURRENT VS OUTPUT HIGH VOLTAGE



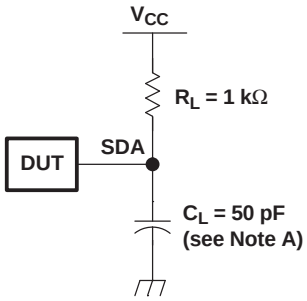
I/O SOURCE CURRENT VS OUTPUT HIGH VOLTAGE



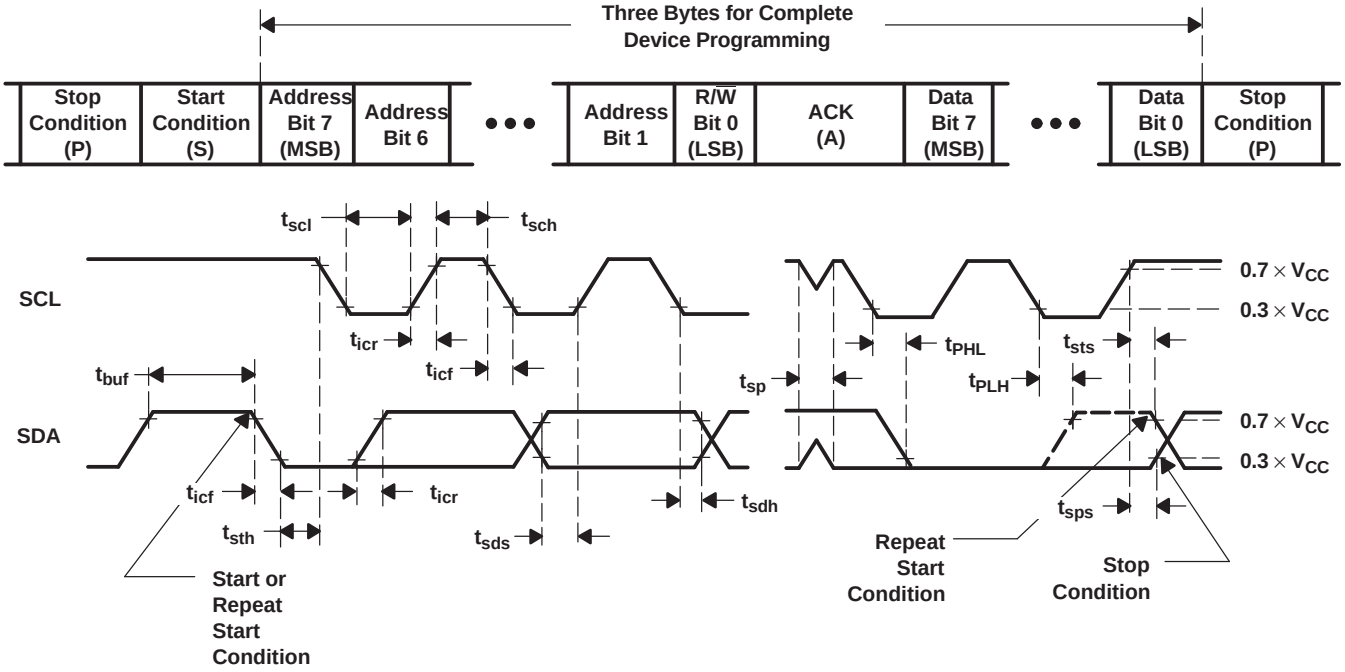
OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

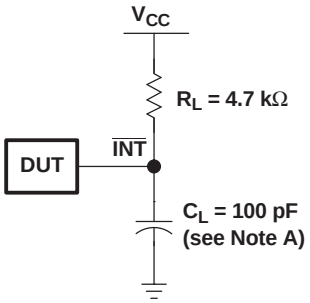
A. C_L include probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

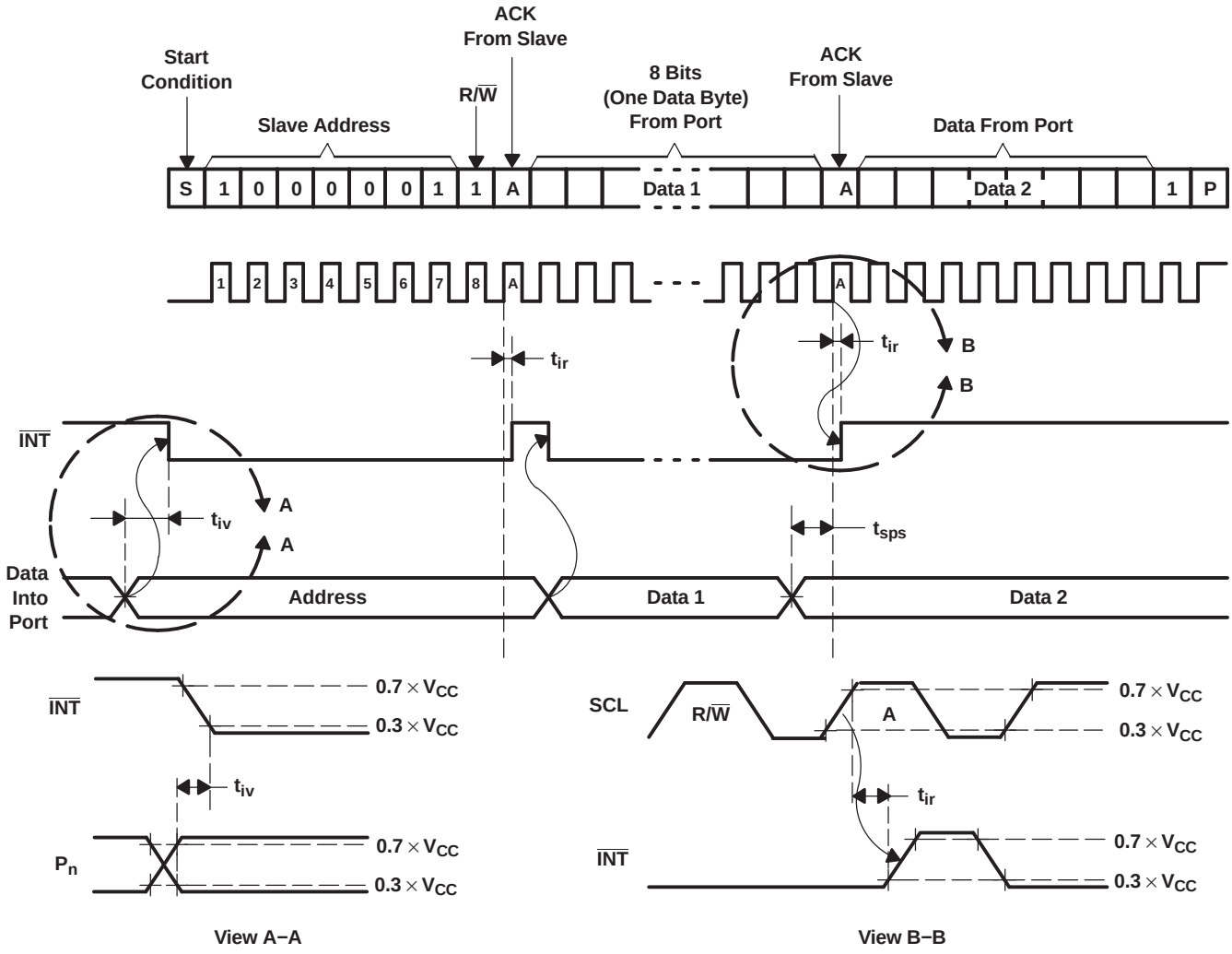
C. All parameters and waveforms are not applicable to all devices.

Figure 10. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION



View A–A

View B–B

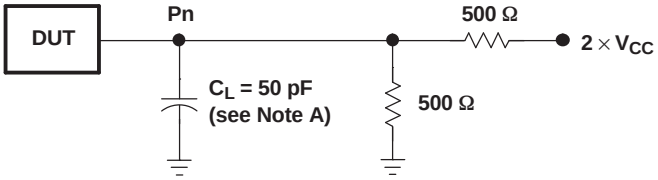
A. C_L include probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

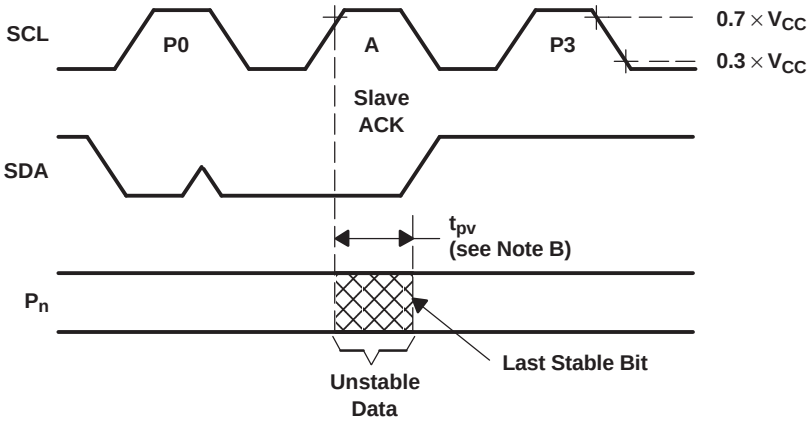
C. All parameters and waveforms are not applicable to all devices.

Figure 11. Interrupt Load Circuit and Voltage Waveforms

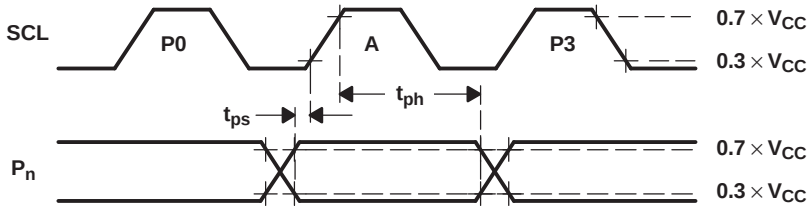
PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)

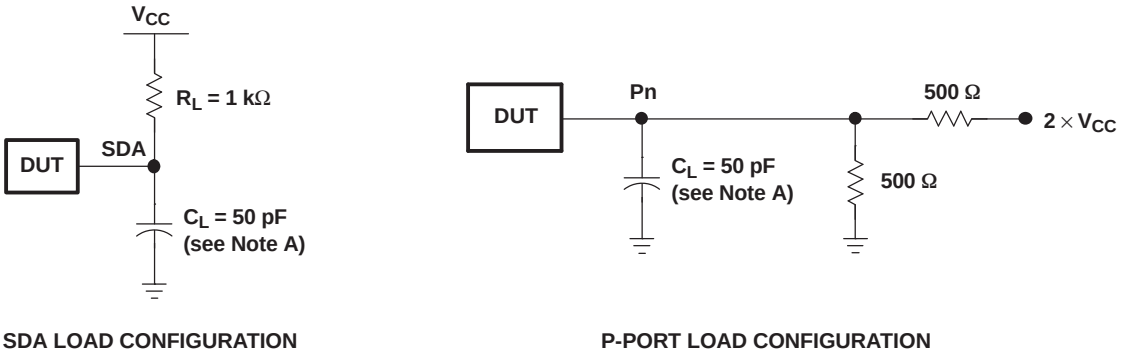


READ MODE (R/$\overline{W}$ = 1)

A. C_L include probe and jig capacitance.
B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

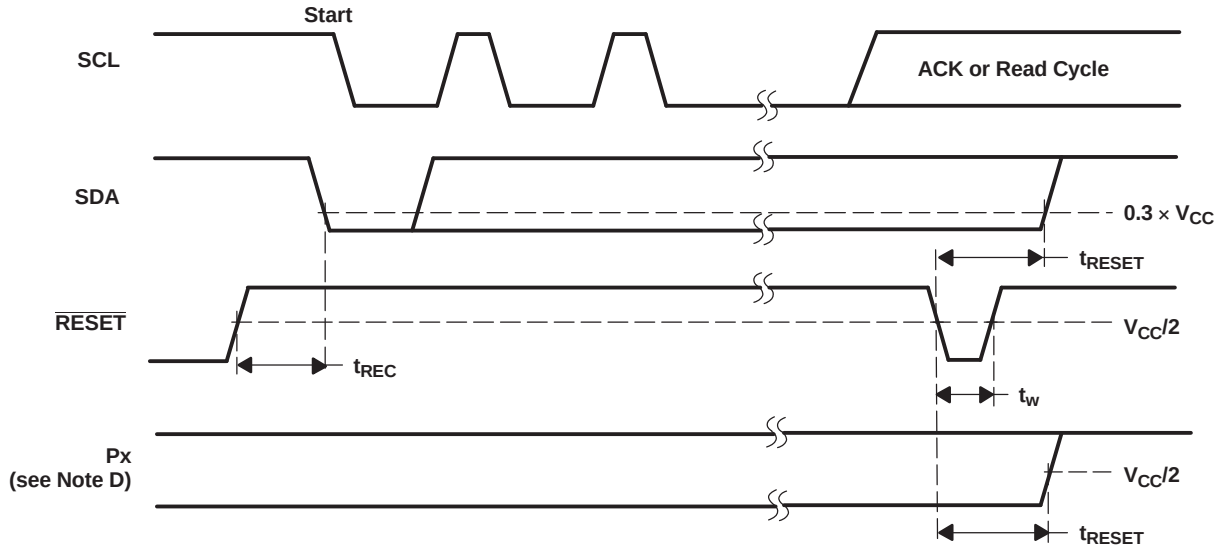
Figure 12. P-Port Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION



A. C_L include probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

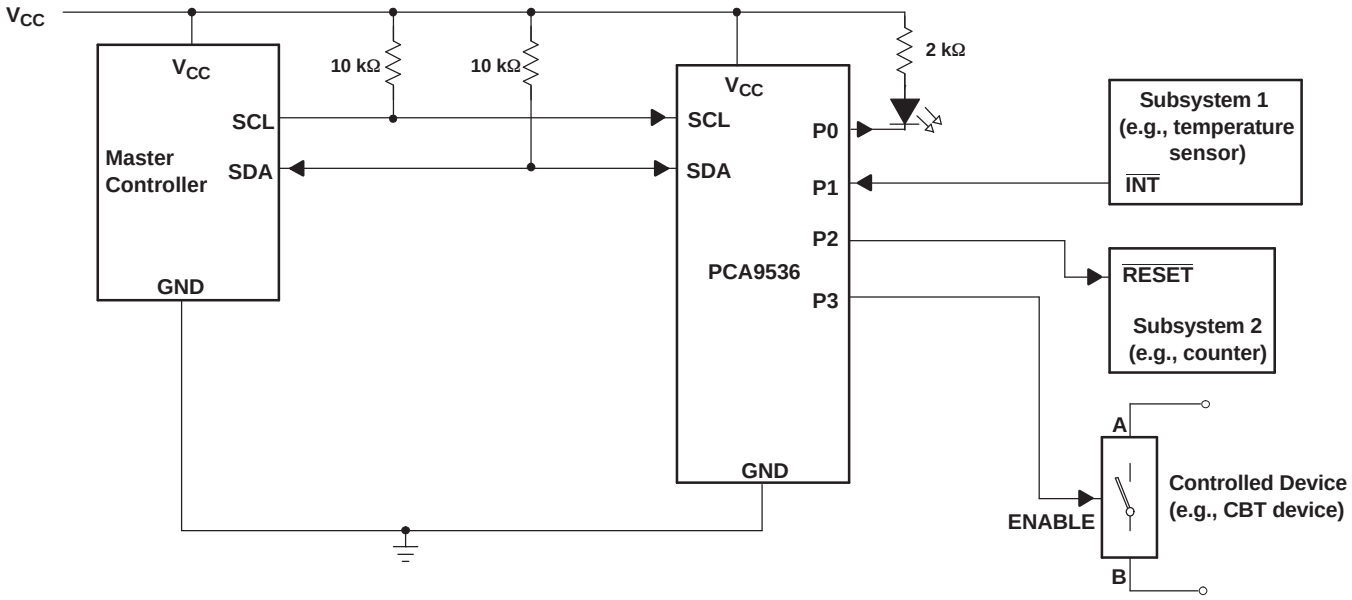
D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 13. Reset Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9536 can be used.



A. Device address is 10000001.
B. P0, P2, and P3 are configured as outputs.
C. P1 is configured as an input.

Figure 14. Typical Application

Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 14. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

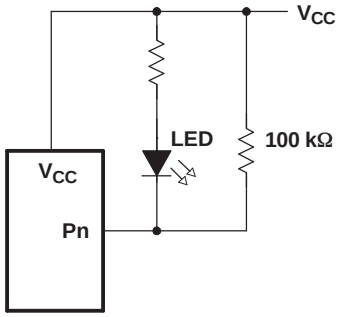


Figure 15. High-Value Resistor in Parallel With the LED

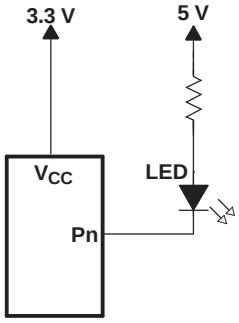


Figure 16. Device Supplied by a Lower Voltage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCA9536D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9536DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9536DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9536DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9536DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9536DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

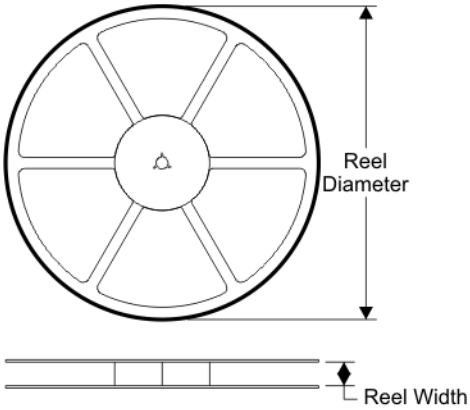
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

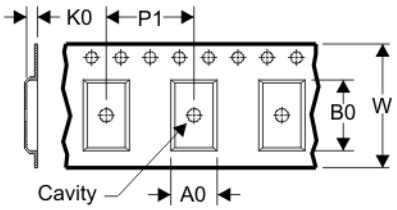
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

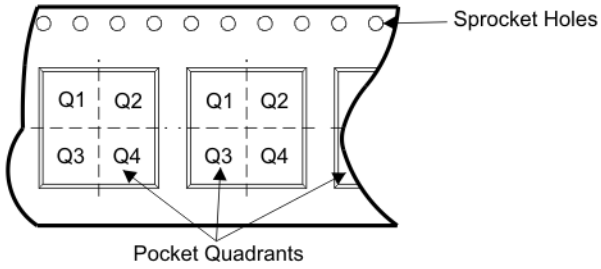


TAPE DIMENSIONS



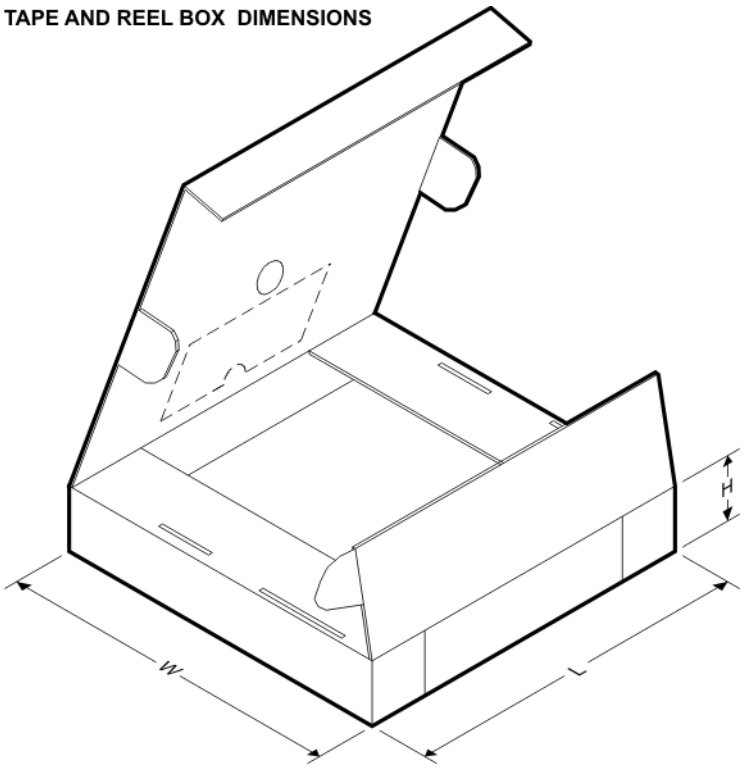
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



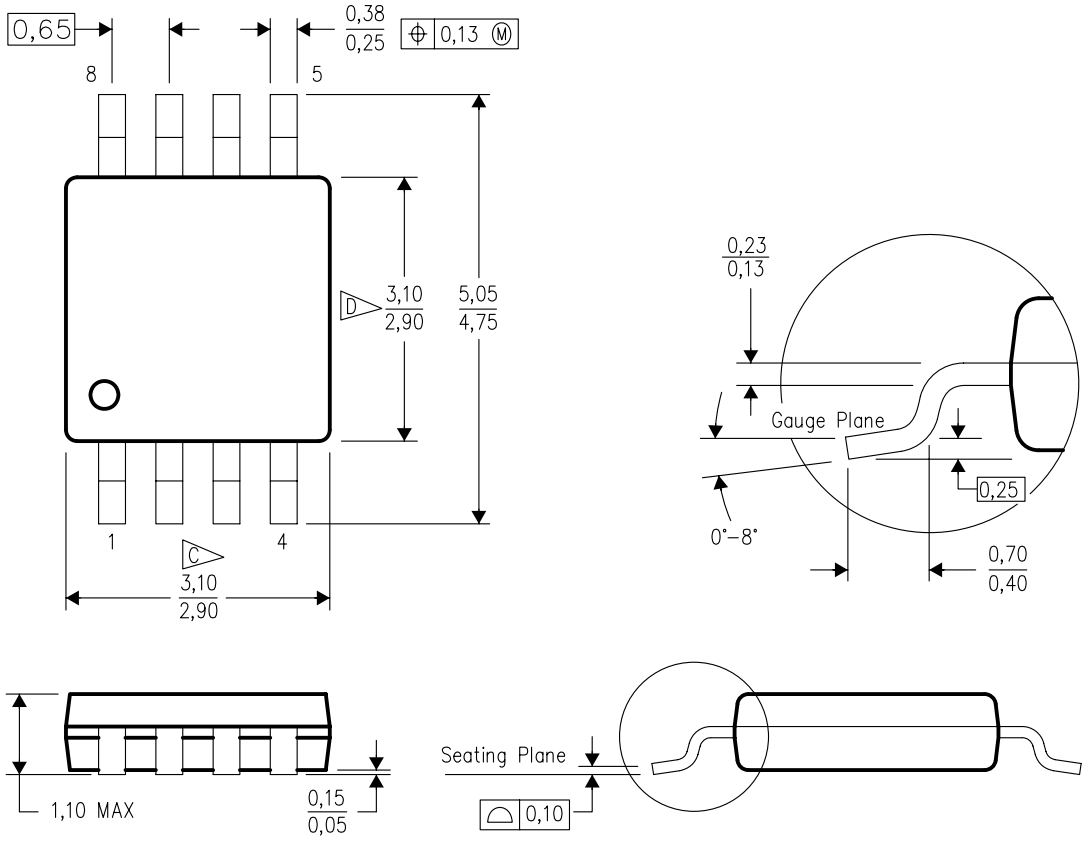
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9536DGKR	DGK	8	SITE 35	330	13	5.3	3.4	1.4	8	12	Q1
PCA9536DR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1
PCA9536DR	D	8	SITE 41	330	12	6.4	5.2	2.1	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
PCA9536DGKR	DGK	8	SITE 35	358.0	335.0	35.0
PCA9536DR	D	8	SITE 27	342.9	336.6	20.64
PCA9536DR	D	8	SITE 41	346.0	346.0	29.0

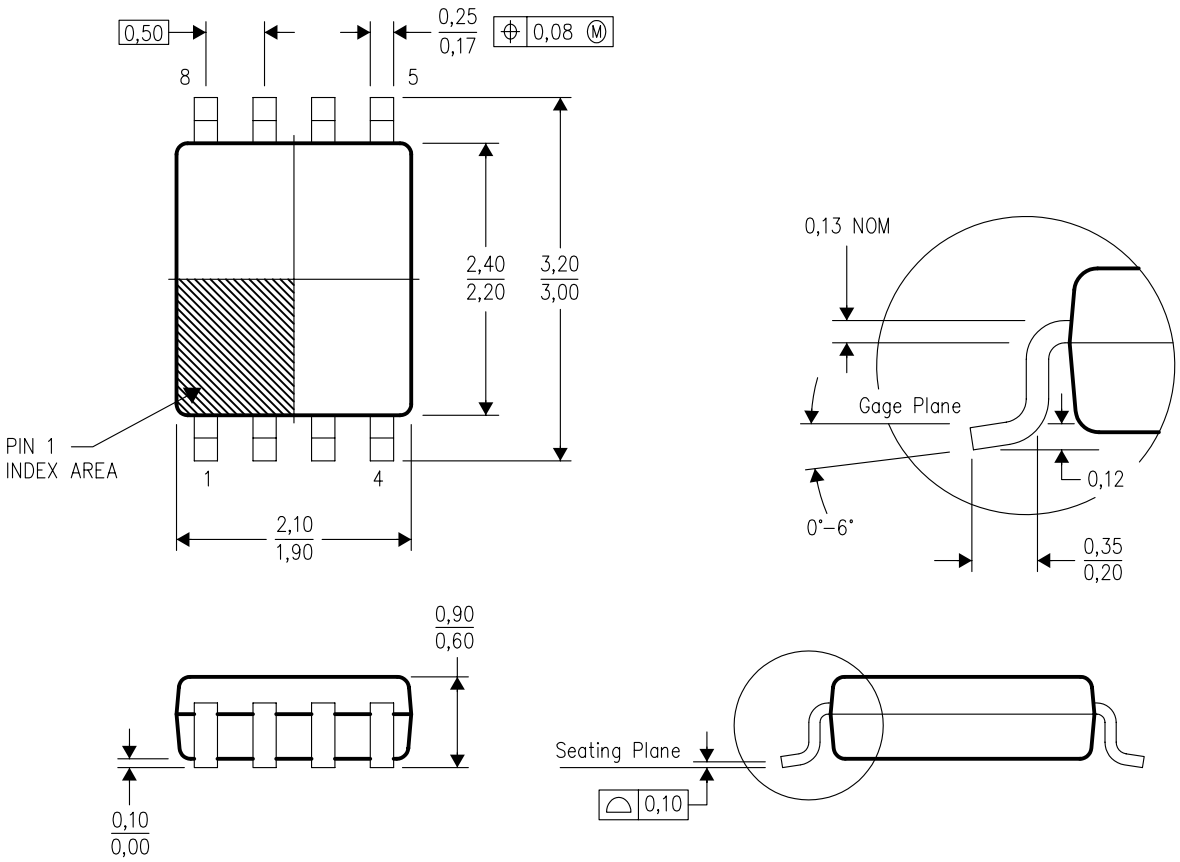
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

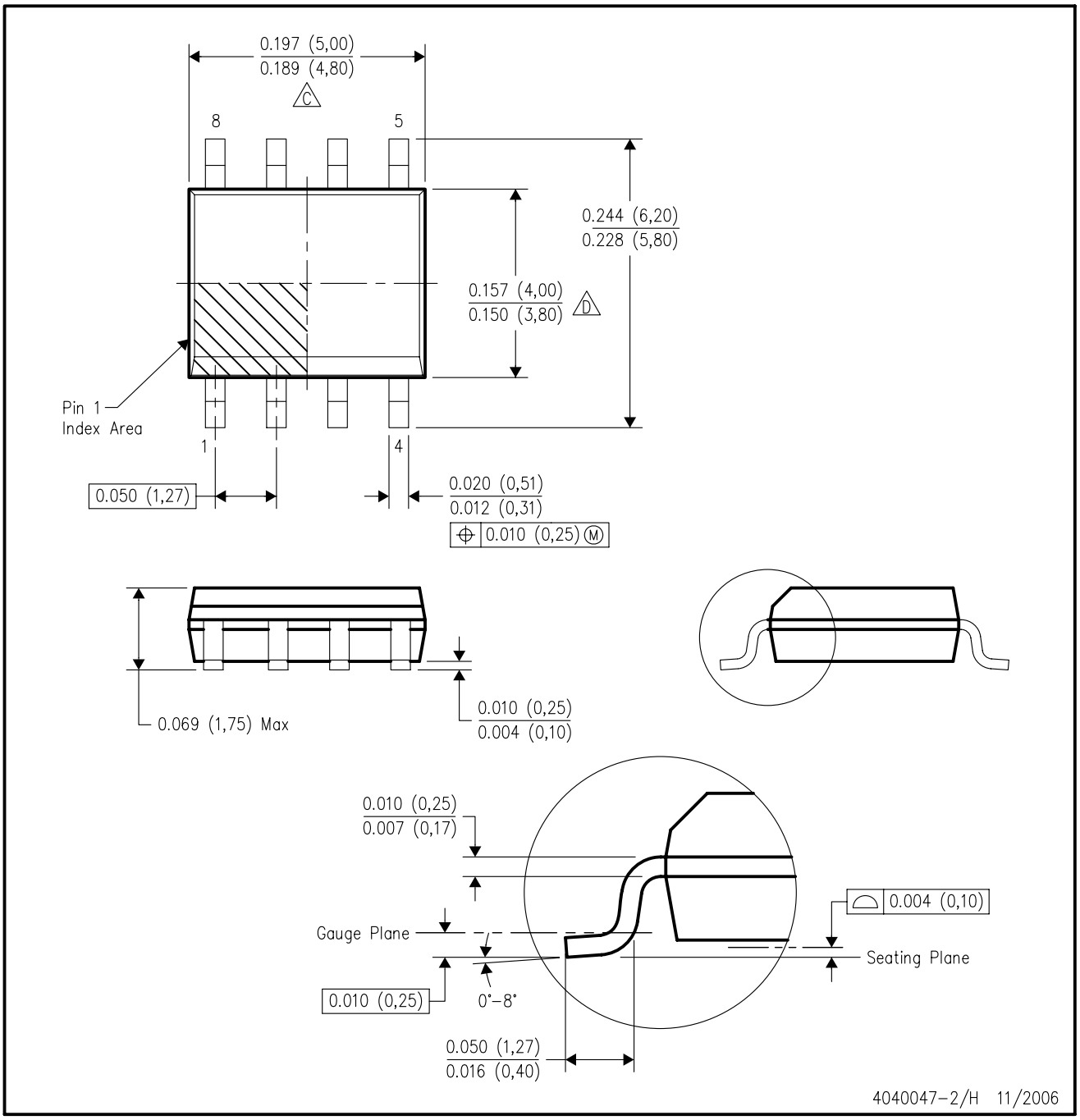
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

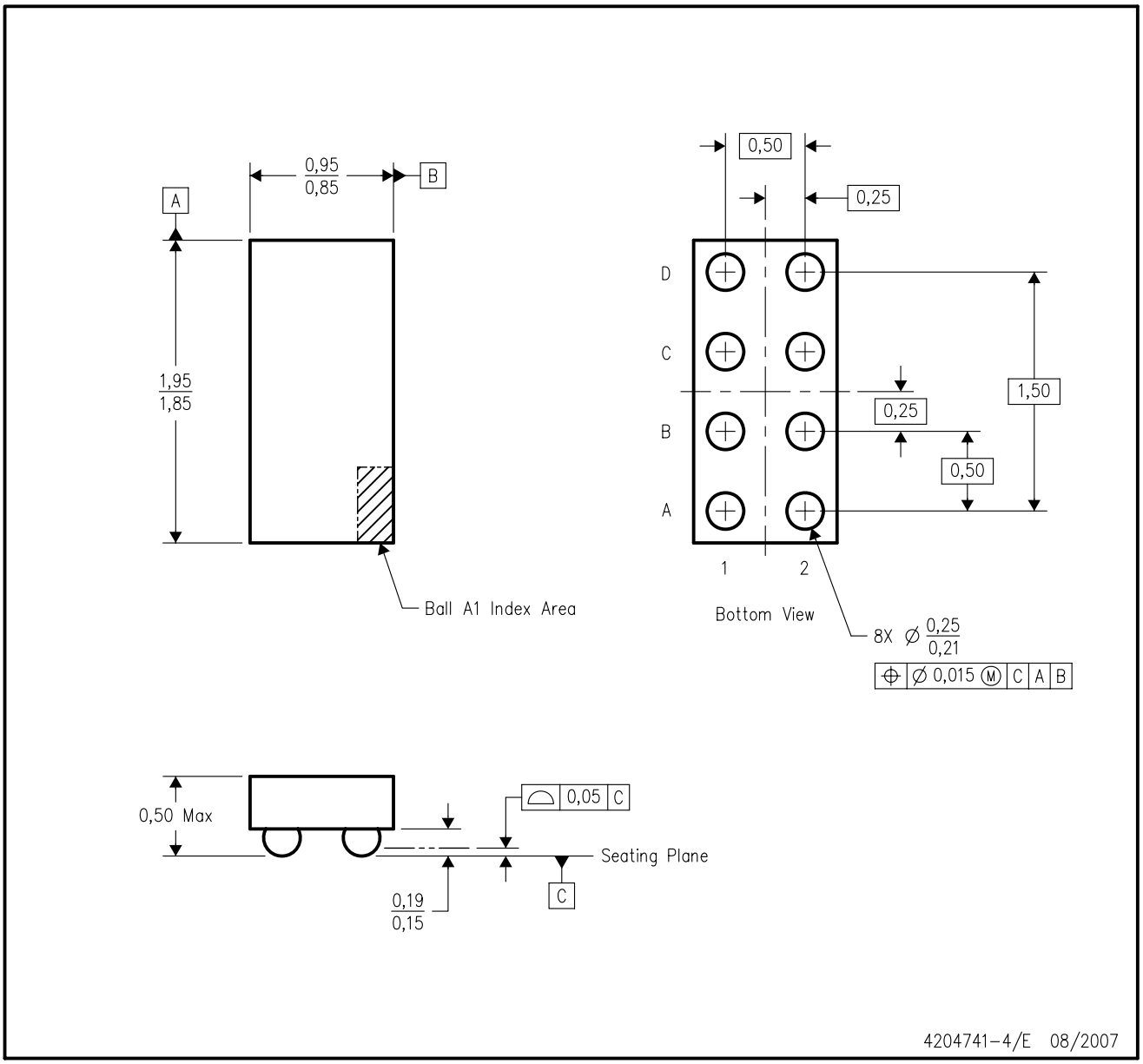
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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