PCA9539

REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS

SCPS130D−AUGUST 2005−REVISED MARCH 2007
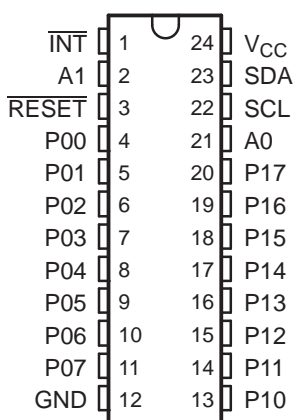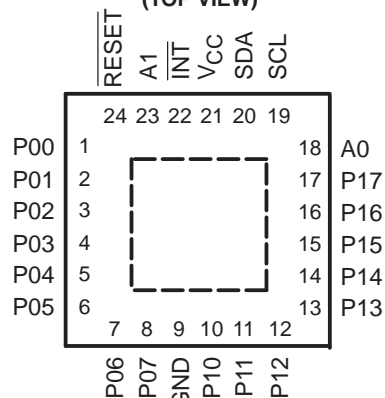
FEATURES

- **Low Standby-Current Consumption of 1 μA Max**
- **I²C to Parallel Port Expander**
- **Open-Drain Active-Low Interrupt Output**
- **Active-Low Reset Input**
- **5-V Tolerant I/O Ports**
- **Compatible With Most Microcontrollers**
- **400-kHz Fast I²C Bus**
- **Polarity Inversion Register**

- **Address by Two Hardware Address Pins for Use of up to Four Devices**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

$\overline{INT}$	1	24	V_{CC}
A1	2	23	SDA
$\overline{RESET}$	3	22	SCL
P00	4	21	A0
P01	5	20	P17
P02	6	19	P16
P03	7	18	P15
P04	8	17	P14
P05	9	16	P13
P06	10	15	P12
P07	11	14	P11
GND	12	13	P10

RGE PACKAGE
(TOP VIEW)

Top pins (24 23 22 21 20 19): $\overline{RESET}$, A1, $\overline{INT}$, V_{CC}, SDA, SCL

Left	Pin	Pin	Right
P00	1	18	A0
P01	2	17	P17
P02	3	16	P16
P03	4	15	P15
P04	5	14	P14
P05	6	13	P13

Bottom pins (7 8 9 10 11 12): P06, P07, GND, P10, P11, P12

DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DB	Reel of 2000	PCA9539DBR	PCA9539
		Tube of 60	PCA9539DB	
	QSOP – DBQ	Reel of 2500	PCA9539DBQR	PD9539
	TVSOP – DGV	Reel of 2000	PCA9539DGVR	PD9539
	SOIC – DW	Tube of 25	PCA9539DW	PCA9539
		Reel of 2000	PCA9539DWR	
	TSSOP – PW	Tube of 60	PCA9539PW	PD9539
		Reel of 1200	PCA9539PWR	
		Reel of 250	PCA9539PWT	
	QFN – RGE	Reel of 3000	PCA9539RGER	PD9539

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

![Warning icon] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PCA9539
REMOTE 16-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS
INSTRUMENTS
www.ti.com

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This 16-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL), serial data (SDA)].

The PCA9539 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9539 in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I^{2}C/SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset/initialization to occur without depowering the part.

The PCA9539 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^{2}C bus. Thus, the PCA9539 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The PCA9539 is identical to the PCA9555, except for the removal of the internal I/O pullup resistor, which greatly reduces power consumption when the I/Os are held low, replacement of A2 with $\overline{\text{RESET}}$, and a different address range.

Two hardware pins (A0 and A1) are used to program and vary the fixed I^{2}C address and allow up to four devices to share the same I^{2}C bus or SMBus.

TERMINAL FUNCTIONS

NO. SOIC (DW), SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	NO. QFN (RGE)	NAME	DESCRIPTION
1	22	$\overline{\text{INT}}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	23	A1	Address input. Connect directly to V_{CC} or ground.
3	24	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
4	1	P00	P-port input/output. Push-pull design structure.
5	2	P01	P-port input/output. Push-pull design structure.
6	3	P02	P-port input/output. Push-pull design structure.
7	4	P03	P-port input/output. Push-pull design structure.
8	5	P04	P-port input/output. Push-pull design structure.
9	6	P05	P-port input/output. Push-pull design structure.
10	7	P06	P-port input/output. Push-pull design structure.
11	8	P07	P-port input/output. Push-pull design structure.
12	9	GND	Ground
13	10	P10	P-port input/output. Push-pull design structure.
14	11	P11	P-port input/output. Push-pull design structure.
15	12	P12	P-port input/output. Push-pull design structure.
16	13	P13	P-port input/output. Push-pull design structure.
17	14	P14	P-port input/output. Push-pull design structure.
18	15	P15	P-port input/output. Push-pull design structure.
19	16	P16	P-port input/output. Push-pull design structure.
20	17	P17	P-port input/output. Push-pull design structure.
21	18	A0	Address input. Connect directly to V_{CC} or ground.
22	19	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
23	20	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
24	21	V_{CC}	Supply voltage

TEXAS INSTRUMENTS
www.ti.com

LOGIC DIAGRAM (POSITIVE LOGIC)
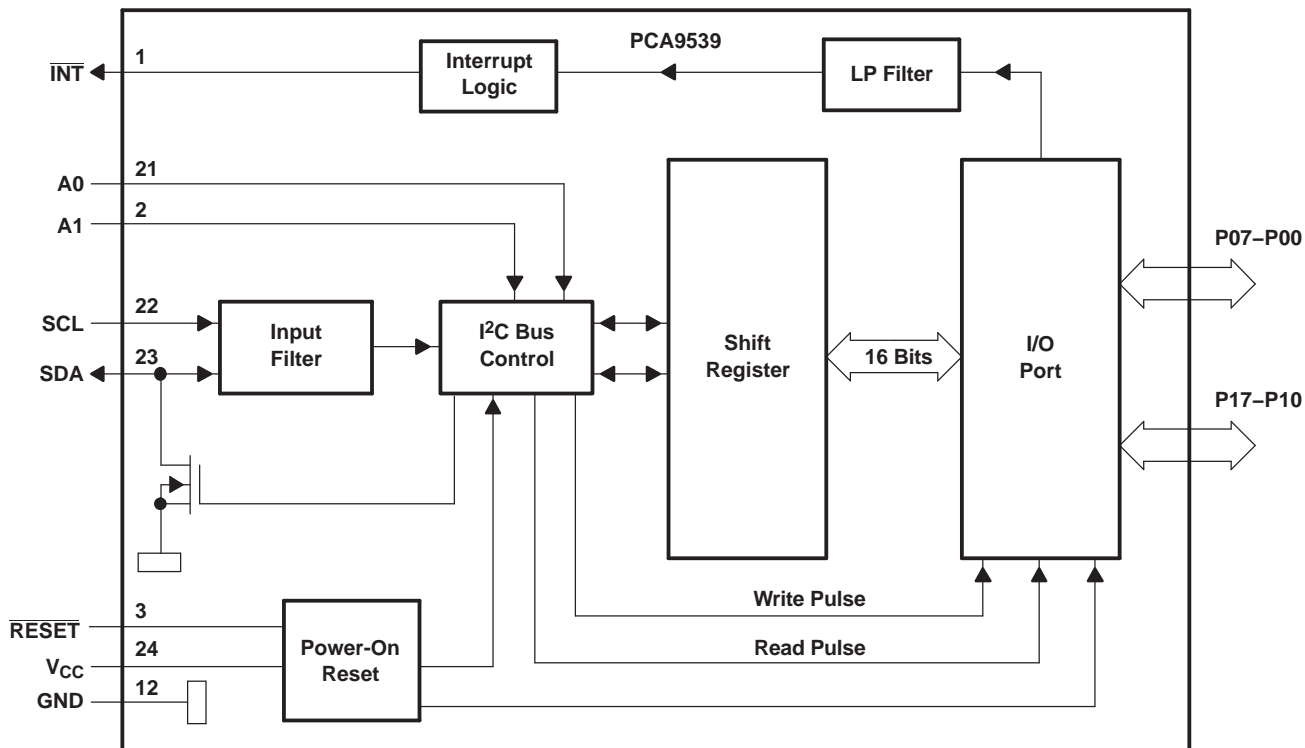
A.   Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

B.   All I/Os are set to inputs at reset.

SIMPLIFIED SCHEMATIC OF P-PORT I/Os[(1)]
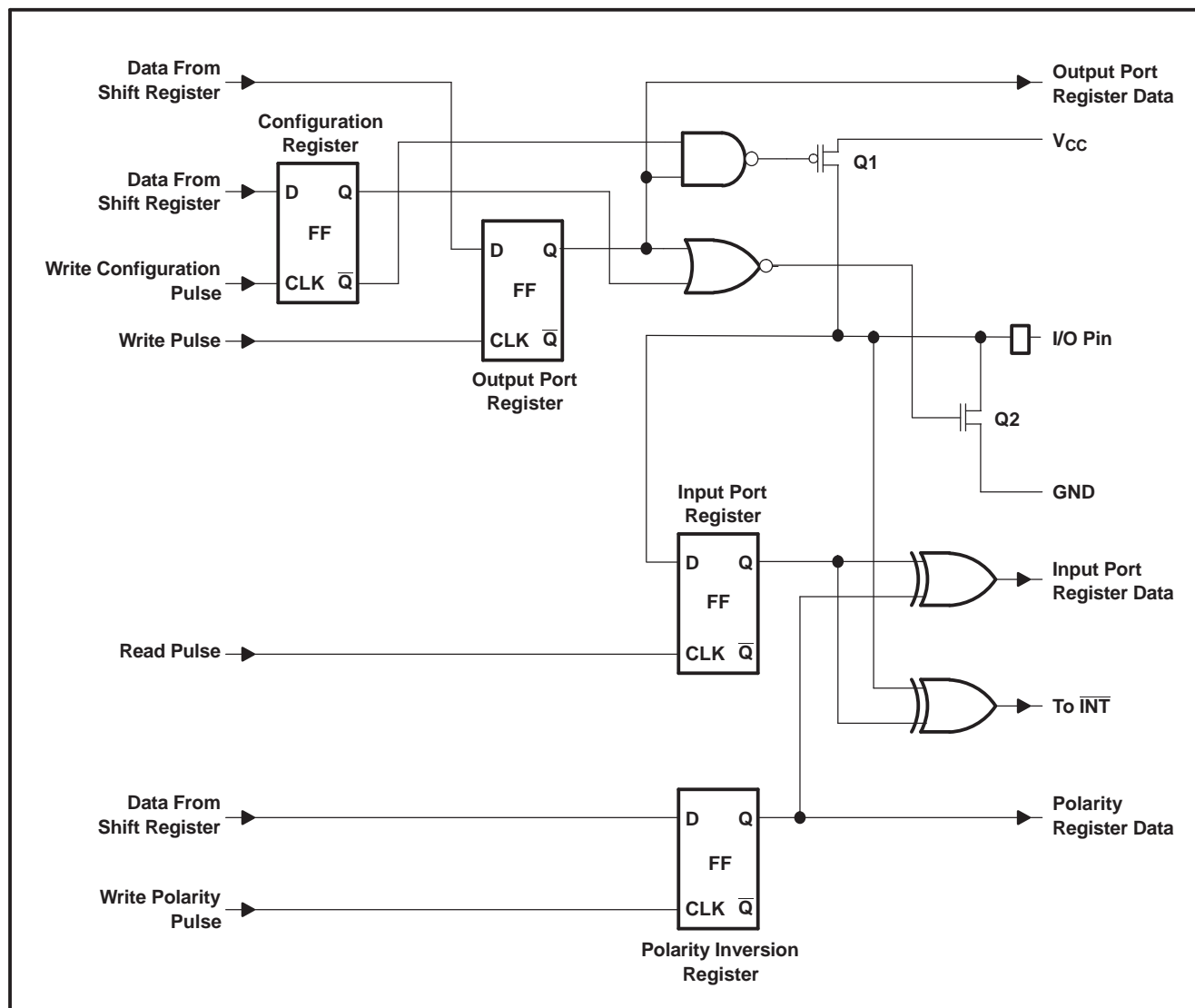
(1) At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS

TEXAS INSTRUMENTS
www.ti.com

SCPS130D−AUGUST 2005−REVISED MARCH 2007

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 and A1) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
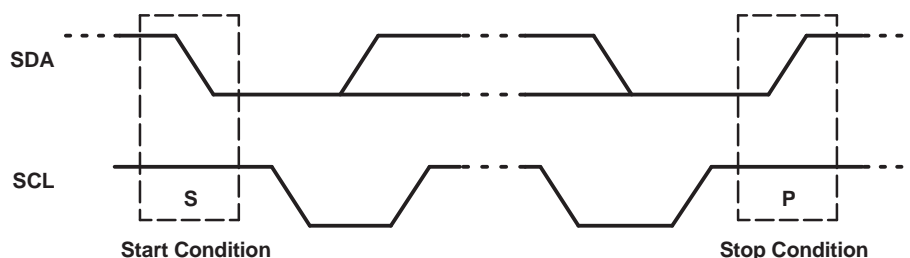

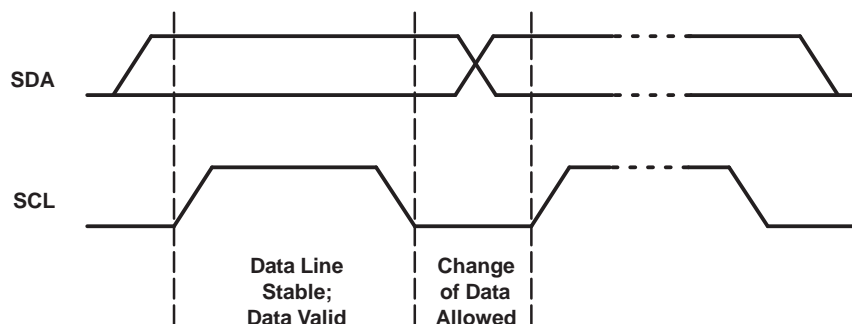**Figure 1. Definition of Start and Stop Conditions**
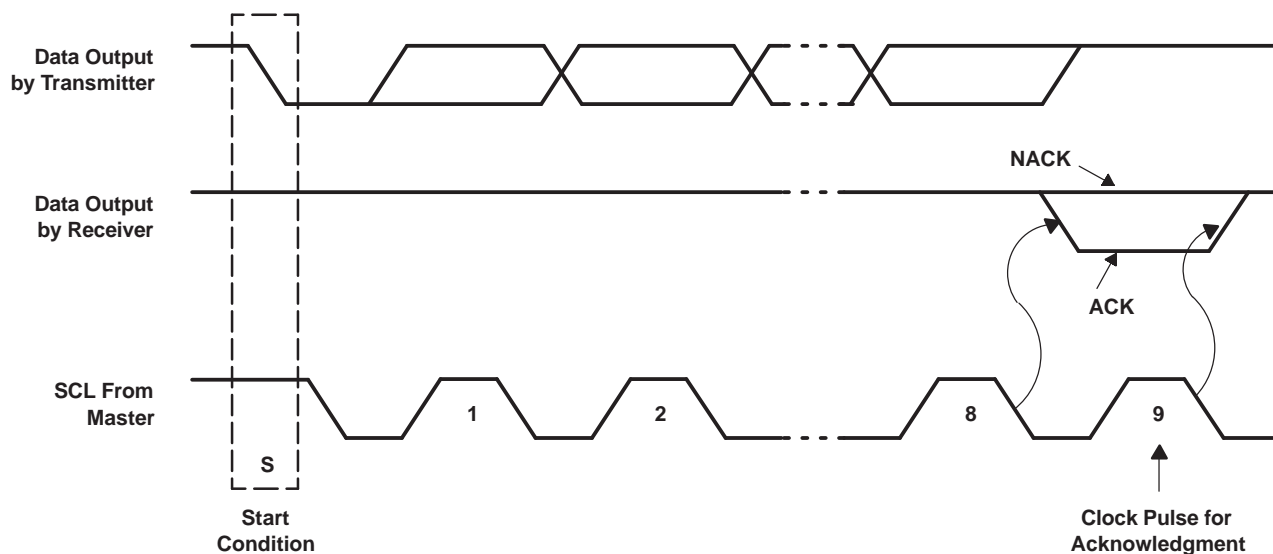

Figure 2. Bit Transfer

Figure 3. Acknowledgment on I²C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	H	H	H	L	H	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS
INSTRUMENTS
www.ti.com

Device Address

Figure 4 shows the address byte of the PCA9539.
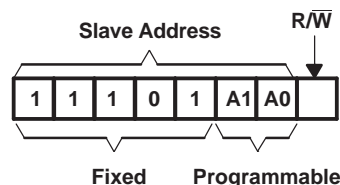
Figure 4. PCA9539 Address

Address Reference

INPUTS		I²C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9539. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.
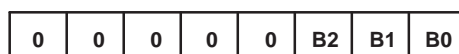

Figure 5. Control Register Bits

Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I²C device that the Input Port register will be accessed next.

Registers 0 and 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Registers 2 and 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (Registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Registers 4 and 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Registers 6 and 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9539 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9539 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

**TEXAS
INSTRUMENTS**
www.ti.com

$\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA9539 registers and I²C/SMBus state machine are held in their default states until $\overline{\text{RESET}}$ is once again high. This input requires a pullup resistor to V_{CC}, if no active connection is used.

Interrupt ($\overline{\text{INT}}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt, or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) bit or not acknowledge (NACK) bit after the falling edge of the SCL signal. In a Stop event, $\overline{\text{INT}}$ is cleared after the rising edge of SDA. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{\text{INT}}$ has an open-drain structure and requires a pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and PCA9539 through write and read commands.

Writes

Data is transmitted to the PCA9539 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9539 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports, and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 6 and Figure 7). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.
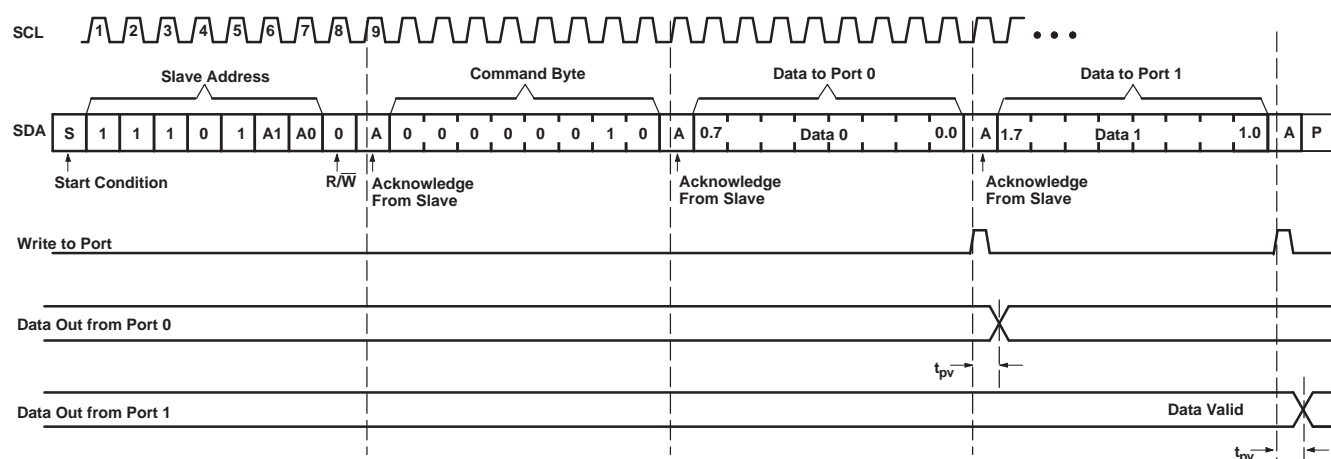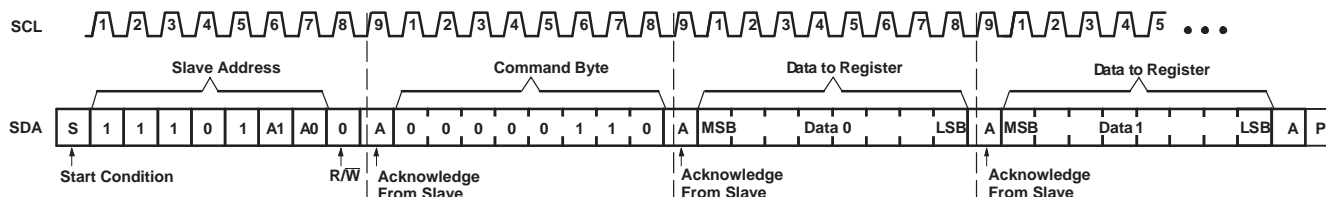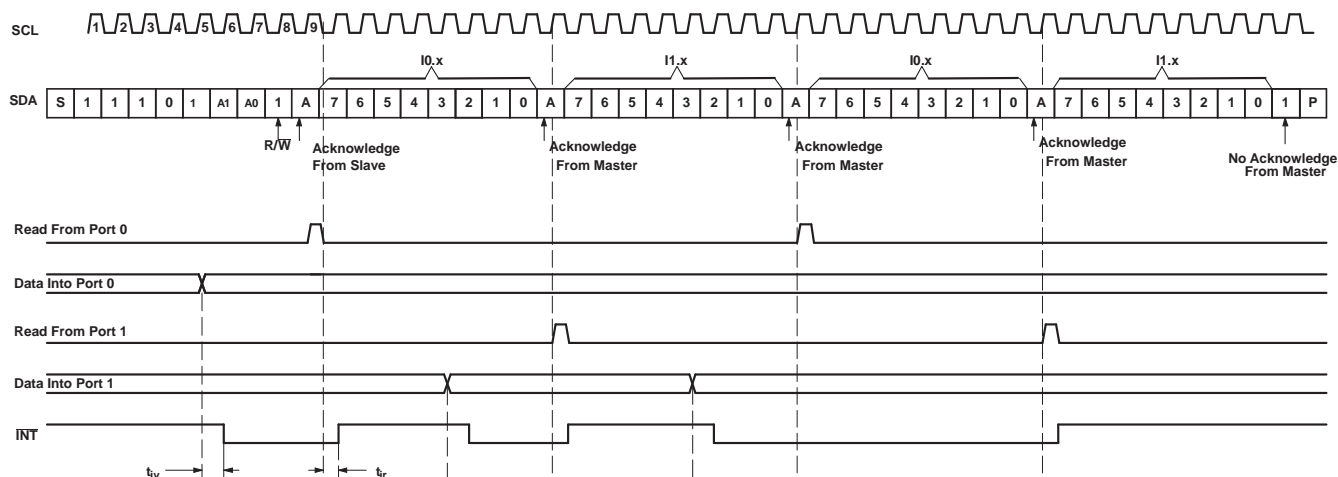

Figure 6. Write to Output Port Registers

Submit Documentation Feedback

Figure 7. Write to Configuration Registers

Reads

The bus master first must send the PCA9539 address with the least-significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9539 (see Figure 8 through Figure 10).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.
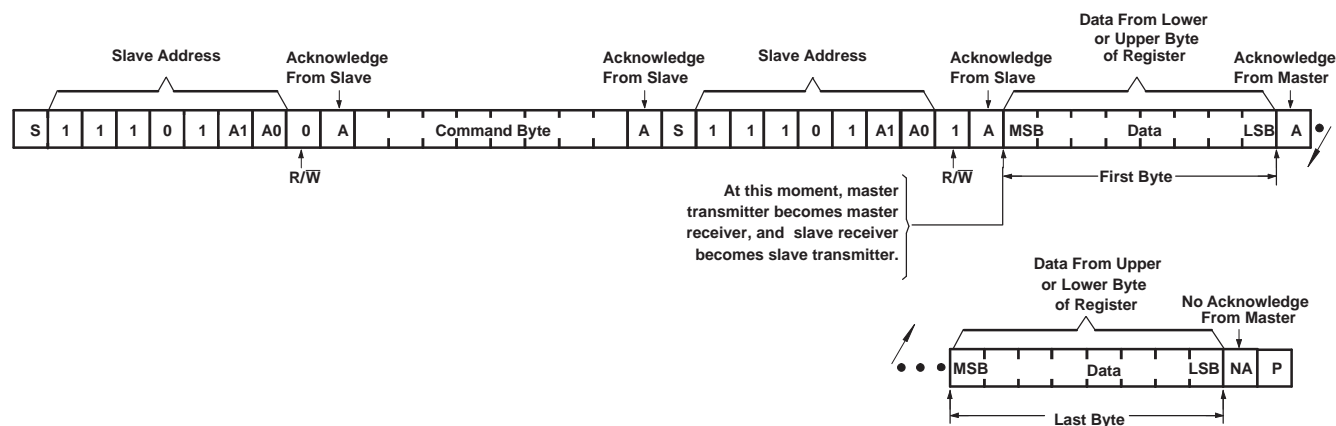

Figure 8. Read From Register

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS INSTRUMENTS
www.ti.com

A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 8 for these details).

Figure 9. Read Input Port Register, Scenario 1
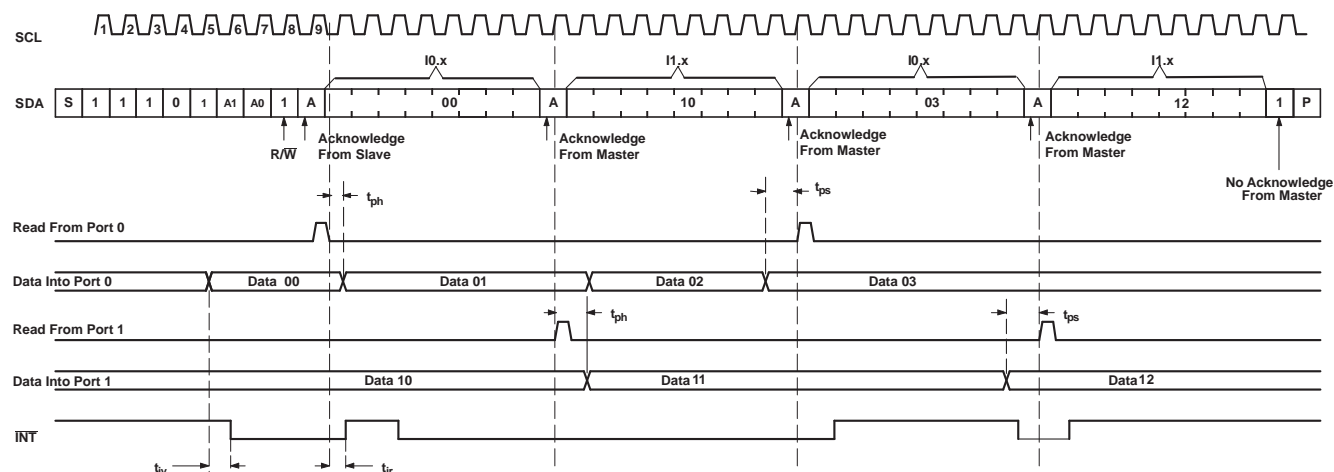
A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 8 for these details).

Figure 10. Read Input Port Register, Scenario 2

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range[2]		−0.5	6	V
V_O	Output voltage range[2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance, junction to free air[3]	DB package		63	°C/W
		DBQ package		61	
		DGV package		86	
		DW package		46	
		PW package		88	
		RGE package		45	
θ_{JP}	Package thermal impedance, junction to pad	RGE package		1.5	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

|			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A0, A1, $\overline{\text{RESET}}$, P07–P00, P17–P10	$0.7 \times V_{CC}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A0, A1, $\overline{\text{RESET}}$, P07–P00, P17–P10	−0.5	$0.3 \times V_{CC}$	
I_{OH}	High-level output current	P07–P00, P17–P10		−10	mA
I_{OL}	Low-level output current	P07–P00, P17–P00		25	mA
T_A	Operating free-air temperature		−40	85	°C

PCA9539
REMOTE 16-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS INSTRUMENTS
www.ti.com

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V		3		mA
	P port[3]	$V_{OL} = 0.5$ V			8	20	
		$V_{OL} = 0.7$ V			10	24	
	$\overline{INT}$	$V_{OL} = 0.4$ V			3		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A0, A1, $\overline{RESET}$					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	$V_I = $ GND	2.3 V to 5.5 V			−1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 400$ kHz	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	$V_I = $ GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 0$ kHz	5.5 V		0.5	1	
			3.6 V		0.4	0.9	
			2.7 V		0.25	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			200	µA
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
	P port				3.7	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 11)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$[1]	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$[1]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b$[1]	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(data)}$	Valid-data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	µs
C_b	I²C bus capacitive load			400	pF

(1) C_b = total capacitance of one bus line in pF

$\overline{\text{RESET}}$ Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 14)

		MIN	MAX	UNIT
t_W	Reset pulse duration	6		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 12 and Figure 13)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS INSTRUMENTS
www.ti.com

TYPICAL CHARACTERISTICS

$T_A = 25°C$ (unless otherwise noted)

SUPPLY CURRENT vs TEMPERATURE
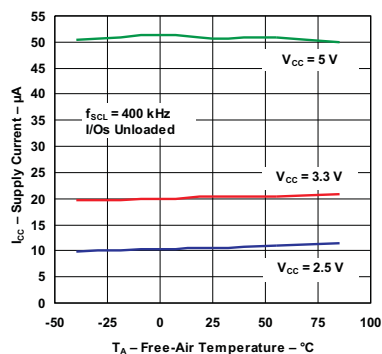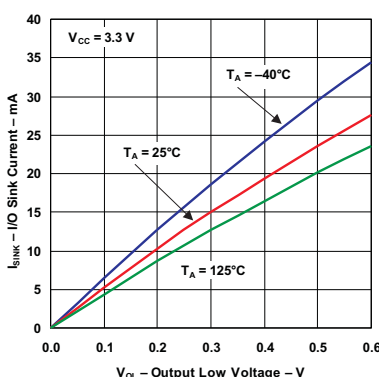

STANDBY SUPPLY CURRENT vs TEMPERATURE
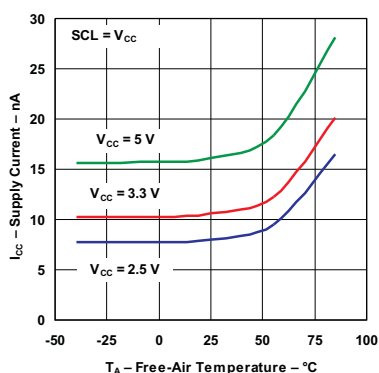
SUPPLY CURRENT vs SUPPLY VOLTAGE
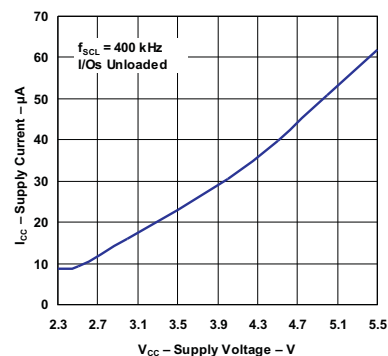
I/O SINK CURRENT vs OUTPUT LOW VOLTAGE
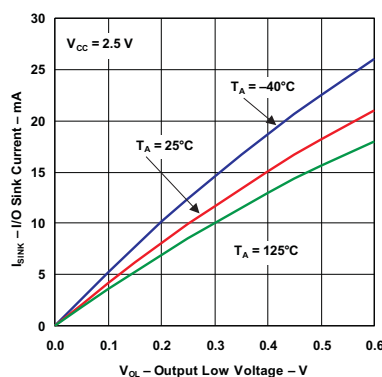
I/O SINK CURRENT vs OUTPUT LOW VOLTAGE

I/O SINK CURRENT vs OUTPUT LOW VOLTAGE
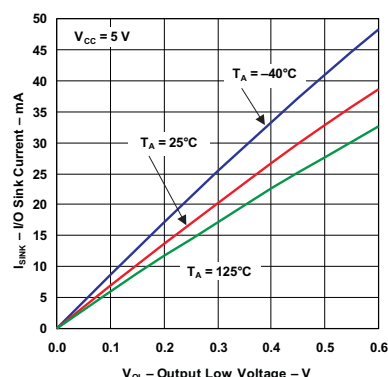
I/O OUTPUT LOW VOLTAGE vs TEMPERATURE
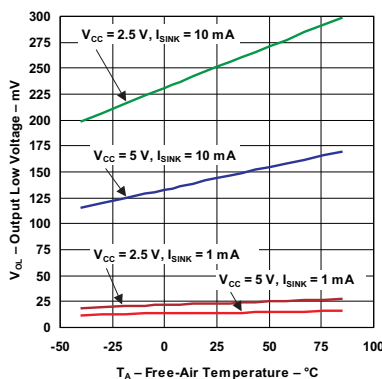
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE
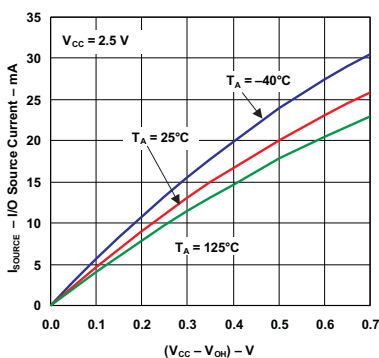
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE
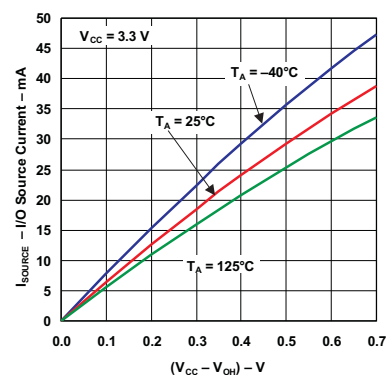
TYPICAL CHARACTERISTICS (continued)

$T_A = 25°C$ (unless otherwise noted)

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE
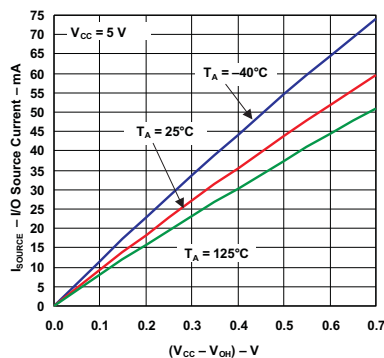
I/O HIGH VOLTAGE
vs
TEMPERATURE
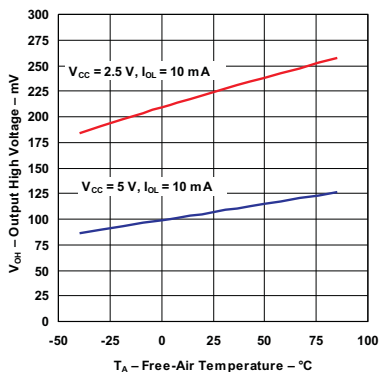
OUTPUT HIGH VOLTAGE
vs
SUPPLY VOLTAGE

PCA9539
REMOTE 16-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS INSTRUMENTS
www.ti.com
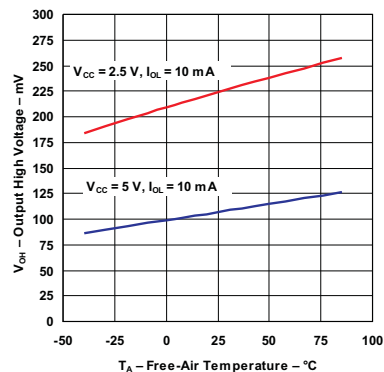
PARAMETER MEASUREMENT INFORMATION
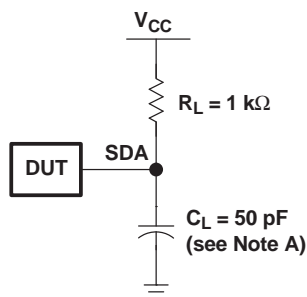
SDA LOAD CONFIGURATION
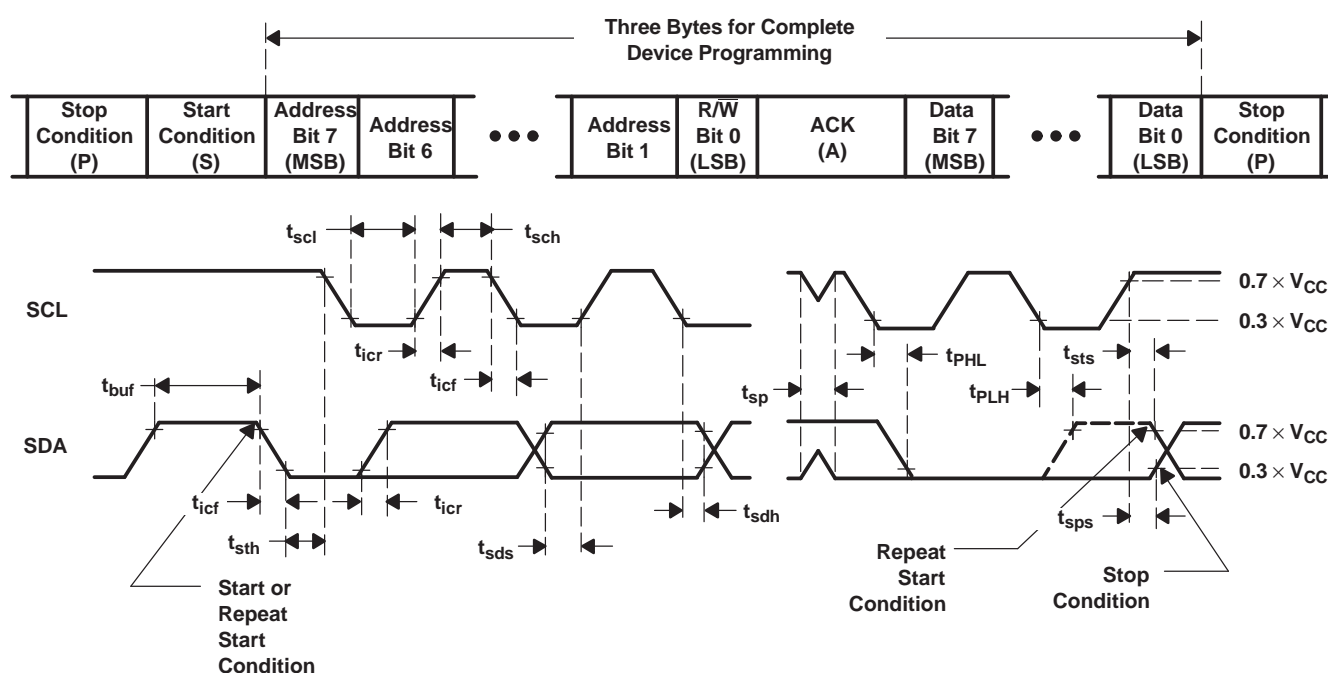
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^{2}C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 11. I^{2}C Interface Load Circuit and Voltage Waveforms
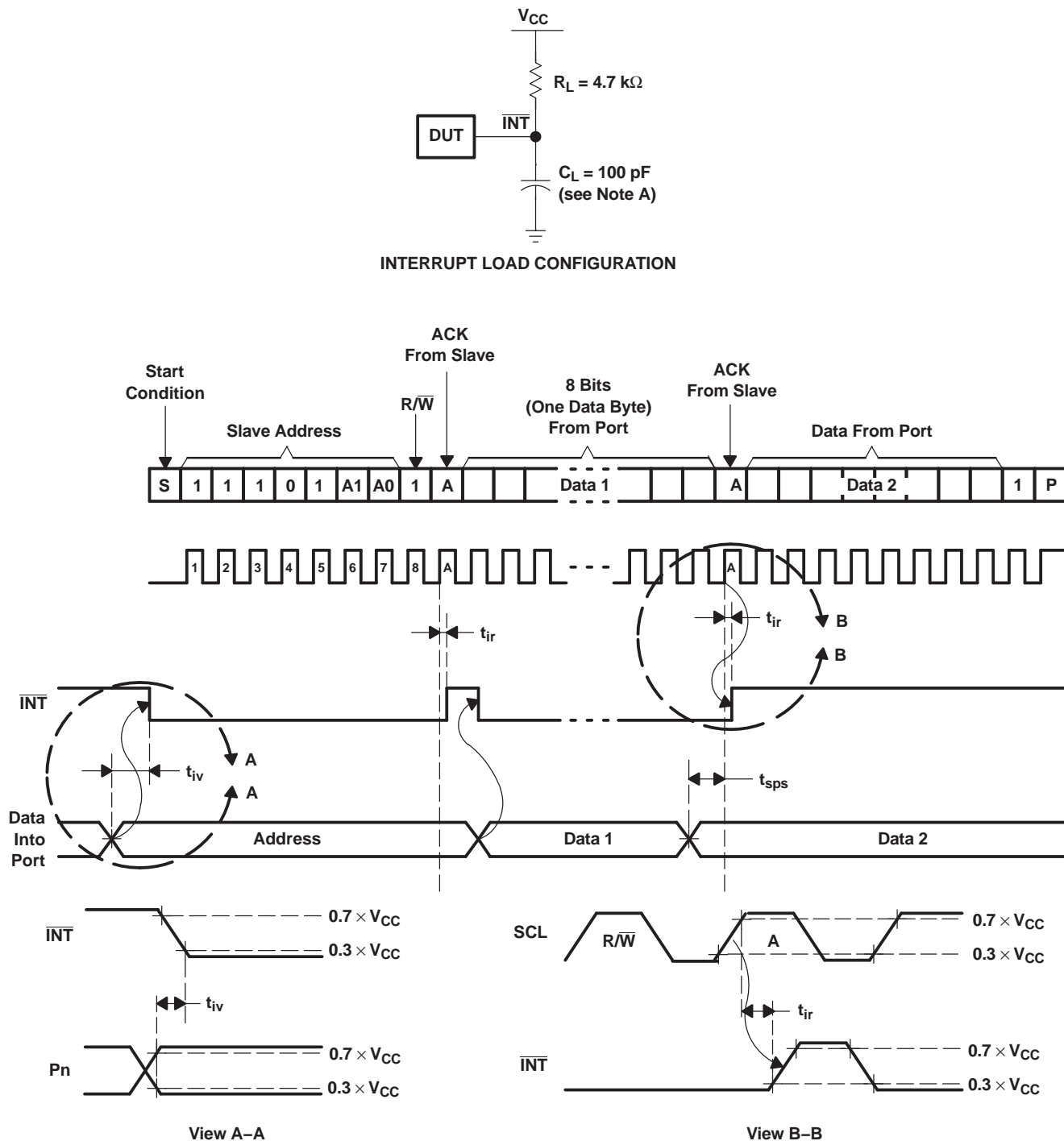
PARAMETER MEASUREMENT INFORMATION (continued)

INTERRUPT LOAD CONFIGURATION

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 12. Interrupt Load Circuit and Voltage Waveforms

PCA9539
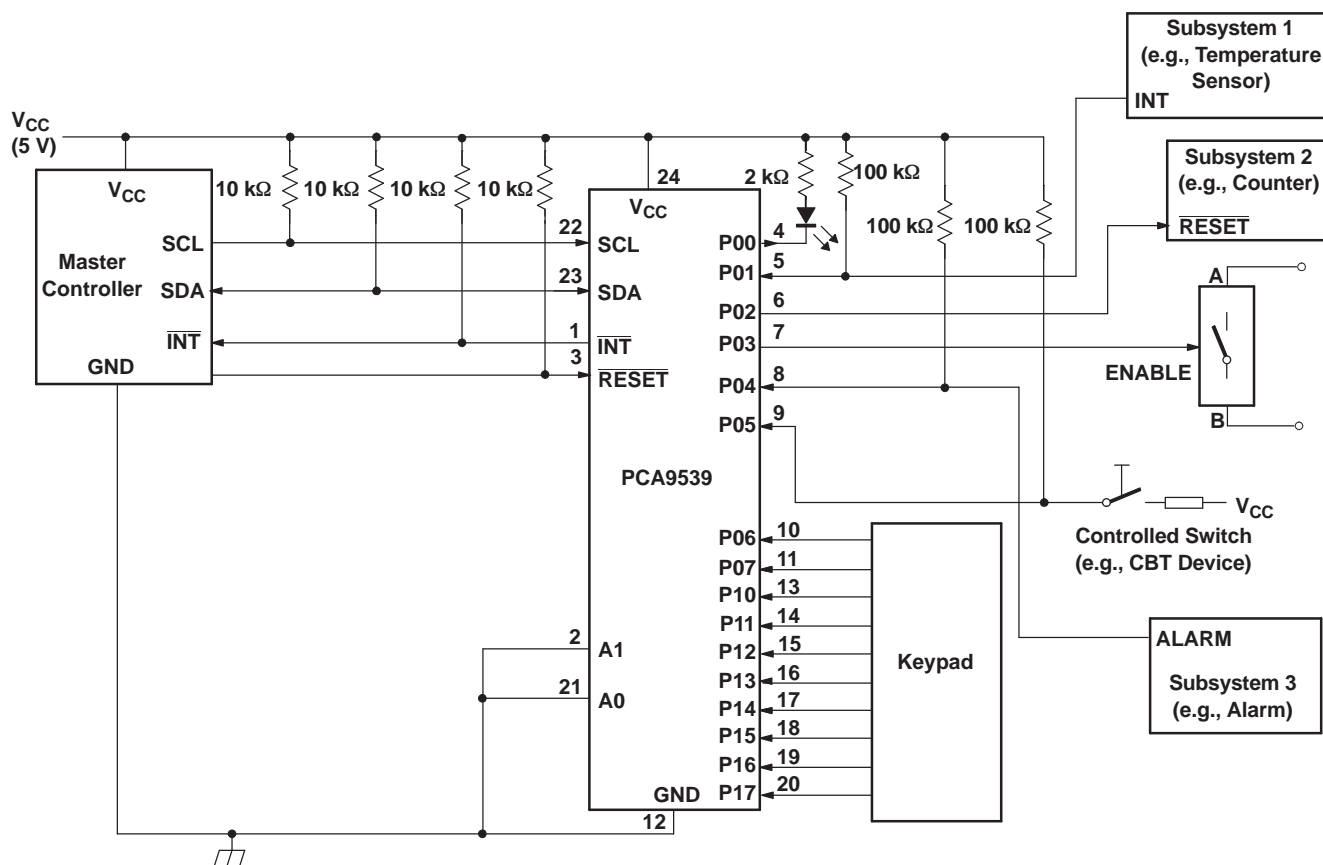**REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER**
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS
INSTRUMENTS
www.ti.com

PARAMETER MEASUREMENT INFORMATION (continued)

P-PORT LOAD CONFIGURATION

WRITE MODE (R/$\overline{W}$ = 0)

READ MODE (R/$\overline{W}$ = 1)
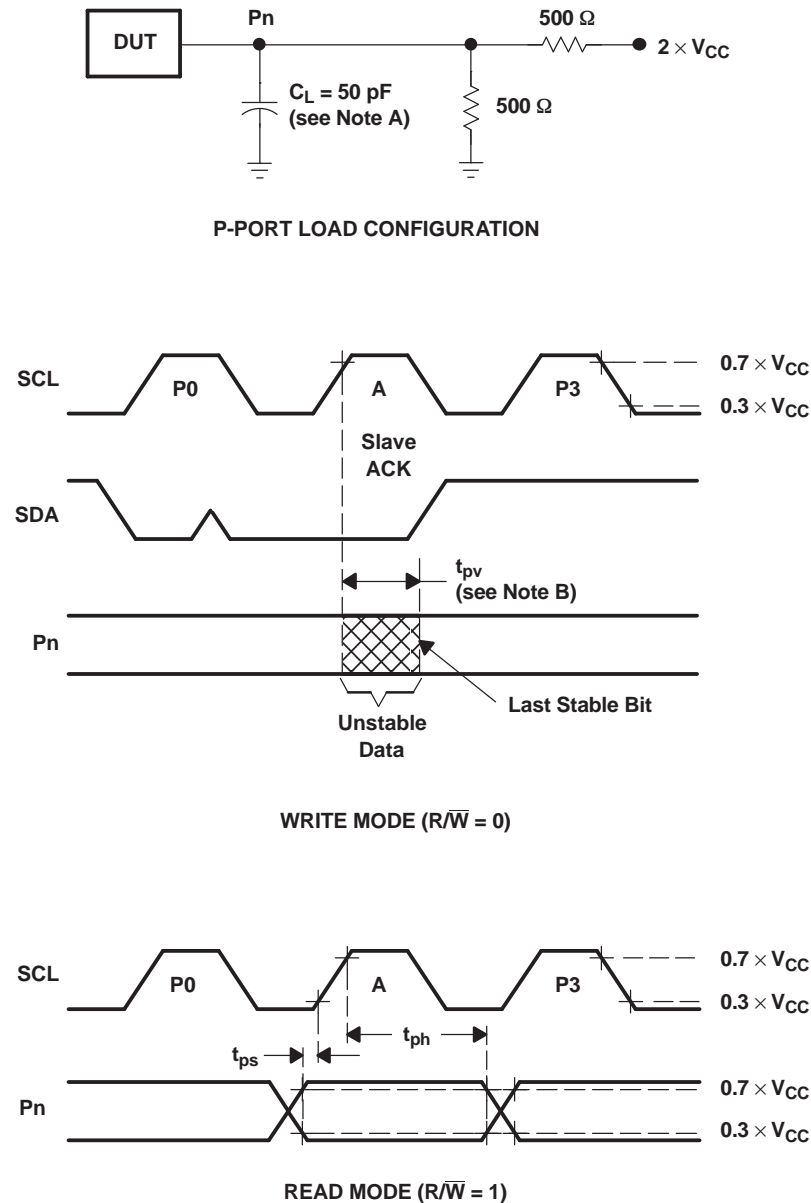
A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.

C.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D.   The outputs are measured one at a time, with one transition per measurement.

E.   All parameters and waveforms are not applicable to all devices.

Figure 13. P-Port Load Circuit and Voltage Waveforms
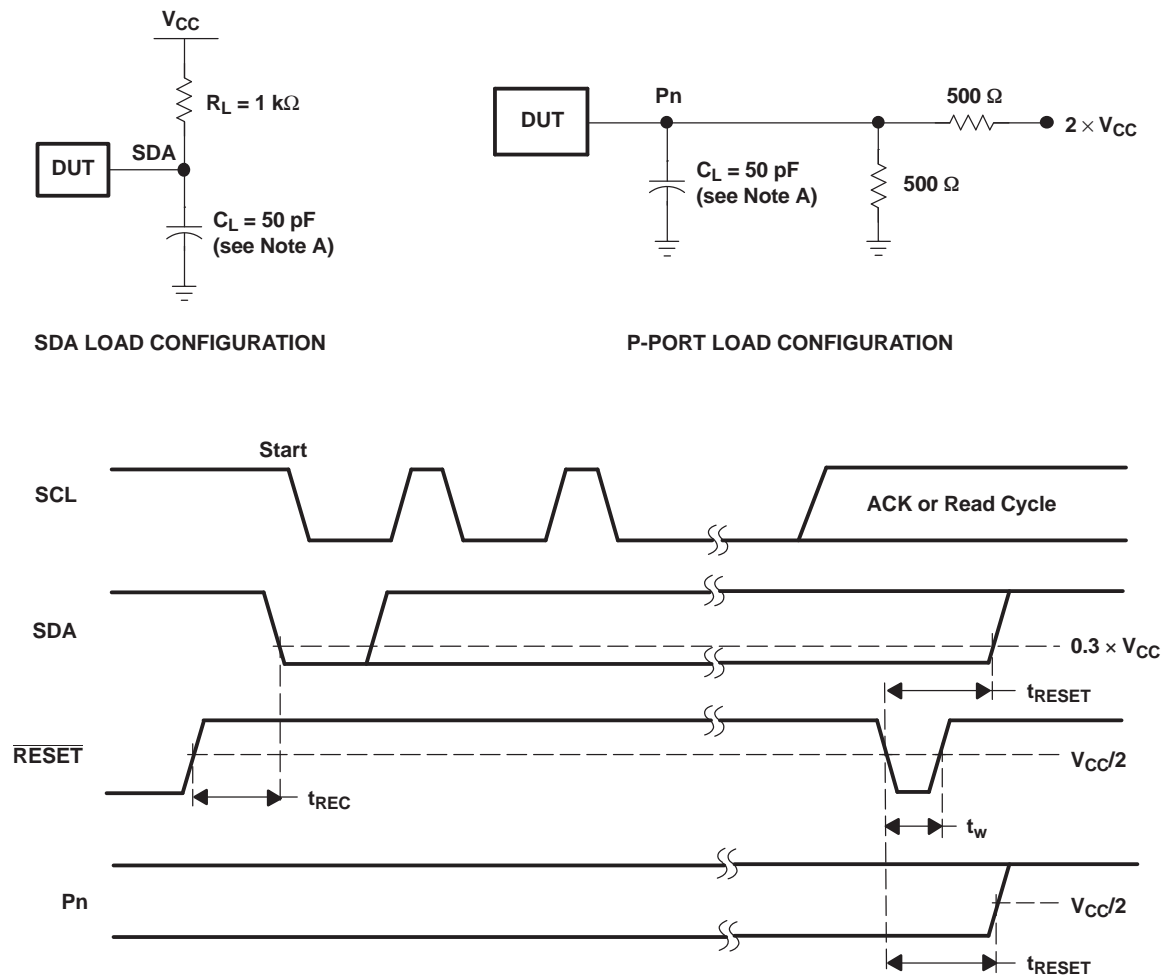
PARAMETER MEASUREMENT INFORMATION (continued)

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 14. Reset Load Circuits and Voltage Waveforms

PCA9539
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT, RESET, AND CONFIGURATION REGISTERS
SCPS130D−AUGUST 2005−REVISED MARCH 2007

TEXAS INSTRUMENTS
www.ti.com

APPLICATION INFORMATION

Figure 15 shows an application in which the PCA9539 can be used.

A. Device address is configured as 1110100 for this example.

B. P00, P02, and P03 are configured as outputs.

C. P01 and P04 to P17 are configured as inputs.

D. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

Figure 15. Typical Application

APPLICATION INFORMATION (continued)

Minimizing I_{CC} When I/O Is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor (see Figure 15). Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

Figure 16 shows a high-value resistor in parallel with the LED. Figure 17 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{CC} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.
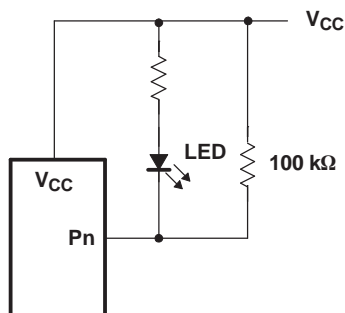
Figure 16. High-Value Resistor in Parallel With LED
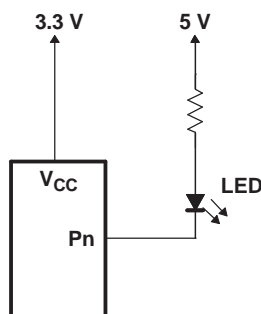
Figure 17. Device Supplied by Lower Voltage

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCA9539DB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DBG4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9539DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9539DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9539RGER	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9539RGERG4	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9539RHLR	PREVIEW	QFN	RHL	24	1000	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check

http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
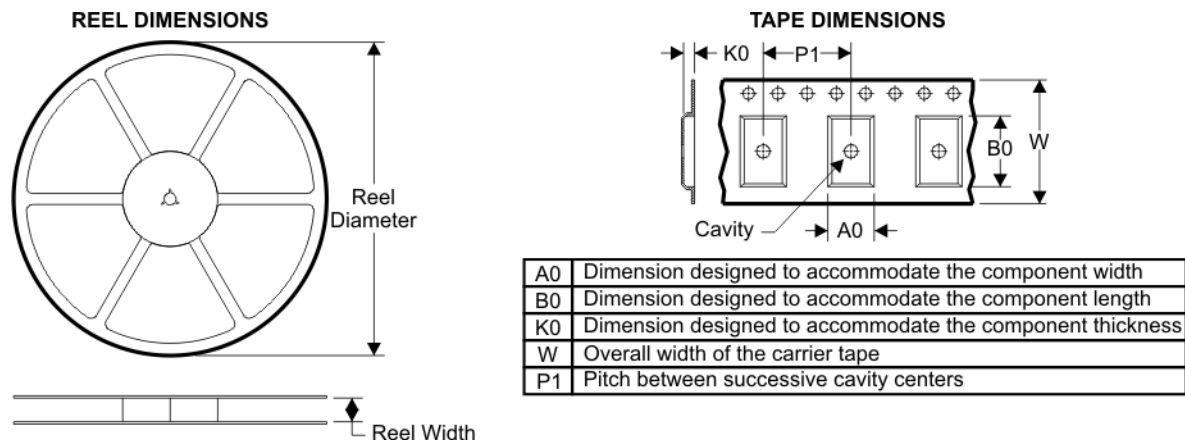
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Pocket Quadrants
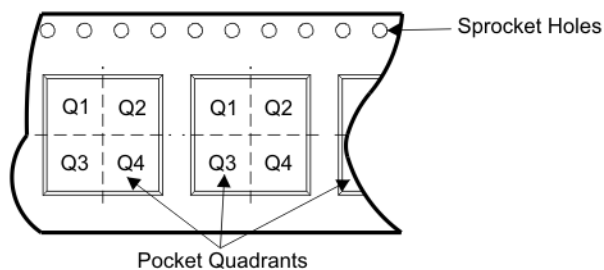
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9539DBQR	DBQ	24	SITE 41	330	16	6.5	9.0	2.1	8	16	Q1
PCA9539DBR	DB	24	SITE 41	330	16	8.2	8.8	2.5	12	16	Q1
PCA9539DGVR	DGV	24	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1
PCA9539DWR	DW	24	SITE 60	330	24	10.75	15.7	2.7	12	24	Q1
PCA9539PWR	PW	24	SITE 41	330	16	6.95	8.3	1.6	8	16	Q1
PCA9539RGER	RGE	24	SITE 41	330	12	4.3	4.3	1.5	8	12	Q2

TEXAS INSTRUMENTS

TAPE AND REEL BOX DIMENSIONS

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
PCA9539DBQR	DBQ	24	SITE 41	346.0	346.0	33.0
PCA9539DBR	DB	24	SITE 41	346.0	346.0	33.0
PCA9539DGVR	DGV	24	SITE 41	346.0	346.0	29.0
PCA9539DWR	DW	24	SITE 60	346.0	346.0	41.0
PCA9539PWR	PW	24	SITE 41	346.0	346.0	33.0
PCA9539RGER	RGE	24	SITE 41	346.0	346.0	29.0

DGV (R-PDSO-G**)　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23 / 0,13 ⊕ 0,07 Ⓜ

24　　　　　13

4,50 / 4,30　　6,60 / 6,20

1　　　　　12

A

0,16 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

⌒ 0,08

DIM　PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
　　　　D. Falls within JEDEC: 24/48 Pins – MO-153
　　　　　　　　　　　　　　　14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

$\frac{0.614\ (15,60)}{0.598\ (15,20)}$

24

13

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1

12

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

◁ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AD.

DBQ (R−PDSO−G24) PLASTIC SMALL−OUTLINE PACKAGE
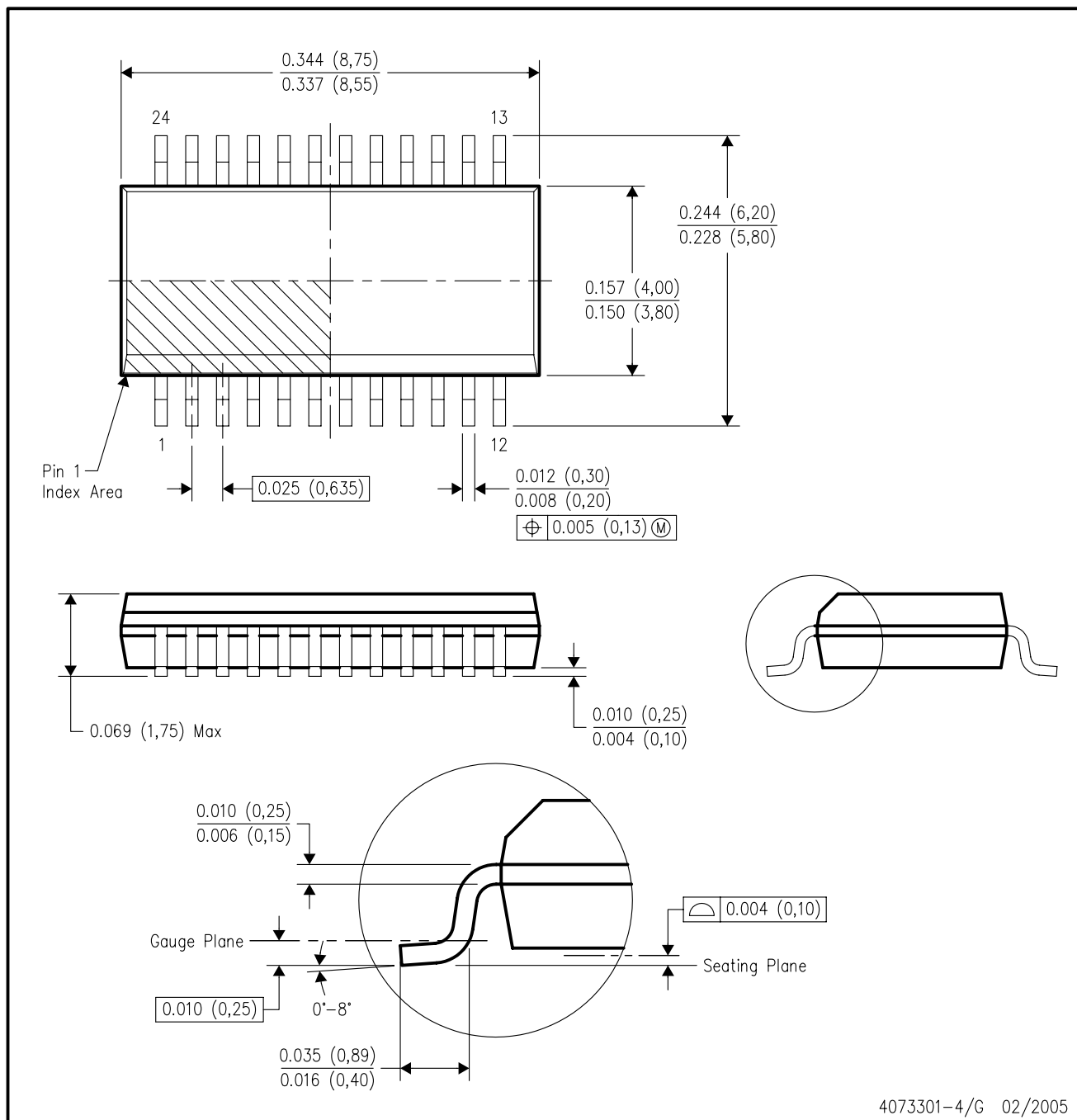
0.344 (8,75)
0.337 (8,55)

24   13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.006 (0,15)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/G 02/2005

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D. Falls within JEDEC MO−137 variation AE.

RHL (R−PQFP−N24)   PLASTIC QUAD FLATPACK
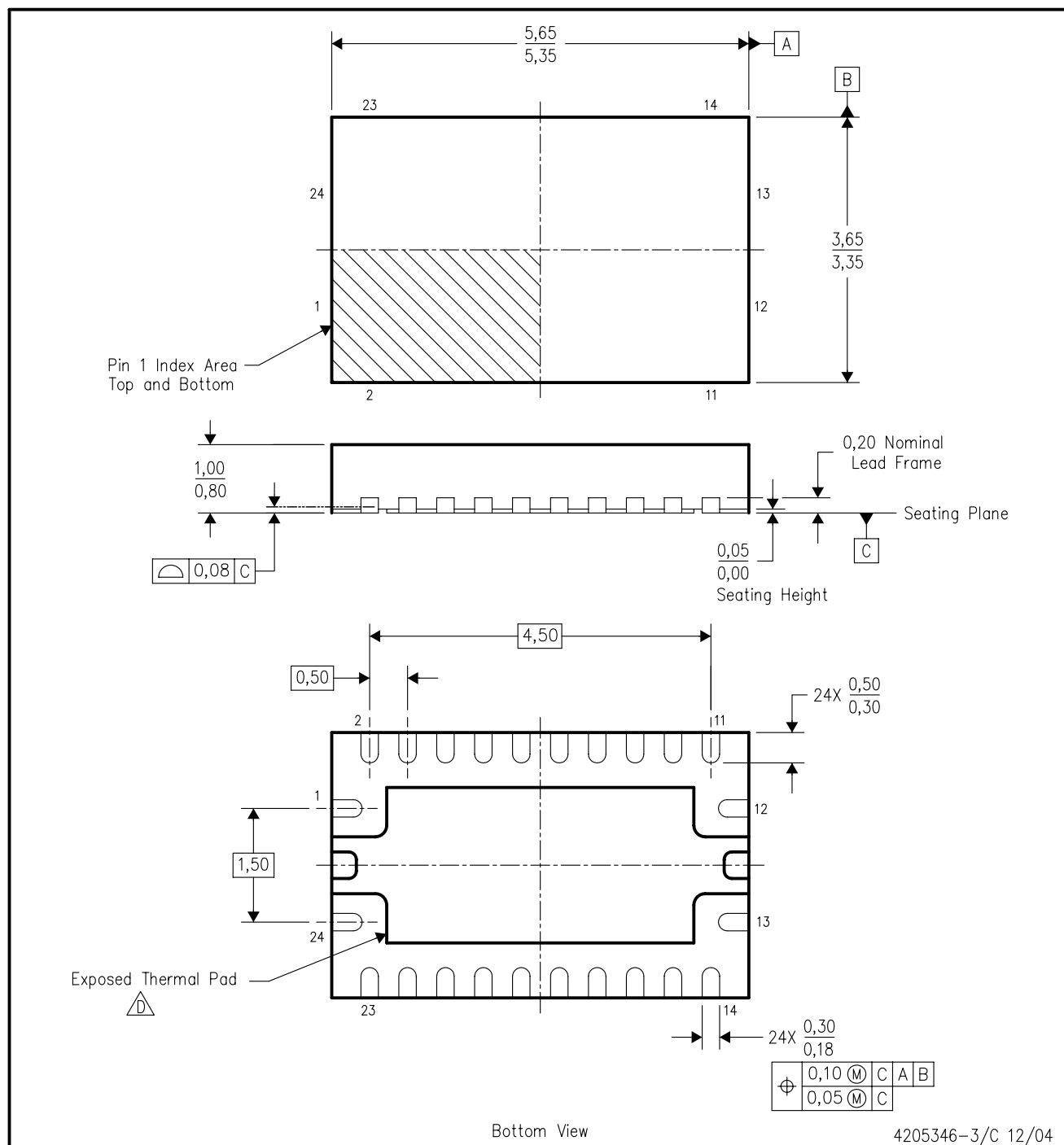
5,65
5,35

A

B

23   14

24   13

3,65
3,35

1

Pin 1 Index Area
Top and Bottom

2   11

1,00
0,80

0,20 Nominal
Lead Frame

Seating Plane

⌒ 0,08 C

0,05
0,00
Seating Height

C

4,50

0,50

24X 0,50
0,30

2   11

1   12

1,50

24   13

Exposed Thermal Pad

⚠ D

23

14

24X 0,30
0,18

⊕ | 0,10 Ⓜ | C | A | B |
  | 0,05 Ⓜ | C |

Bottom View

4205346−3/C 12/04

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. QFN (Quad Flatpack No−Lead) package configuration.
     ⚠ D   The package thermal pad must be soldered to the board for thermal and mechanical performance.
             See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E. JEDEC MO−241 package registration pending.

RGE (S−PQFP−N24)   PIN 1 OPTION   PLASTIC QUAD FLATPACK

$\frac{4,15}{3,85}$

$\frac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

⌓ 0,08

$\frac{0,05}{0,00}$

PIN 1 INDICATOR

$24X \frac{0,50}{0,30}$

0,50

1   6

24   7

19   12

EXPOSED THERMAL PAD

⚠D

18   13

2,50

$24X \frac{0,30}{0,18}$

⊕ Ø 0,10 Ⓜ
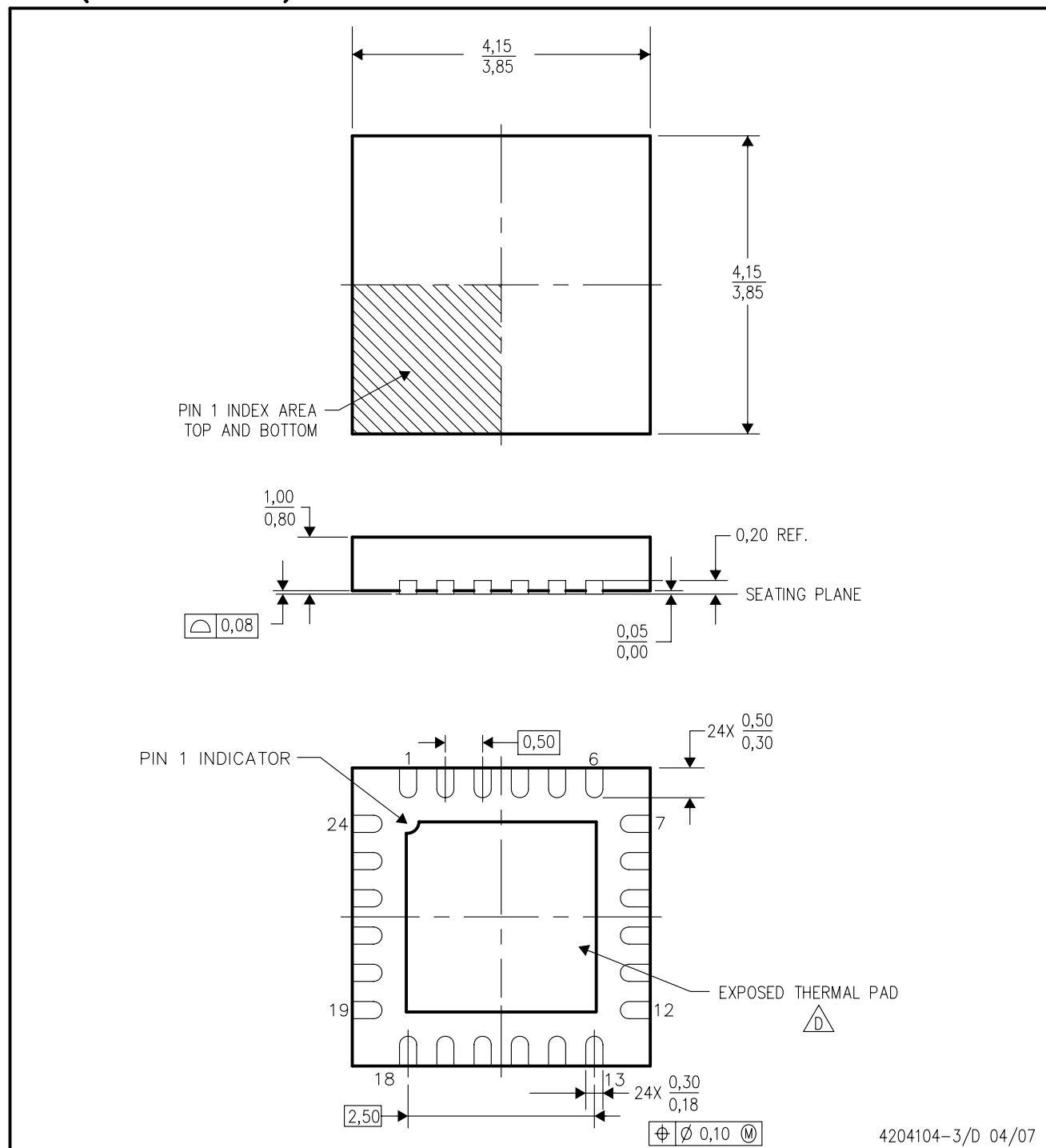
4204104−3/D 04/07

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Quad Flatpack, No−Leads (QFN) package configuration.
        ⚠D   The package thermal pad must be soldered to the board for thermal and mechanical performance.
                See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
          E.   Falls within JEDEC MO−220.

TEXAS
INSTRUMENTS
www.ti.com

DB (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

4,50
4,30

6,60
6,20

1   7

A

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

△ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE