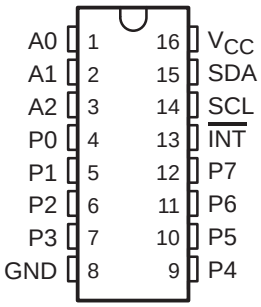
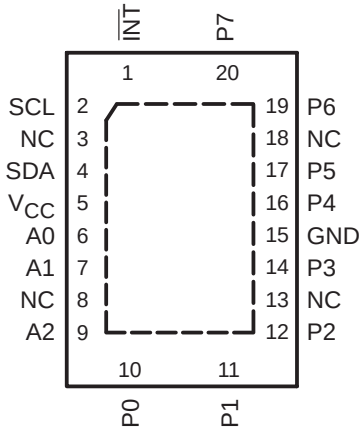
- **Low Standby-Current Consumption of 10 μA Maximum**
- **I²C to Parallel-Port Expander**
- **Open-Drain Interrupt Output**
- **Compatible With Most Microcontrollers**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DW OR N PACKAGE
(TOP VIEW)

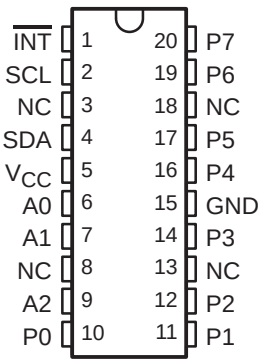


RGY PACKAGE
(TOP VIEW)



NC − No internal connection

DGV OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I²C) is designed for 2.5-V to 6-V V_{CC} operation.

The PCF8574A provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0−P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V_{CC} is active. An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	PCF8574ARGYR	PF574A
	PDIP − N	Tube	PCF8574AN	PCF8574AN
	SOIC − DW	Tube	PCF8574ADW	PCF8574A
		Tape and reel	PCF8574ADWR	
	TSSOP − PW	Tape and reel	PCF8574APWR	PF574A
	TVSOP − DGV	Tape and reel	PCF8574ADGVR	PF574A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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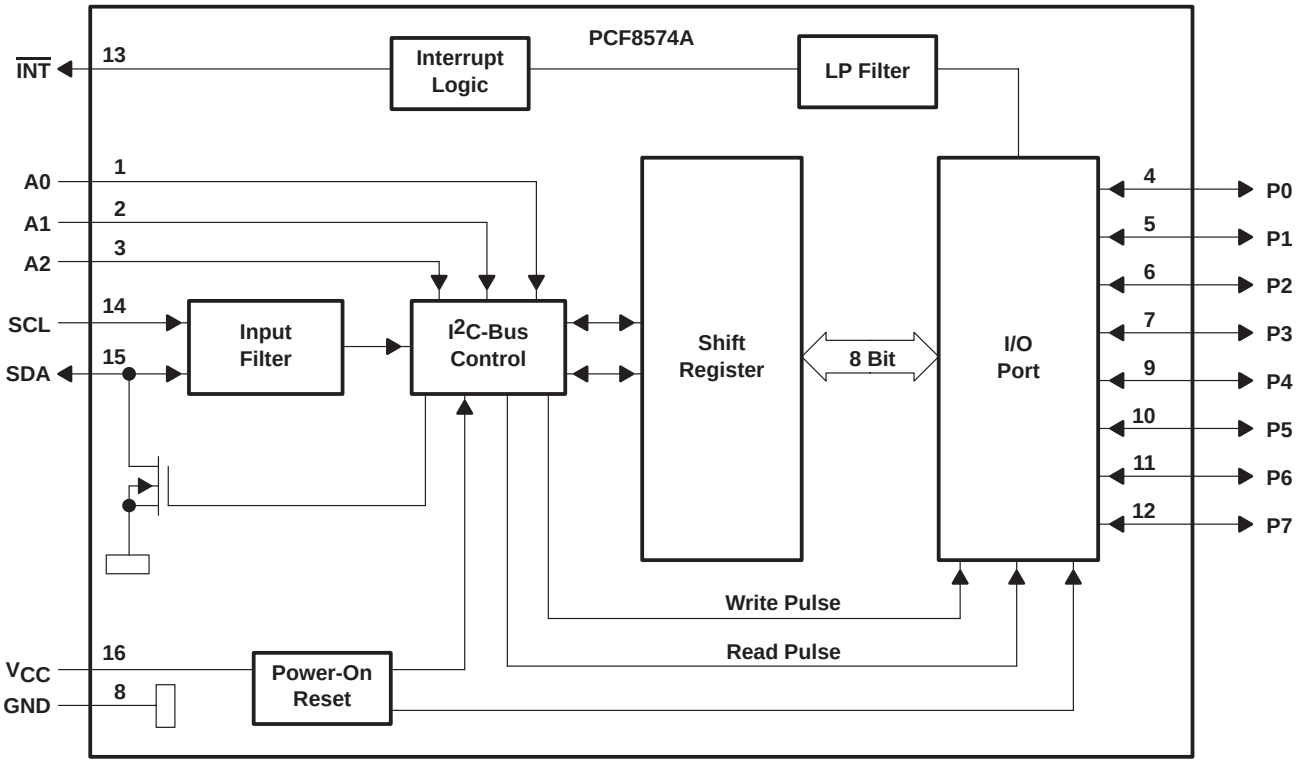
description/ordering information (continued)

The PCF8574A provides an open-drain output ($\overline{INT}$), which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

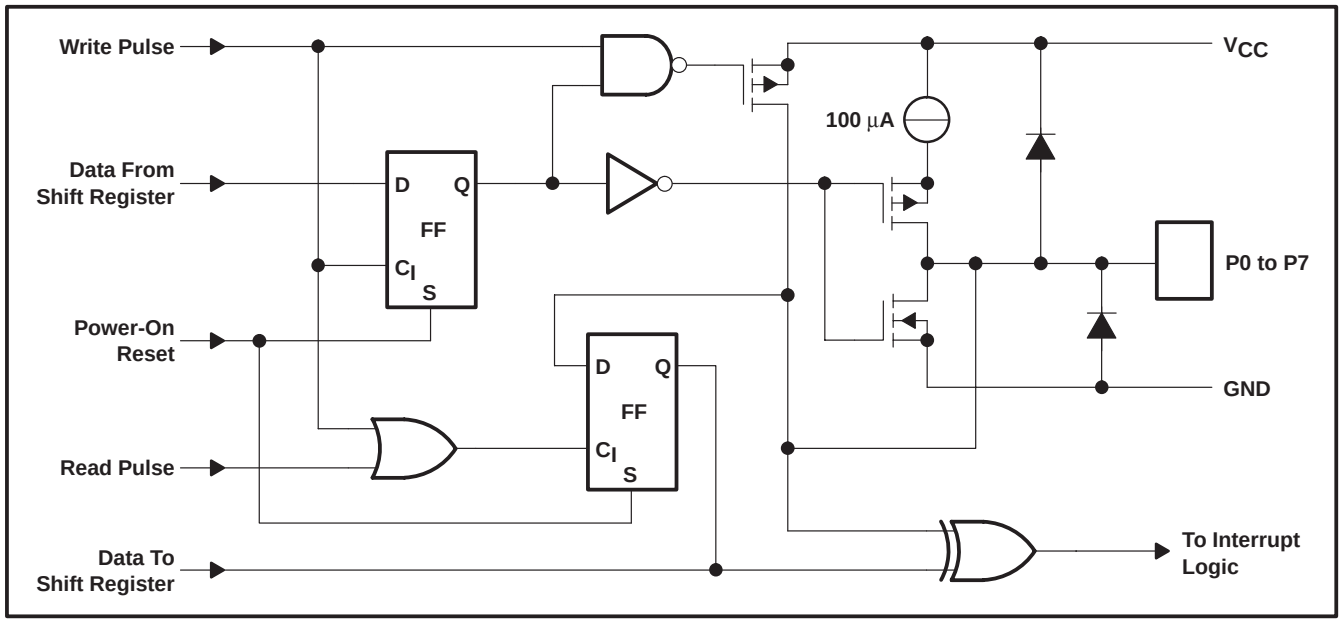
By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the PCF8574A can remain a simple slave device.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

simplified schematic diagram of each P-port input/output



I²C interface

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the serial data (SDA) input/output while the serial clock (SCL) input is high. After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse. The address inputs (A0−A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/$\overline{W}$ bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time t_{pv} after the low-to-high transition of SCL, during the clock cycle for the acknowledge.

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

INTERFACE DEFINITION TABLE

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	H	H	A2	A1	AO	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

ADDRESS REFERENCE TABLE

INPUTS			I²C-BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −20 mA
Input/Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±400 µA
Continuous output low current, I_{OL} (V_O = 0 to V_{CC}) . . . . . 50 mA
Continuous output high current, I_{OH} (V_O = 0 to V_{CC}) . . . . . −4 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DGV package . . . . . 92°C/W
(see Note 2): DW package . . . . . 57°C/W
(see Note 2): N package . . . . . 67°C/W
(see Note 2): PW package . . . . . 83°C/W
(see Note 3): RGY package . . . . . 37°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	6	V
V_{IH}	High-level input voltage	0.7 × V_{CC}	V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	−0.5	0.3 × V_{CC}	V
I_{OH}	High-level output current		−1	mA
I_{OL}	Low-level output current		25	mA
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = −18 mA	2.5 V to 6 V	−1.2			V
V_{POR}	Power-on reset voltage‡	$V_I = V_{CC}$ or GND, I_O = 0	6 V		1.3	2.4	V
I_{OH}	P port	V_O = GND	2.5 V to 6 V	30		300	µA
I_{OHT}	P-port transient pullup current	High during acknowledge V_{OH} = GND	2.5 V		−1		mA
I_{OL}	SDA	V_O = 0.4 V	2.5 V to 6 V	3			mA
	P port	V_O = 1 V	5 V	10	25		
	$\overline{INT}$	V_O = 0.4 V	2.5 V to 6 V	1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.5 V to 6 V			±5	µA
	$\overline{INT}$					±5	
	A0, A1, A2					±5	
I_{IHL}	P port	$V_I \geq V_{CC}$ or $V_I \leq$ GND	2.5 V to 6 V			±400	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, f_{SCL} = 100 kHz	6 V		40	100	µA
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0			2.5	10	
C_i	SCL	$V_I = V_{CC}$ or GND	2.5 V to 6 V		1.5	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The power-on reset circuit resets the I²C-bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to V_{CC}).

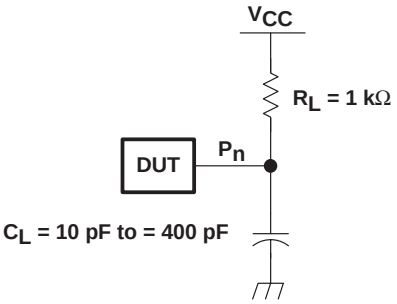
I²C interface timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency			100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			100	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0	900	ns
t_{icr}	I²C input rise time			1	µs
t_{icf}	I²C input fall time			0.3	µs
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)			300	ns
t_{buf}	I²C-bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop-condition setup		4		µs
t_{vd}	Valid-data time	SCL low to SDA output valid		3.4	µs
C_b	I²C-bus capacitive load			400	pF

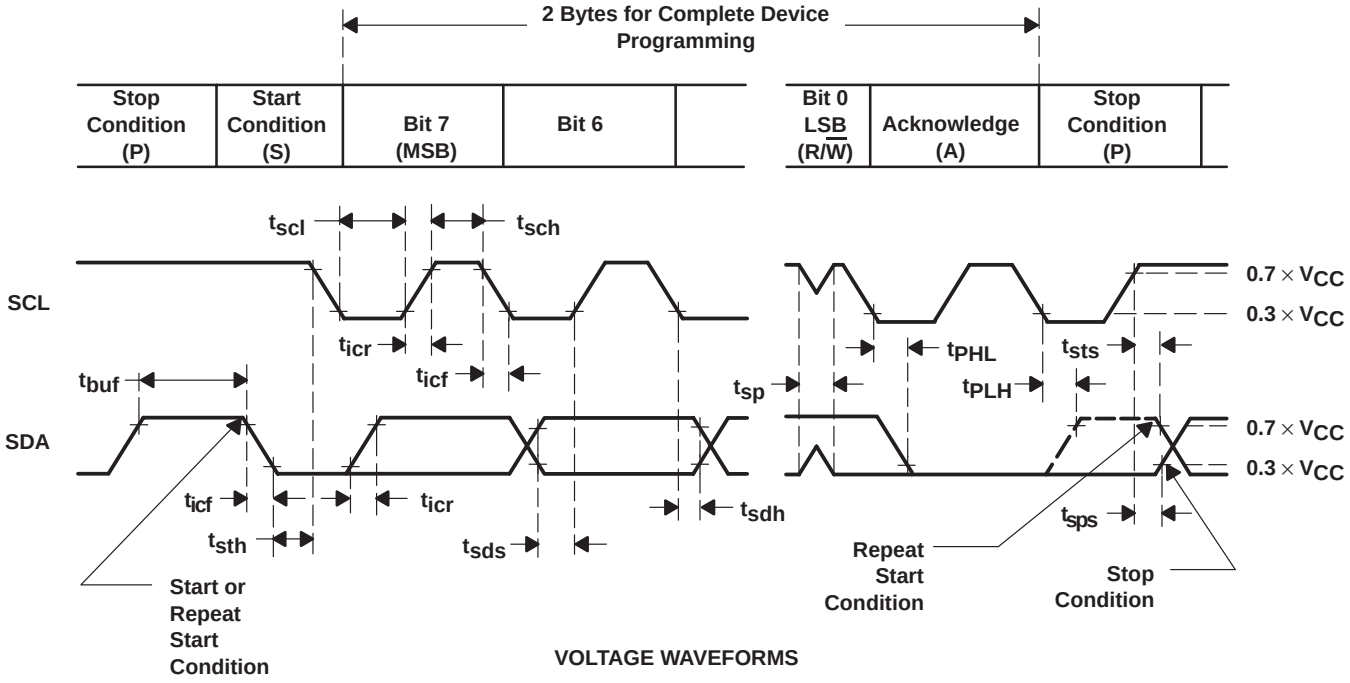
switching characteristics over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pv}	Output data valid	SCL	P port		4	µs
t_{su}	Input data setup time	P port	SCL	0		µs
t_h	Input data hold time	P port	SCL	4		µs
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2	P port data

Figure 1. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

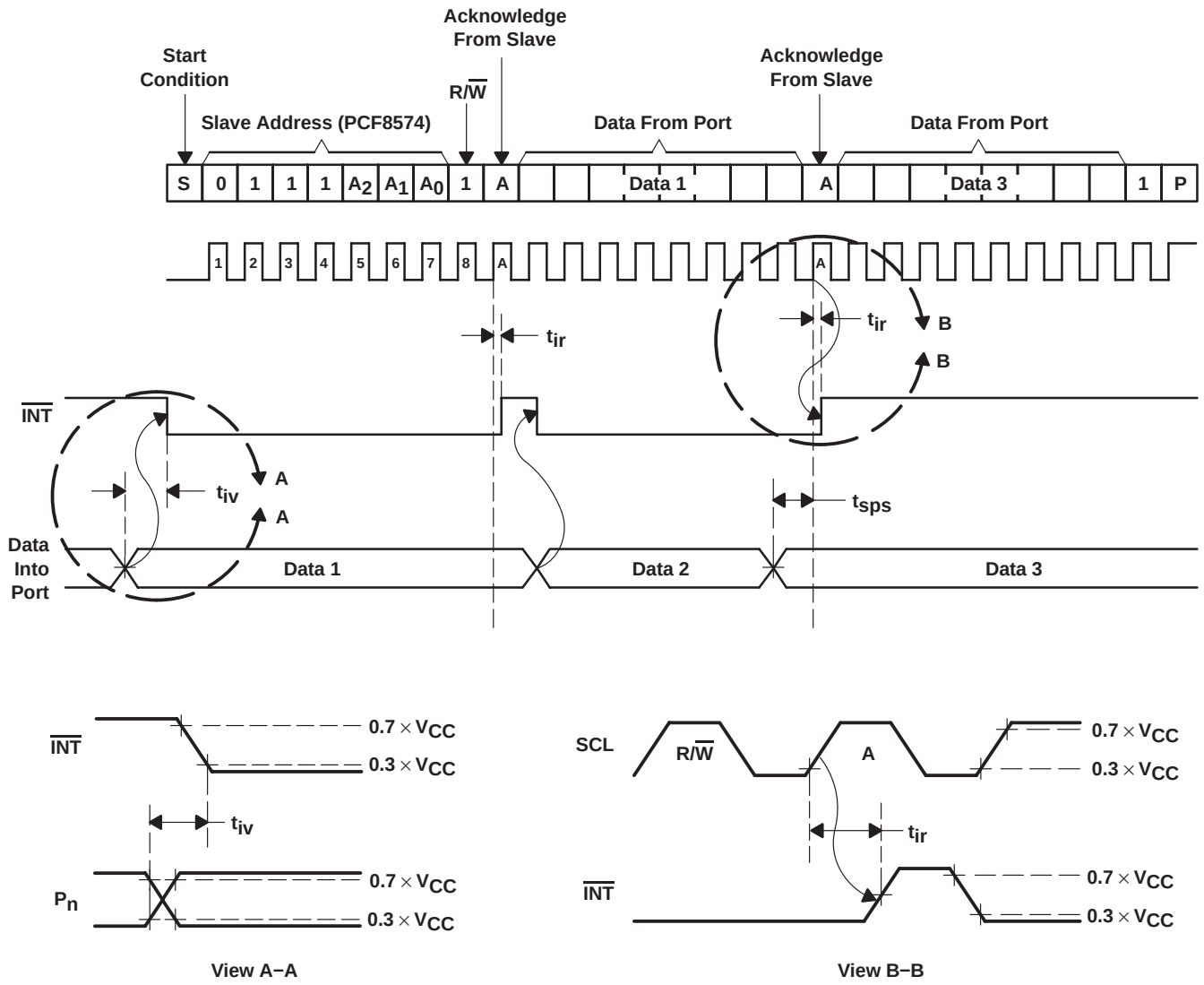


Figure 2. Interrupt-Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

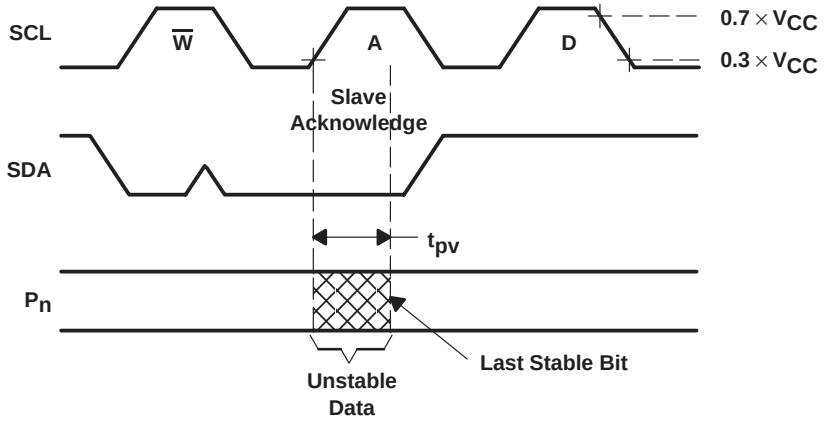


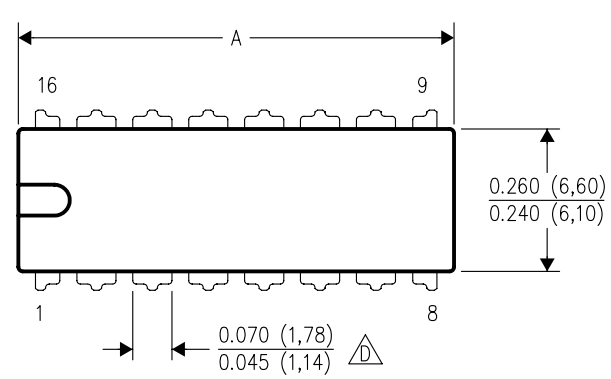
Figure 3. Write-Mode Timing

Figure 4. Load Circuits

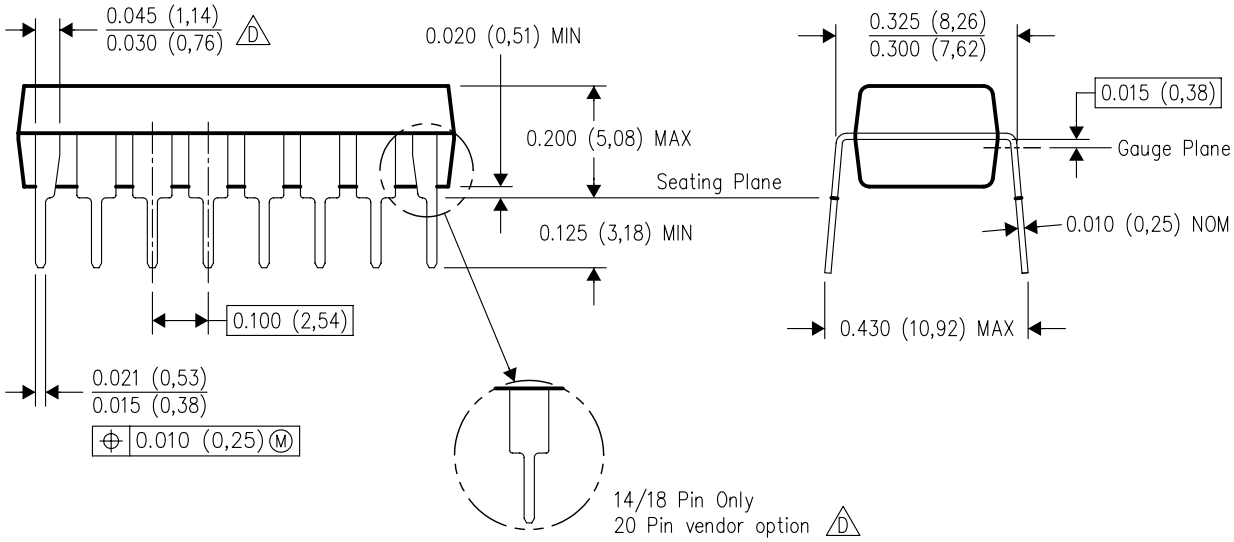
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

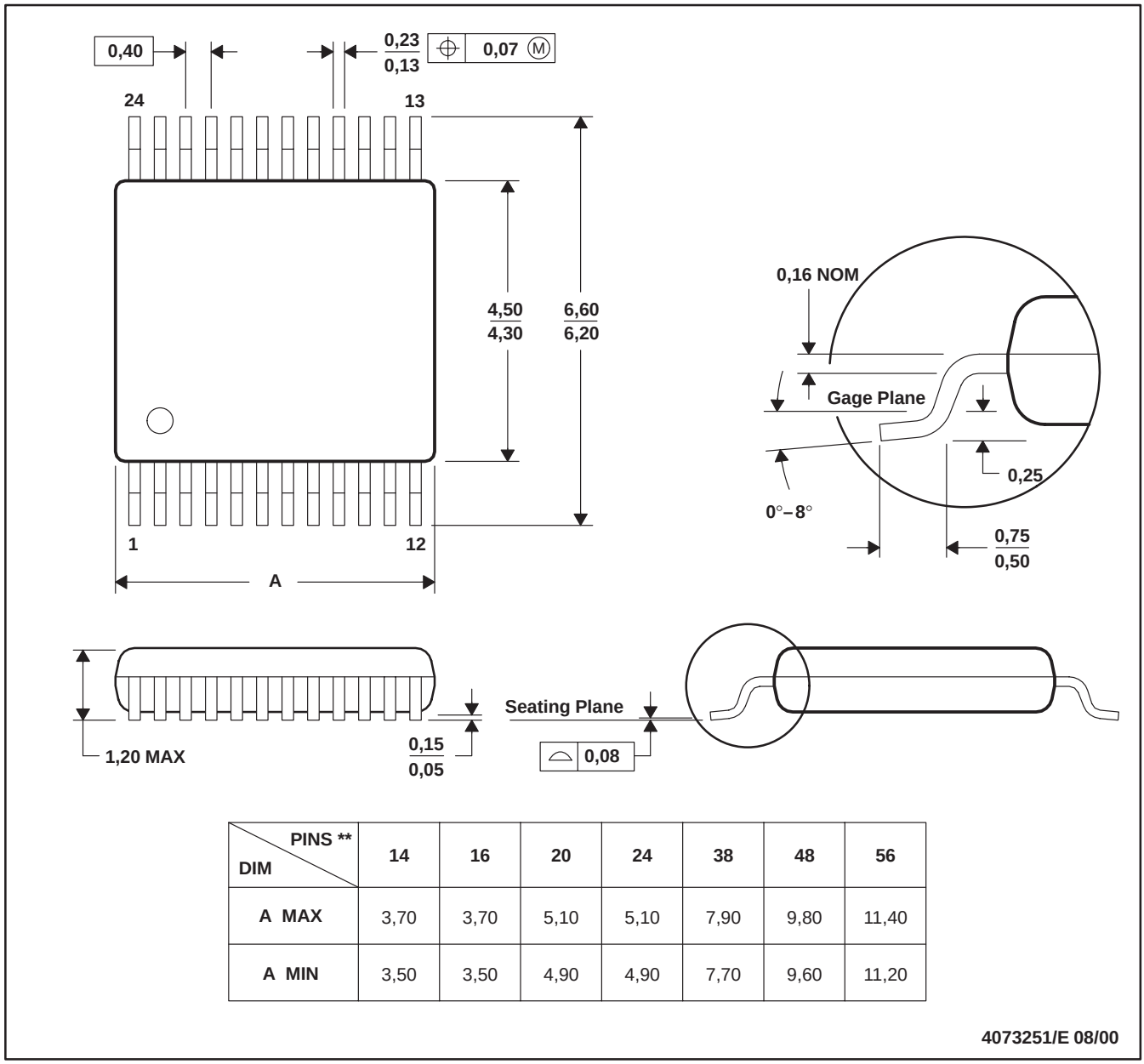


4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

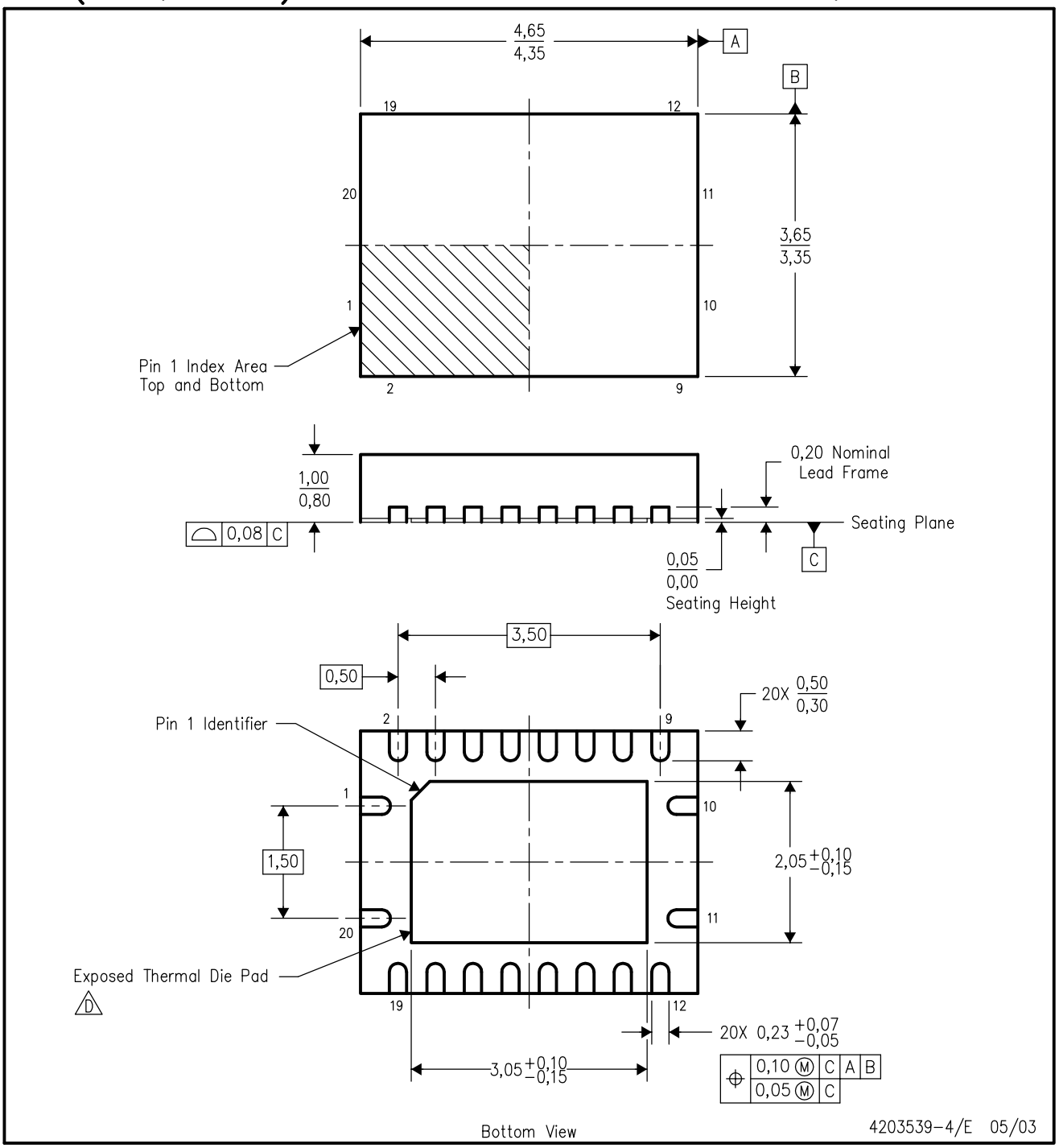


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

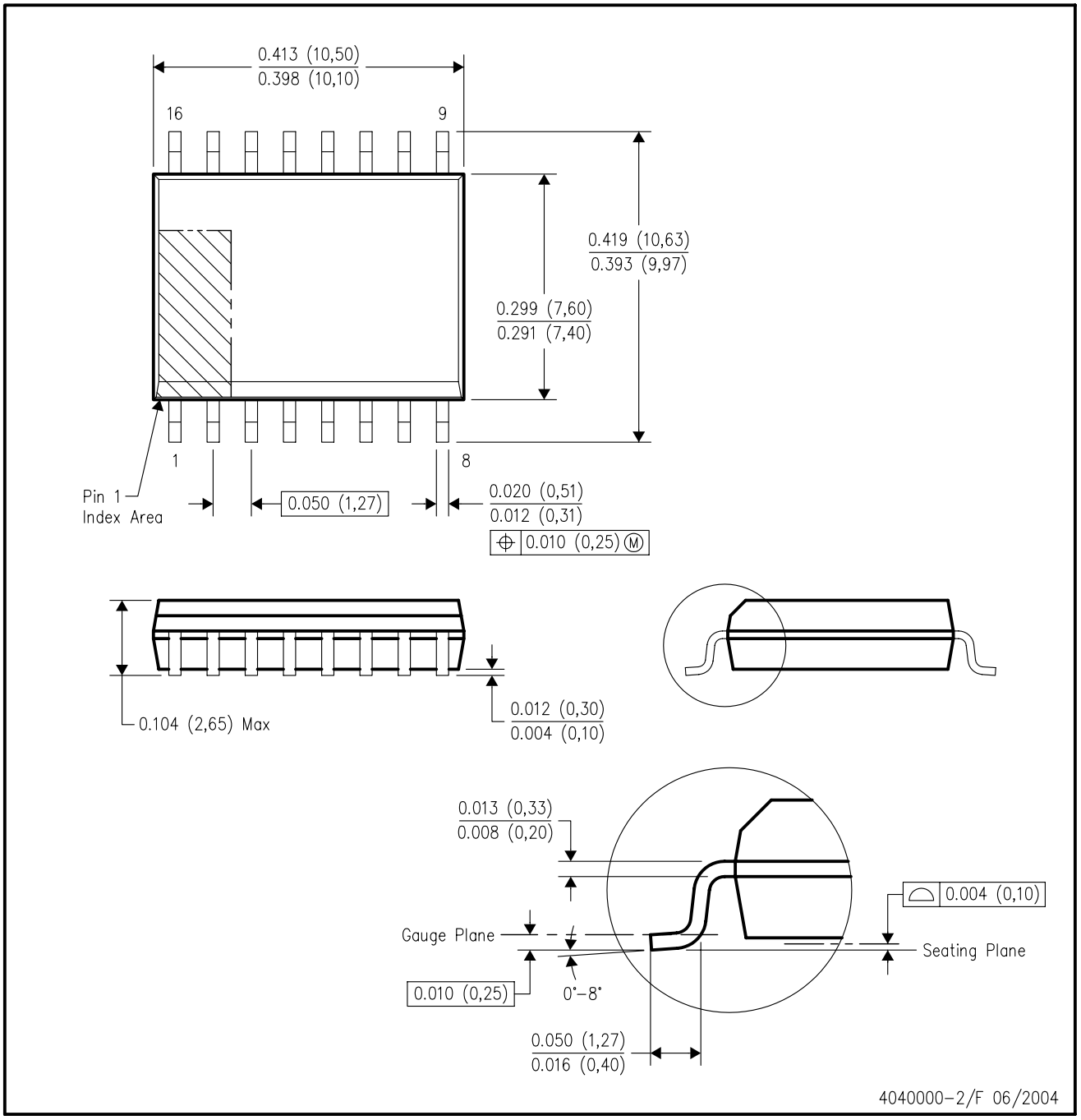
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Package complies to JEDEC MO–241 variation BC.

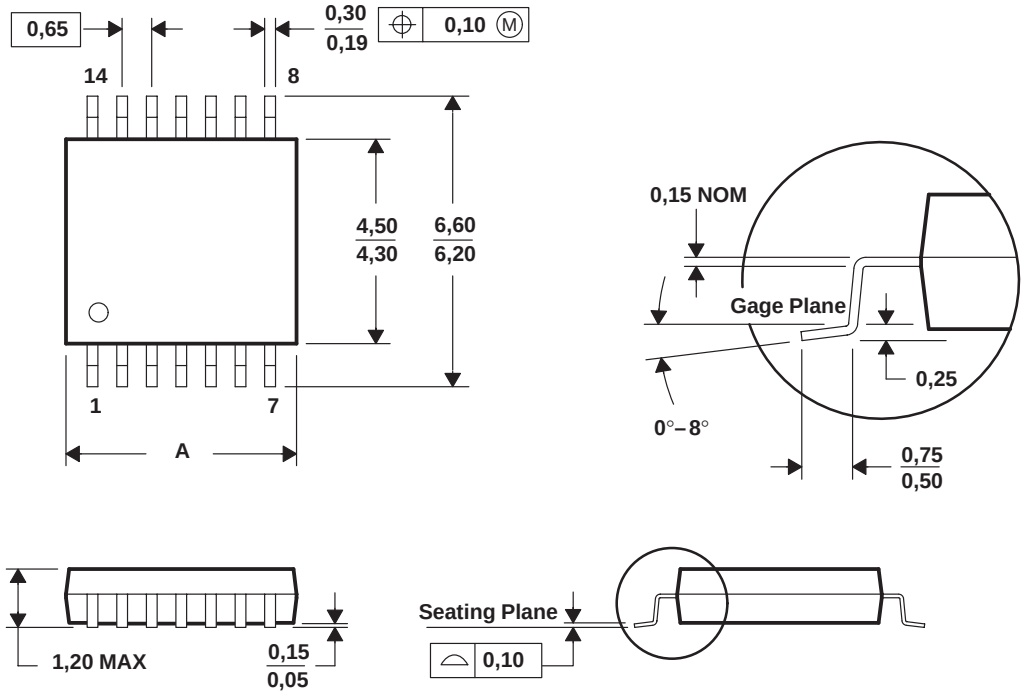
DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265