3.3-V CAN TRANSCEIVERS

FEATURES

- **Bus-Pin Fault Protection Exceeds ±36 V**
- **Bus-Pin ESD Protection Exceeds 16-kV HBM**
- **GIFT/ICT Compliant (SN65HVD234)**
- **Compatible With ISO 11898**
- **Signaling Rates[(1)] up to 1 Mbps**
- **Extended –7-V to 12-V Common-Mode Range**
- **High-Input Impedance Allows for 120 Nodes**
- **LVTTL I/Os Are 5-V Tolerant**
- **Adjustable Driver Transition Times for Improved Signal Quality**
- **Unpowered Node Does Not Disturb the Bus**
- **Low-Current Standby Mode . . . 200-μA Typical**
- **Low-Current Sleep Mode . . . 50-nA Typical (SN65HVD234)**
- **Thermal Shutdown Protection**
- **Power-Up / Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance With Low V_{CC}**
  - **Monolithic Output During Power Cycling**
- **Loopback for Diagnostic Functions Available (SN65HVD233)**
- **Loopback for Autobaud Function Available (SN65HVD235)**
- **DeviceNet Vendor ID #806**

APPLICATIONS

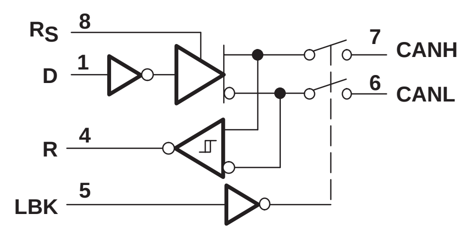
- **CAN Data Bus**
- **Industrial Automation**
  - **DeviceNet™ Data Buses**
  - **Smart Distributed Systems (SDS™)**
- **SAE J1939 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**

DESCRIPTION

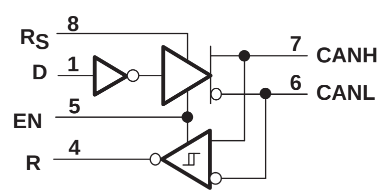
The SN65HVD233, SN65HVD234, and SN65HVD235 are used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, each provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the devices feature cross-wire, overvoltage and loss of ground protection to ±36 V, with overtemperature protection and common-mode transient protection of ±100 V. These devices operate over a –7-V to 12-V common-mode range with a maximum of 60 nodes on a bus.

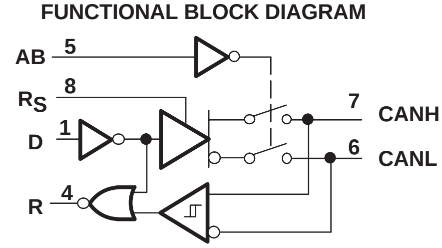
**SN65HVD233
FUNCTIONAL BLOCK DIAGRAM**



**SN65HVD234
FUNCTIONAL BLOCK DIAGRAM**



**SN65HVD235
FUNCTIONAL BLOCK DIAGRAM**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

(1)The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).
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Other trademarks are the property of their respective owners.

DESCRIPTION (Continued)

If the common-mode range is restricted to the ISO-11898 Standard range of –2 V to 7 V, up to 120 nodes may be connected on a bus. These transceivers interface the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

The R_S, pin 8 of the SN65HVD233, SN65HVD234, and SN65HVD235 provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting pin 8 directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8, since the slope is proportional to the pin’s output current. Slope control is implemented with a resistor value of 10 kΩ to achieve a slew rate of ≈15 V/us and a value of 100 kΩ to achieve ≈ 2.0 V/µs slew rate. For more information about slope control, refer to the application information section.

The SN65HVD233, SN65HVD234, and SN65HVD235 enter a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to pin 8. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback LBK pin 5 of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

The SN65HVD234 enters an ultralow-current sleep mode in which both the driver and receiver circuits are deactivated if a low logic level is applied to EN pin 5. The device remains in this sleep mode until the circuit is reactivated by applying a high logic level to pin 5.

The AB pin 5 of the SN65HVD235 implements a bus listen-only loopback feature which allows the local node controller to synchronize its baud rate with that of the CAN bus. In autobaud mode, the driver’s bus output is placed in a high-impedance state while the receiver’s bus input remains active. For more information on the autobaud mode, refer to the application information section.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PART NUMBER	LOW POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233D	200-µA standby mode	Adjustable	Yes	No
SN65HVD234D	200-µA standby mode or 50-nA sleep mode	Adjustable	No	No
SN65HVD235D	200-µA standby mode	Adjustable	No	Yes

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ORDERING INFORMATION

PACKAGE (D)	MARKED AS
SN65HVD233D	VP233
SN65HVD233DR(1)	
SN65HVD234D	VP234
SN65HVD234DR(1)	
SN65HVD235D	VP235
SN65HVD235DR(1)	

(1) R suffix indicated tape and reel

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

ABSOLUTE MAXIMUM RATINGS (1) (2)

over operating free-air temperature range unless otherwise noted

PARAMETER			VALUE
Supply voltage range, V_{CC}			−0.3 V to 7 V
Voltage range at any bus terminal (CANH or CANL)			−36 V to 36 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see Figure 7)			−100 V to 100 V
Input voltage range, V_I (D, R, R_S, EN, LBK, AB)			−0.5 V to 7 V
Receiver output current, I_O			−10 mA to 10 mA
Electrostatic discharge	Human Body Model(3)	CANH, CANL and GND	16 kV
Electrostatic discharge	Human Body Model(3)	All pins	3 kV
	Charged-Device Mode(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table
Operating junction temperature, T_J			150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114−A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (separately or common mode)		−7		12	V
High−level input voltage, V_{IH}	D, EN, AB, LBK	2		5.5	V
Low−level input voltage, V_{IL}	D, EN, AB, LBK	0		0.8	V
Differential input voltage, V_{ID}		−6		6	V
Resistance from R_S to ground		0		100	kΩ
Input Voltage at R_S for standby, $V_{I(Rs)}$		0.75V_{CC}		5.5	V
High−level output current, I_{OH}	Driver	−50			mA
	Receiver	−10			
Low−level output current, I_{OL}	Driver			50	mA
	Receiver			10	
Operating junction temperature, T_J	HVD233, HVD234, HVD235			150	°C
Operating free−air temperature(1), T_A	HVD233, HVD234, HVD235	−40		125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D at 0 V, R_S at 0 V, See Figures 1 and 2	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (Recessive)	CANH	D at 3 V, R_S at 0 V, See Figures 1 and 2		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D at 0 V, R_S at 0 V, See Figures 1 and 2	1.5	2	3	V
			D at 0 V, R_S at 0 V, See Figures 2 and 3	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D at 3 V, R_S at 0 V, See Figures 1 and 2	−120		12	mV
			D at 3 V, R_S at 0 V, No Load	−0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 10		1		V
I_{IH}	High-level input current; D, EN, LBK, AB		D at 2 V	−30		30	µA
I_{IL}	Low-level input current; D, EN, LBK, AB		D at 0.8 V	−30		30	µA
I_{OS}	Short−circuit output current		V_{CANH} = −7 V, CANL Open, See Figure 15	−250			mA
			V_{CANH} = 12 V, CANL Open, See Figure 15			1	
			V_{CANL} = −7 V, CANH Open, See Figure 15	−1			
			V_{CANL} = 12 V, CANH Open, See Figure 15			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRs(s)}$	R_S input current for standby		R_S at 0.75 V_{CC}	−10			µA
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC}, R_S at 0 V or V_{CC}		0.05	2	µA
		Standby	R_S at V_{CC}, D at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}		200	600	
		Dominant	D at 0 V, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	mA
		Recessive	D at V_{CC}, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	

(1) All typical values are at 25°C and with a 3.3 V supply.

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_S at 0 V, See Figure 4		35	85	ns
		R_S with 10 kΩ to ground, See Figure 4		70	125	
		R_S with 100 kΩ to ground, See Figure 4		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	R_S at 0 V, See Figure 4		70	120	ns
		R_S with 10 kΩ to ground, See Figure 4		130	180	
		R_S with 100 kΩ to ground, See Figure 4		870	1200	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_S at 0 V, See Figure 4		35		ns
		R_S with 10 kΩ to ground, See Figure 4		60		
		R_S with 100 kΩ to ground, See Figure 4		370		
t_r	Differential output signal rise time	R_S at 0 V, See Figure 4	20		70	ns
t_f	Differential output signal fall time		20		70	
t_r	Differential output signal rise time	R_S with 10 kΩ to ground, See Figure 4	30		135	ns
t_f	Differential output signal fall time		30		135	
t_r	Differential output signal rise time	R_S with 100 kΩ to ground, See Figure 4	350		1400	ns
t_f	Differential output signal fall time		350		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figures 8 and 9		0.6	1.5	µs
$t_{en(z)}$	Enable time from sleep to dominant			1	5	

(1) All typical values are at 25°C and with a 3.3 V supply.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		AB at 0 V, LBK at 0 V, EN at V_{CC}, See Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage				500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					100		
V_{OH}	High-level output voltage		I_O = −4 mA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage		I_O = 4 mA, See Figure 6				0.4	
I_I	Bus input current		CANH or CANL at 12 V	Other bus pin at 0 V, D at 3 V, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}	150		500	µA
			CANH or CANL at 12 V, V_{CC} at 0 V		200		600	
			CANH or CANL at −7 V		−610		−150	
			CANH or CANL at −7 V, V_{CC} at 0 V		−450		−130	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			20		
R_{ID}	Differential input resistance		D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}		40		100	kΩ
R_{IN}	Input resistance (CANH or CANL)				20		50	
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC}, Rs at 0 V or V_{CC}			0.05	2	µA
		Standby	R_S at V_{CC}, D at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}			200	600	
		Dominant	D at 0 V, No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	mA
		Recessive	D at V_{CC}, No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	

(1) All typical values are at 25°C and with a 3.3 V supply.

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			7		
t_r	Output signal rise time			2	5	
t_f	Output signal fall time			2	5	

(1) All typical values are at 25°C and with a 3.3 V supply.

DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233	See Figure 12		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	HVD235	See Figure 13		10	20	ns
$t_{(AB2)}$	Loopback delay, bus input to receiver output		See Figure 14		35	60	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S at 0 V, See Figure 11		70	135	ns
			R_S with 10 kΩ to ground, See Figure 11		105	190	
			R_S with 100 kΩ to ground, See Figure 11		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S at 0 V, See Figure 11		70	135	ns
			R_S with 10 kΩ to ground, See Figure 11		105	190	
			R_S with 100 kΩ to ground, See Figure 11		535	1000	

(1) All typical values are at 25°C and with a 3.3 V supply.

PARAMETER MEASUREMENT INFORMATION

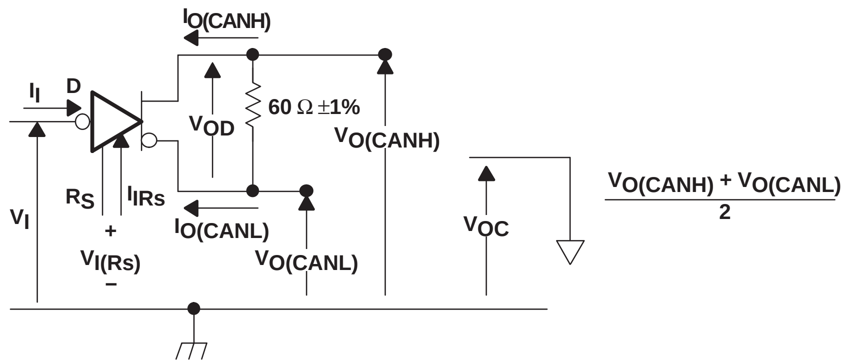


Figure 1. Driver Voltage, Current, and Test Definition

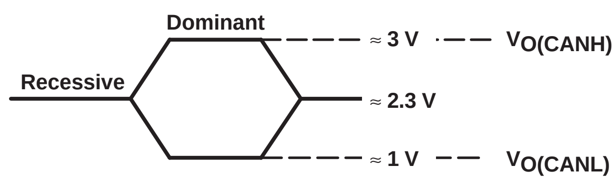


Figure 2. Bus Logic State Voltage Definitions

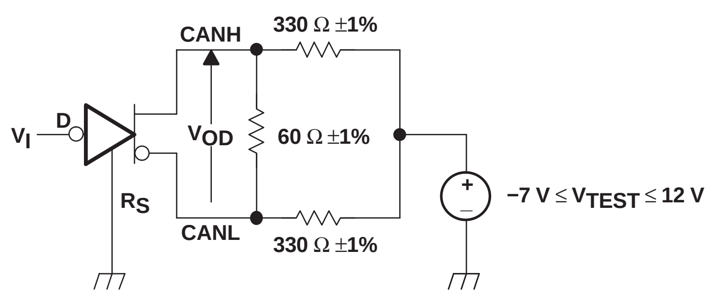
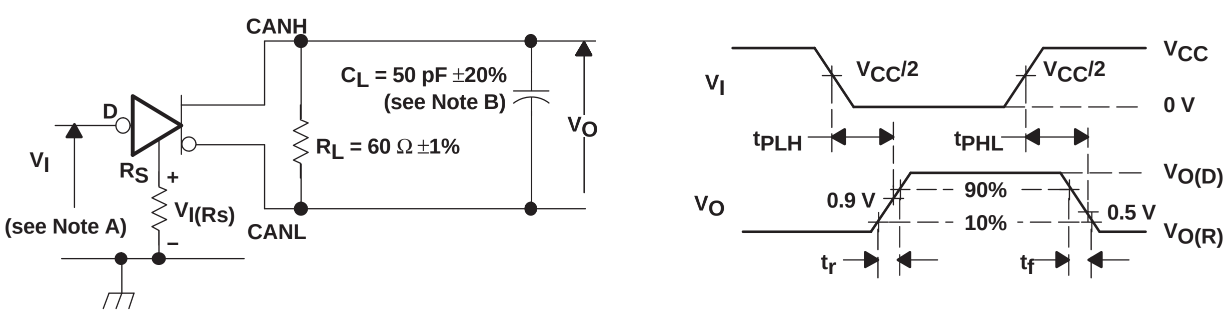


Figure 3. Driver V_{OD}



NOTES:A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ns, $t_f \leq 6$ns, $Z_O = 50\Omega$.

B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

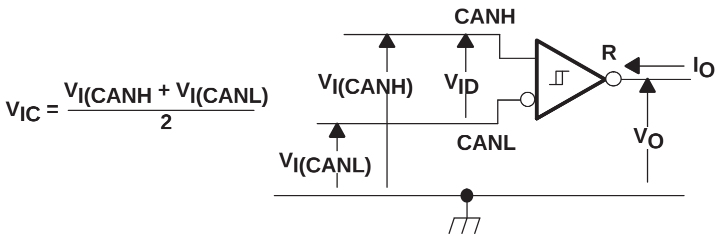
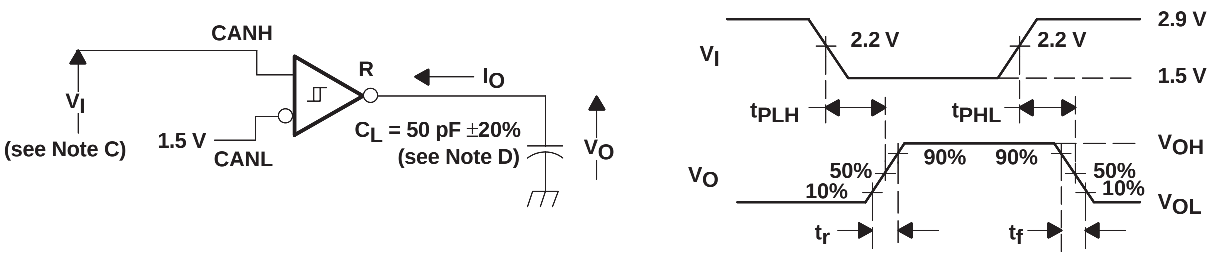


Figure 5. Receiver Voltage and Current Definitions



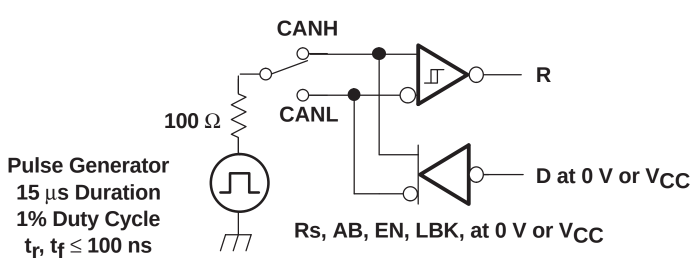
NOTES:C. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \le$ 6ns, $t_f \le$ 6ns, Z_O = 50Ω.

D. C_L includes fixture and instrumentation capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

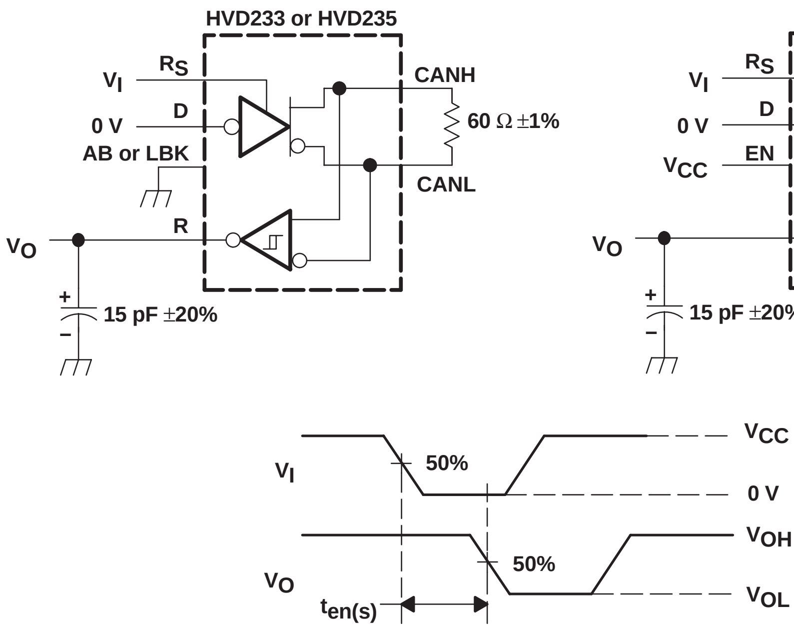
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID} \rvert$
−6.1 V	−7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
−1 V	−7 V	L		6 V
12 V	6 V	L		6 V
−6.5 V	−7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
−7 V	−1 V	H		6 V
6 V	12 V	H		6 V
open	open	H		X



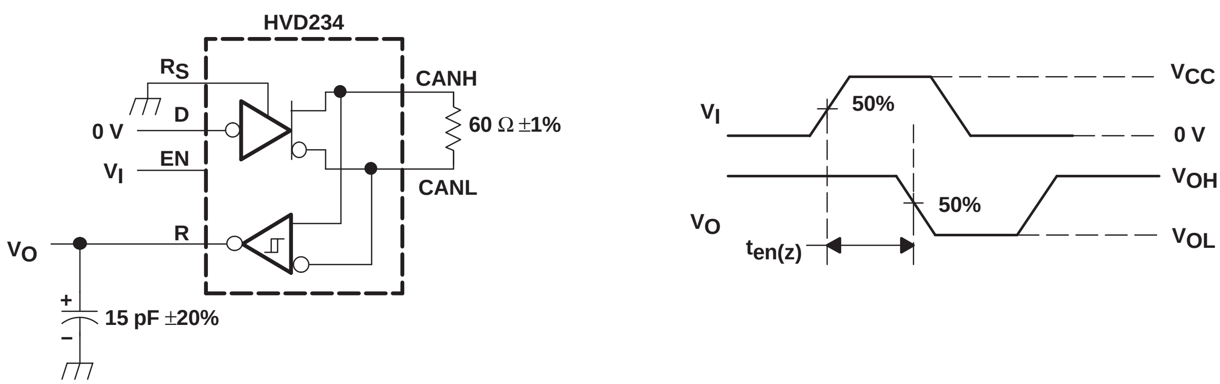
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Over Voltage Test



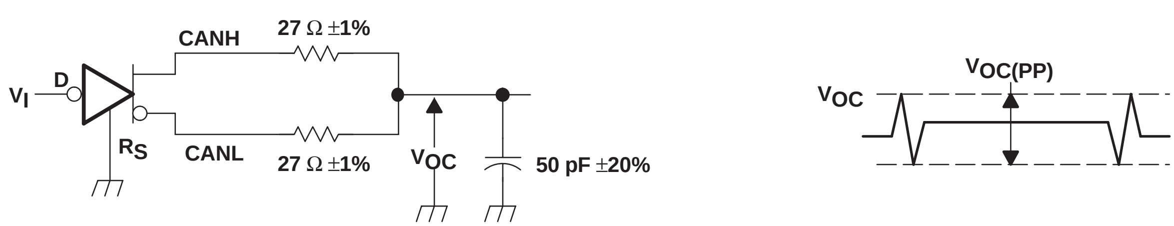
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. $t_{en(s)}$ Test Circuit and Voltage Waveforms



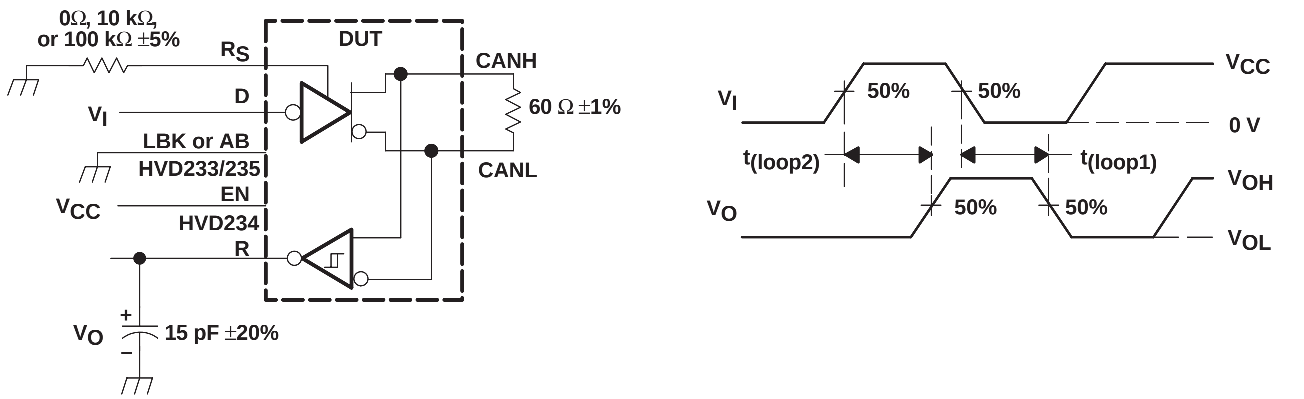
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 50 kHz, 50% duty cycle.

Figure 9. $t_{en(z)}$ Test Circuit and Voltage Waveforms



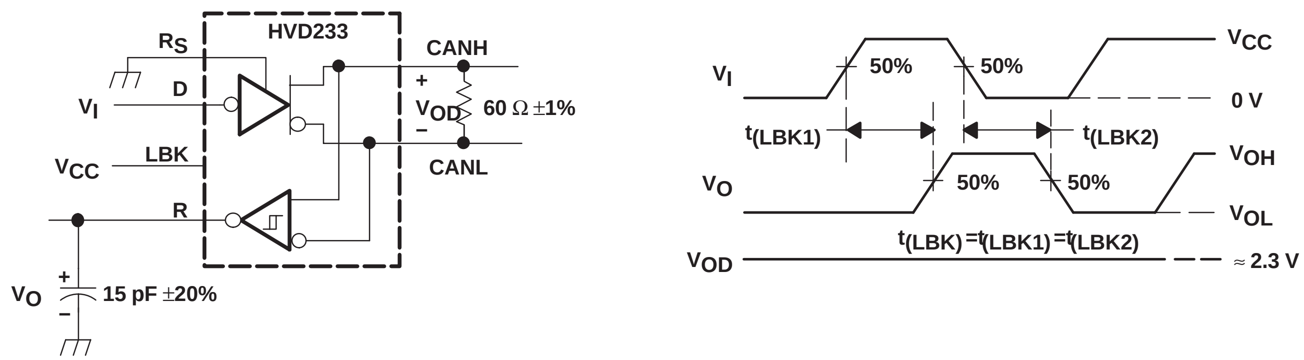
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



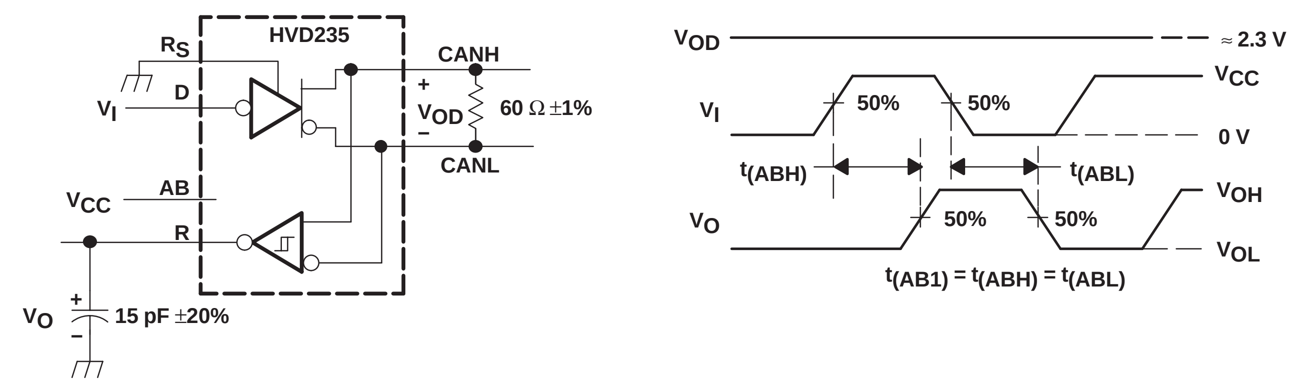
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. $t_{(loop)}$ Test Circuit and Voltage Waveforms



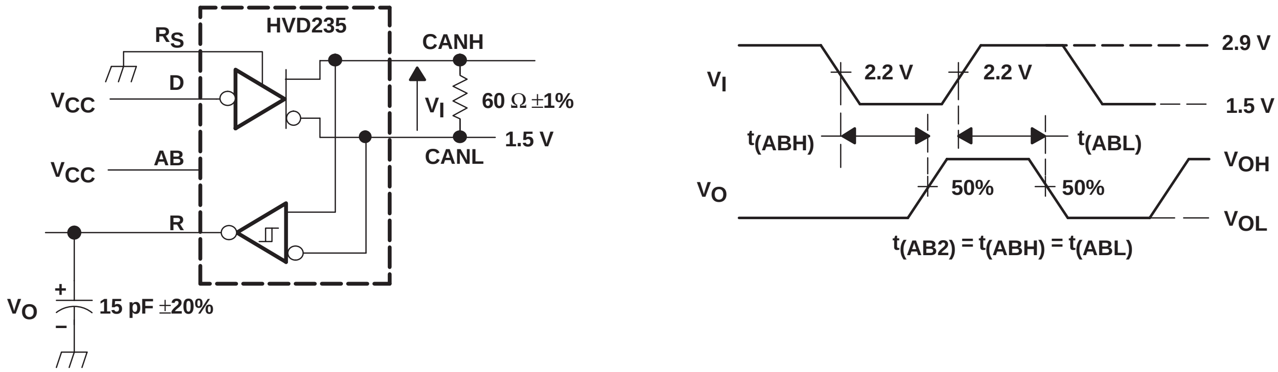
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 12. $t_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 13. $t_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 14. $t_{(AB2)}$ Test Circuit and Voltage Waveforms

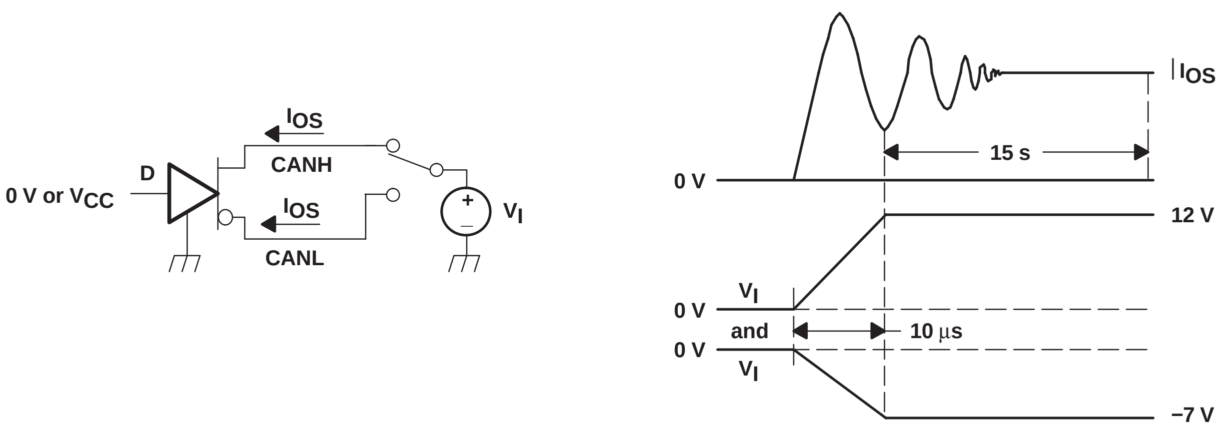
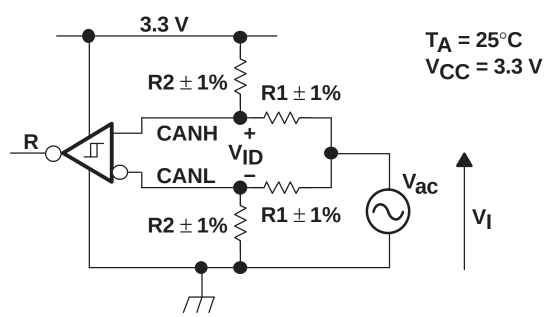
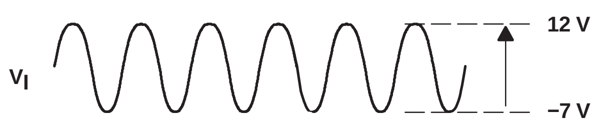


Figure 15. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω

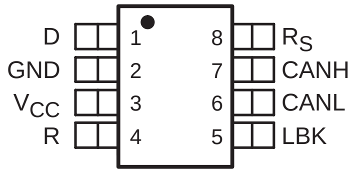


NOTE: All input pulses are supplied by a generator with f ≤ 1.5 MHz.

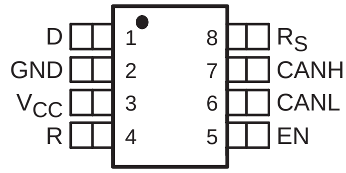
Figure 16. Common-Mode Voltage Rejection

DEVICE INFORMATION

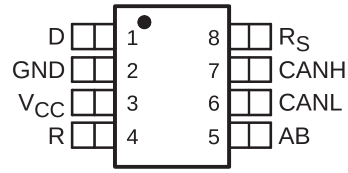
SN65HVD233D
(Marked as VP233)
(TOP VIEW)



SN65HVD234D
(Marked as VP234)
(TOP VIEW)



SN65HVD235D
(Marked as VP235)
(TOP VIEW)



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

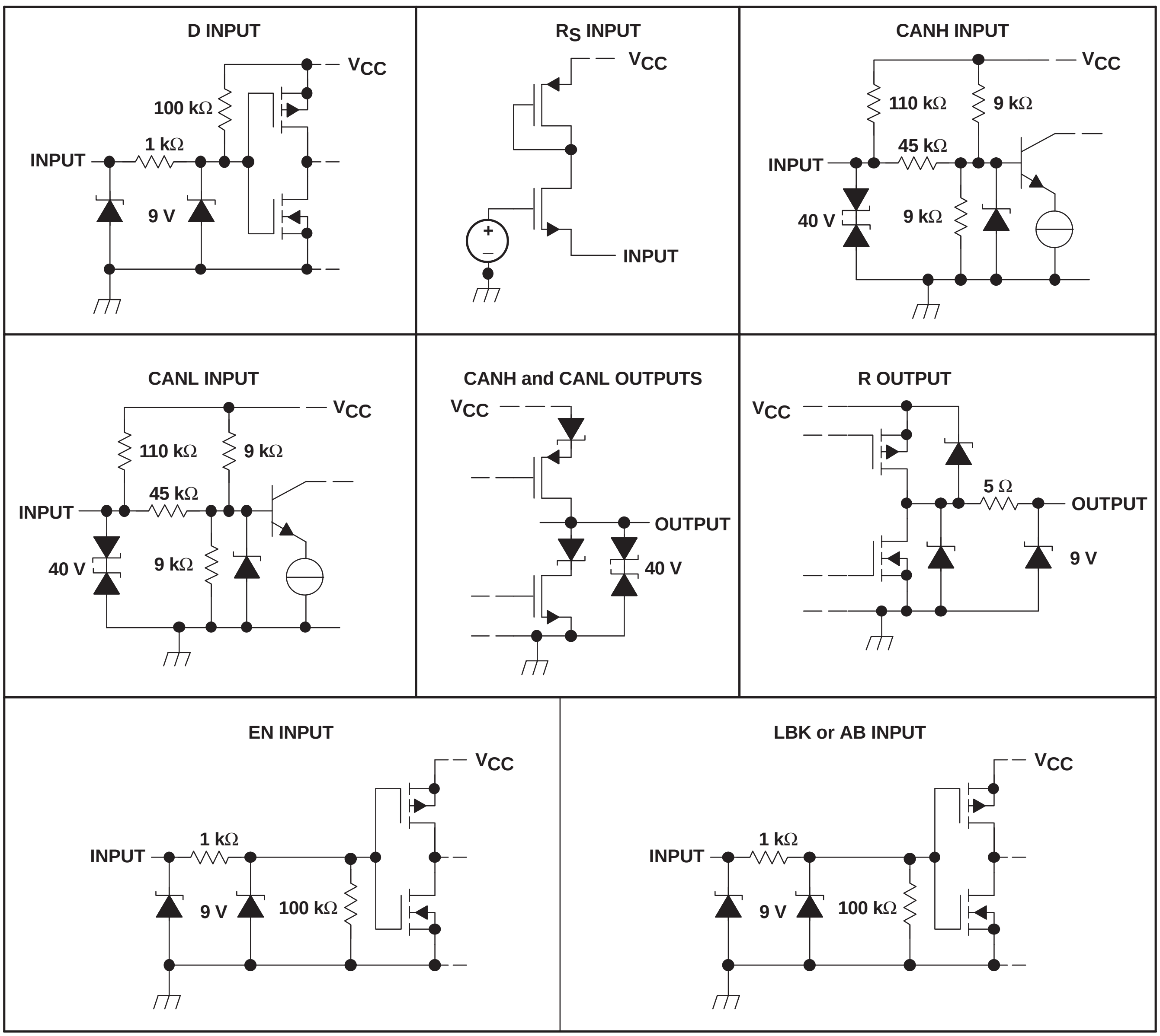


Table 2. Thermal Characteristics

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance(1)	Low-K(2) board, no air flow	185	°C/W
		High-K(3) board, no air flow	101	
Θ_{JB}	Junction-to-board thermal resistance	High-K(3) board, no air flow	82.8	°C/W
Θ_{JC}	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	R_L = 60 Ω, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, T_A = 25°C	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

(1) See TI literature number SZZA003 for an explanation of this parameter.
(2) JESD51−3 low effective thermal conductivity test board for leaded surface mount packages.
(3) JESD51−7 high effective thermal conductivity test board for leaded surface mount packages.

FUNCTION TABLES

DRIVER (SN65HVD233 OR SN65HVD235)					
INPUTS			OUTPUTS		
D	LBK/AB	R_S	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

RECEIVER (SN65HVD233)				
INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R
Dominant	V_{ID} ≥ 0.9 V	L or open	X	L
Recessive	V_{ID} ≤ 0.5 V or open	L or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	L or open	H or open	?
X	X	H	L	L
X	X		H	H

RECEIVER (SN65HVD235)				
INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	AB	D	R
Dominant	V_{ID} ≥ 0.9 V	L or open	X	L
Recessive	V_{ID} ≤ 0.5 V or open	L or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	L or open	H or open	?
Dominant	V_{ID} ≥ 0.9 V	H	X	L
Recessive	V_{ID} ≤ 0.5 V or open	H	H	H
Recessive	V_{ID} ≤ 0.5 V or open	H	L	L
?	0.5 V < V_{ID} < 0.9 V	H	L	L

DRIVER (SN65HVD234)					
INPUTS			OUTPUTS		
D	EN	R_S	CANH	CANL	Bus State
L	H	≤ 0.33 V_{CC}	H	L	Dominant
H	X	≤ 0.33 V_{CC}	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	> 0.75 V_{CC}	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

RECEIVER (SN65HVD234)			
INPUTS			OUTPUT
Bus State	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	EN	R
Dominant	$V_{ID} \geq 0.9$ V	H	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H
?	0.5 V < V_{ID} < 0.9 V	H	?
X	X	L or open	H

H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE

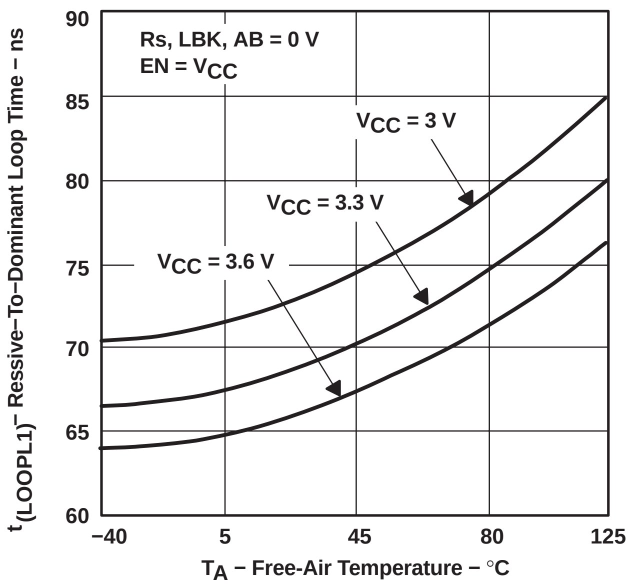


Figure 17

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE

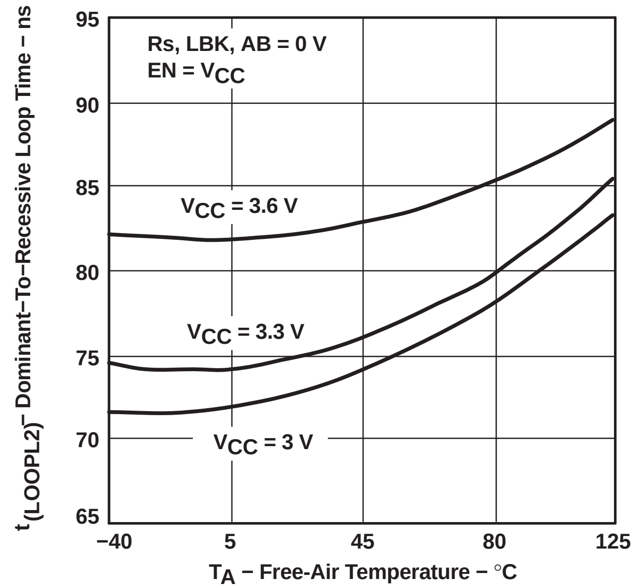


Figure 18

SUPPLY CURRENT
vs
FREQUENCY

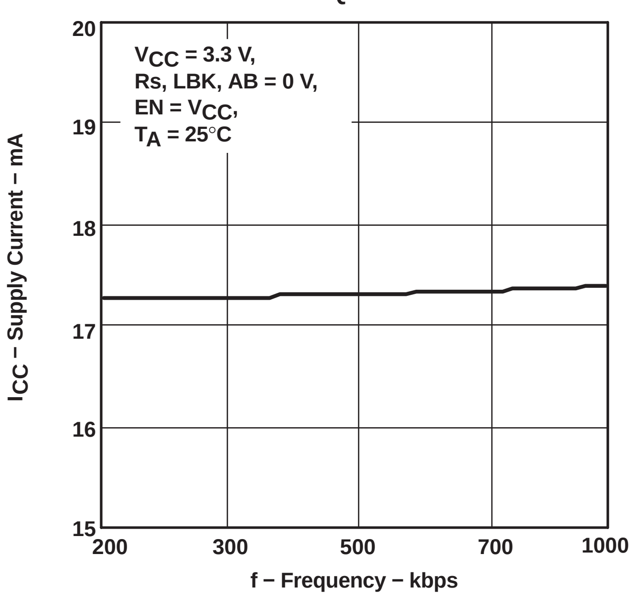


Figure 19

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

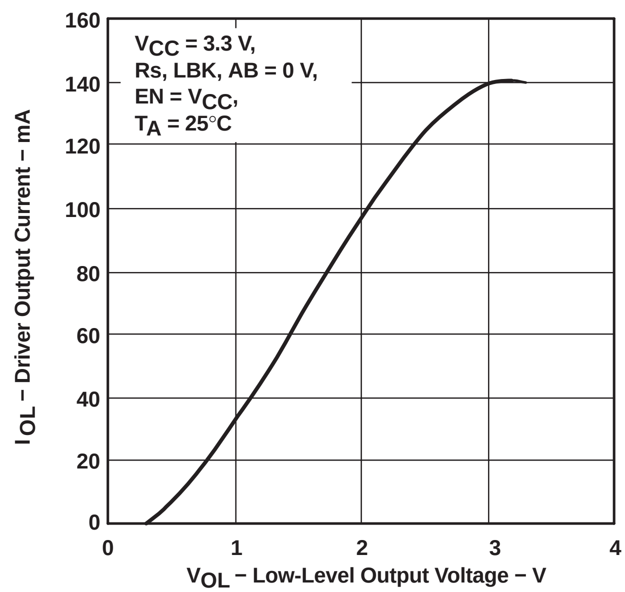


Figure 20

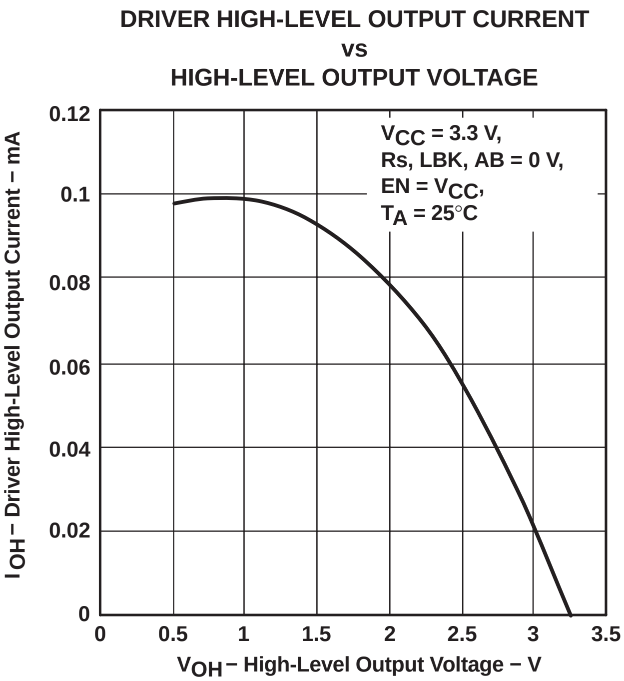


Figure 21

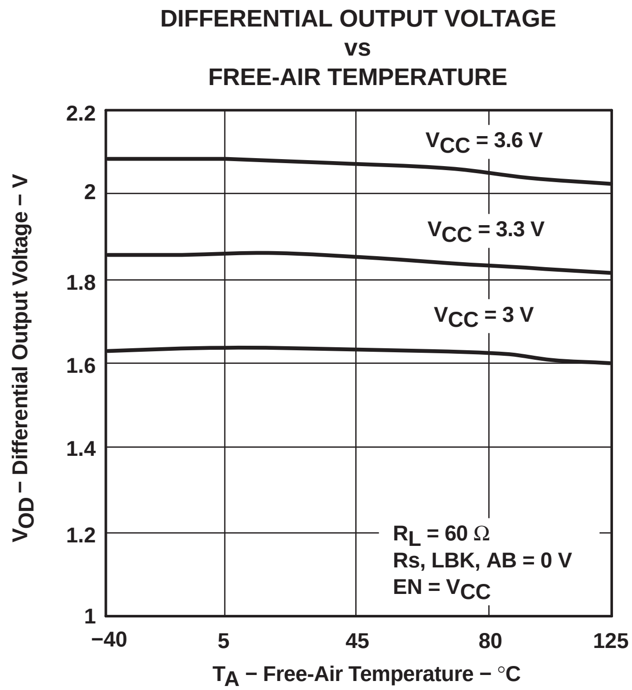


Figure 22

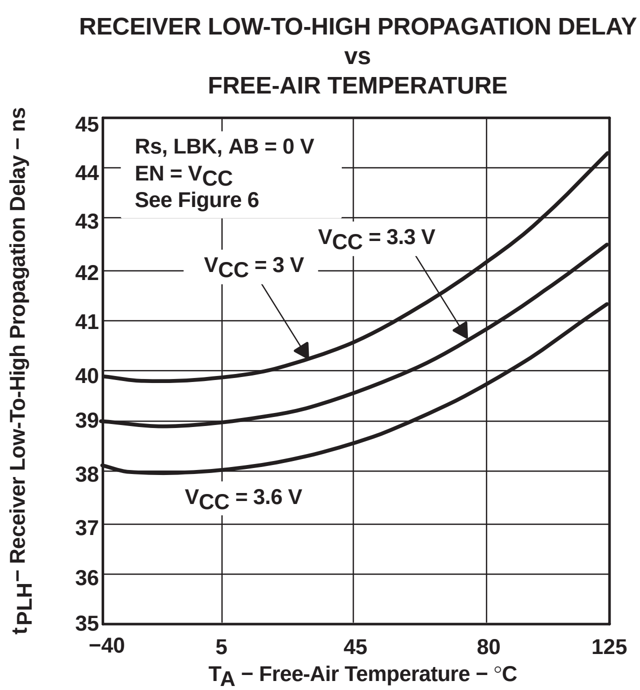


Figure 23

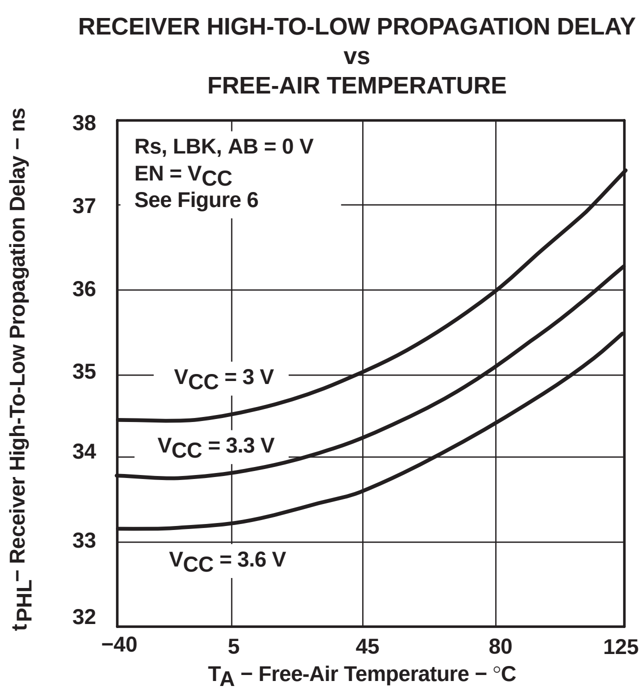


Figure 24

DRIVER LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

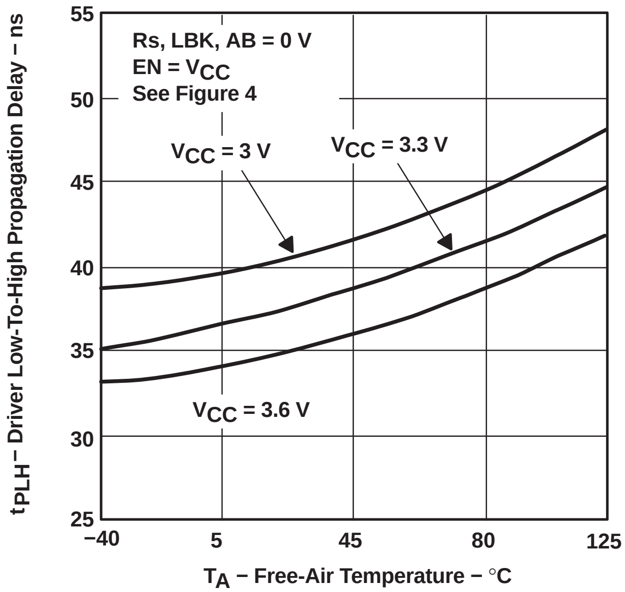


Figure 25

DRIVER HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

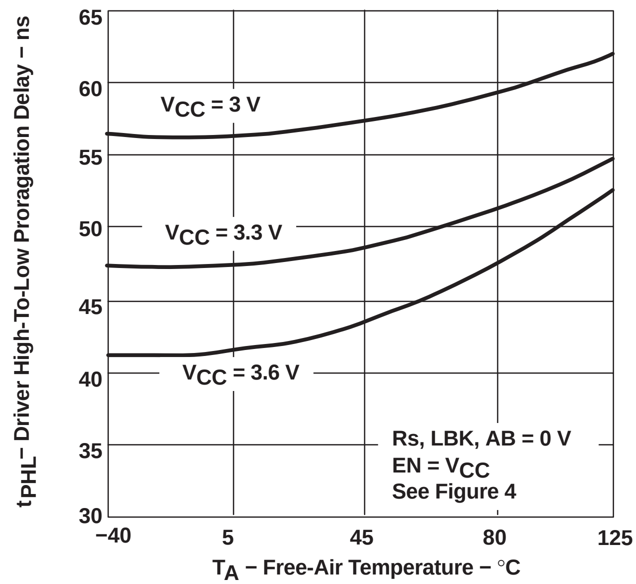


Figure 26

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

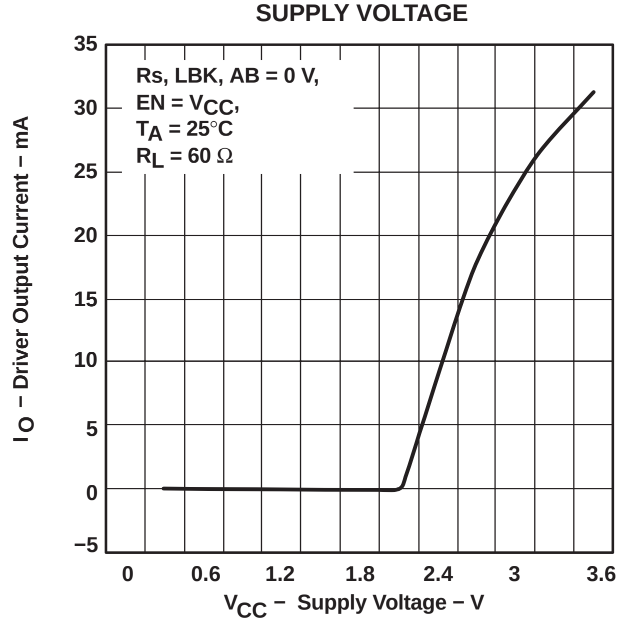


Figure 27

APPLICATION INFORMATION

Diagnostic Loopback (SN65HVD233)

The loopback (LBK) function of the HVD233 is enabled with a high-level input to pin 5. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data output (R) at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 28.

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low−level input) and may be left open if not in use.

Autobaud Loopback (SN65HVD235)

The autobaud feature of the HVD235 is implemented by placing a logic high on pin 5 (AB). In autobaud, the *bus-transmit* function of the transceiver is disabled, while the *bus-receive* function and all of the normal operating functions of the device remain intact. With the autobaud function engaged, normal bus activity can be monitored by the device. However, if an error frame is generated by the local CAN controller, it is not transmitted to the bus. Only the host microprocessor can detect the error frame.

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, a popular industrial application has optional settings of 125 kbps, 250 kbps, or 500 kbps. Once the logic high has been applied to pin 5 (AB) of the HVD235, assume a baud rate such as 125 kbps, then wait for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the host CAN controller. However, since the *bus-transmit* function of the device has been disabled, no other nodes receive the error message of the controller.

This procedure makes use of the CAN controller’s status register indications of message received and error warning status to signal if the current baud rate is correct or not. The warning status indicates that the CAN chip error counters have been incremented. A message received status indicates that a good message has been received.

If an error is generated, reset the CAN controller with another baud rate, and wait to receive another message. When an error-free message has been received, the correct baud rate has been detected. A logic low may now be applied to pin 5 (AB) of the HVD235, returning the *bus-transmit* normal operating function to the transceiver.

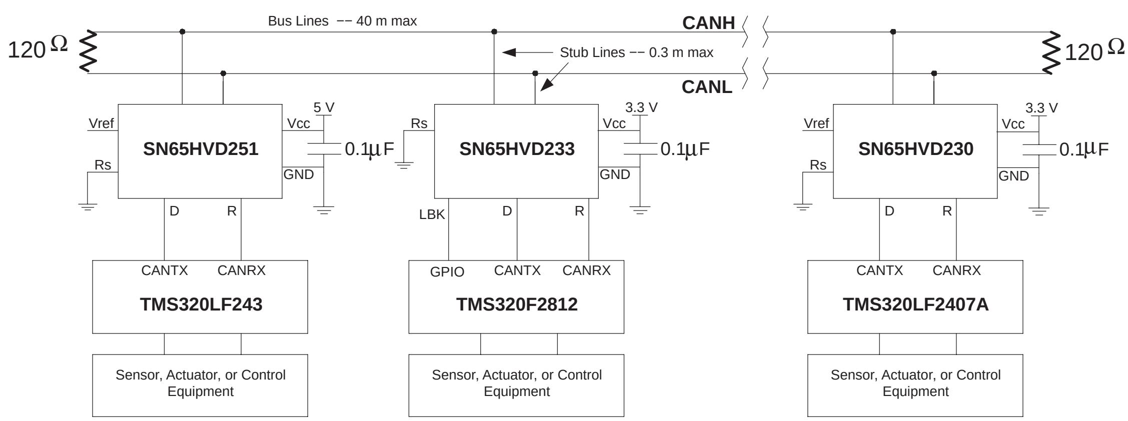


Figure 28. Typical HVD233 Application

Interoperability With 5-V CAN Systems

ISO−11898 specifies the interface characteristics to a CAN bus with the purpose of insuring interchangeability among compatible transceivers. While the levels specified in the standard assume a 5-V supply, there is nothing in the standard that makes this a requirement. The SN65HVD233 is compatible with these requirements with a 3.3-V supply, assuring interoperability with 5-V supplied transceivers.

Bus Cable

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the HVD233.

The standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections.

Slope Control

The rise and fall slope of the SN65HVD233, SN65HVD234, and SN65HVD235 driver output can be adjusted by connecting a resistor from the Rs (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 29.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ≈ 15 V/μs slew rate, and up to 100 kΩ to achieve a ≈ 2.0 V/μs slew rate as displayed in Figure 30. Typical driver output waveforms with slope control are displayed in Figure 31.

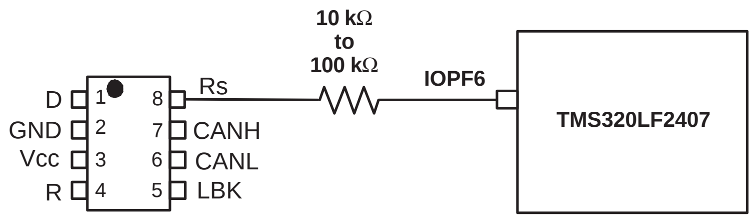


Figure 29. Slope Control/Standby Connection to a DSP

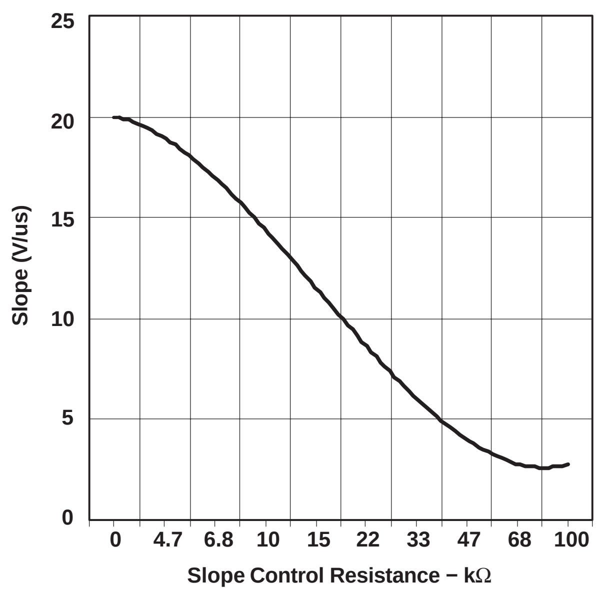


Figure 30. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

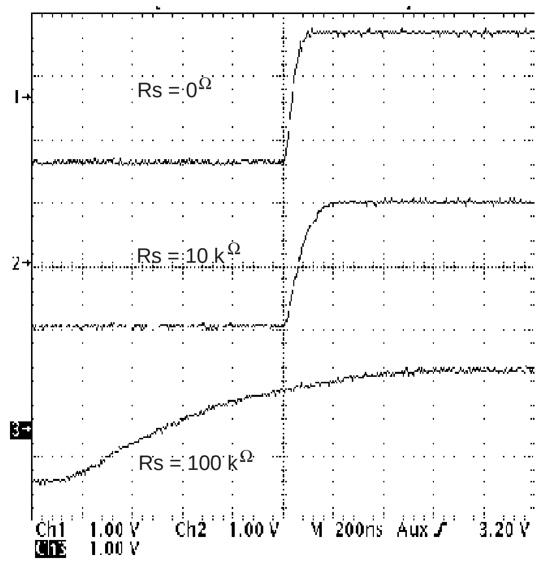


Figure 31. Typical SN65HVD233 250-kbps Output Pulse Waveforms With Slope Control

Standby

If a high−level input (> 0.75 V_{CC}) is applied to Rs (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900 mV typical) occurs on the bus.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65HVD233D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD233DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD233DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD233DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD234D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD234DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD234DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD234DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD235D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD235DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD235DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD235DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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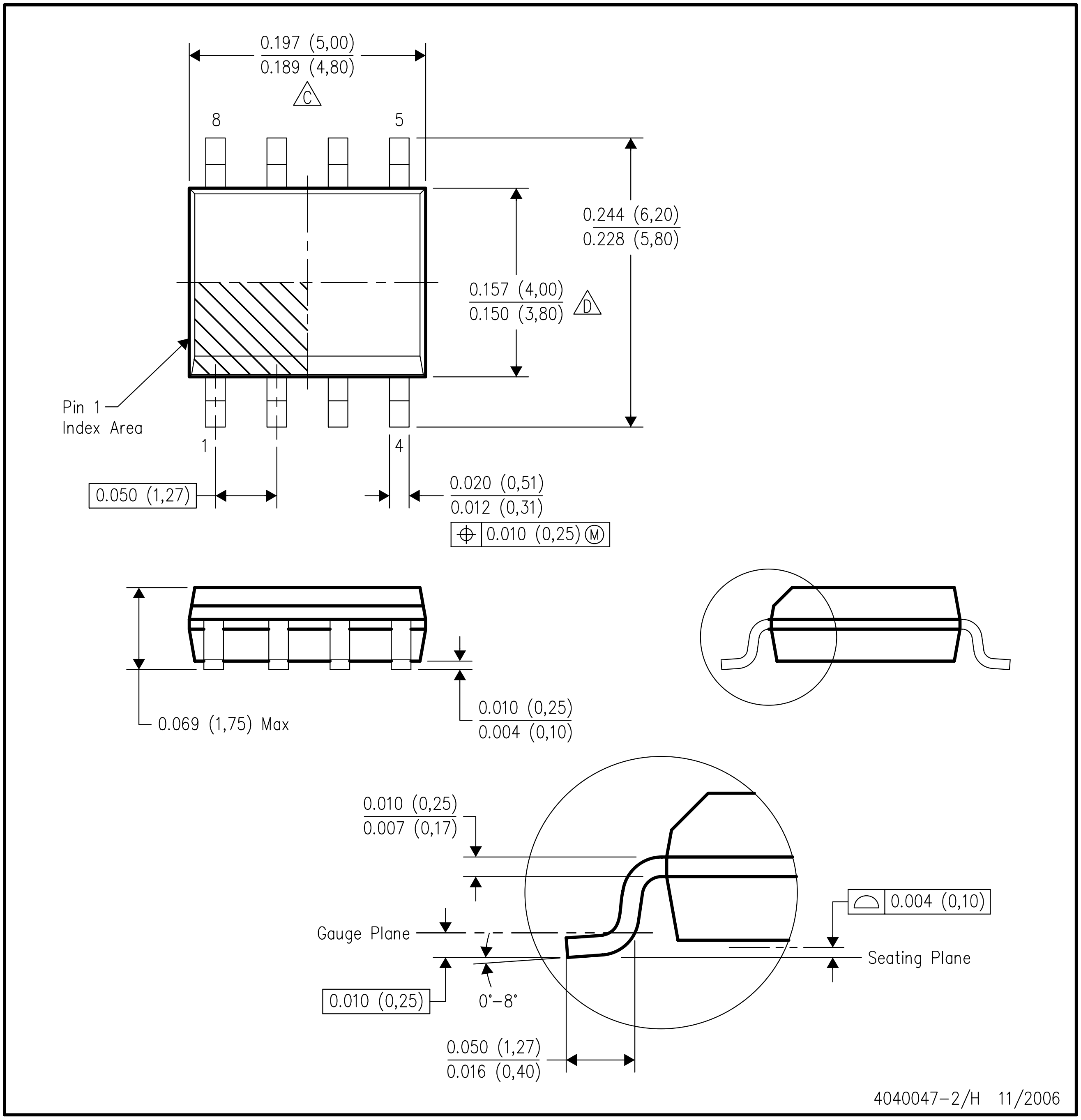
D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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