DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD71055

PARALLEL INTERFACE UNIT

uPD71055

PARALLEL INTERFACE UNIT

The uPD71055 is a programmable parallel interface unit for use in microcomputer systems. The uPD71055 is provided with three I/O ports and is capable of operations ranging from basic input/output to high level operations using handshaking protocols.
The uPD71055, fabricated by CMOS technology, realizes low power consumption.

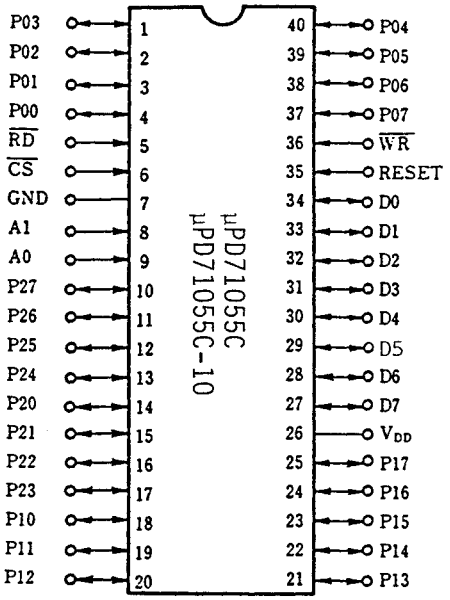
FEATURES

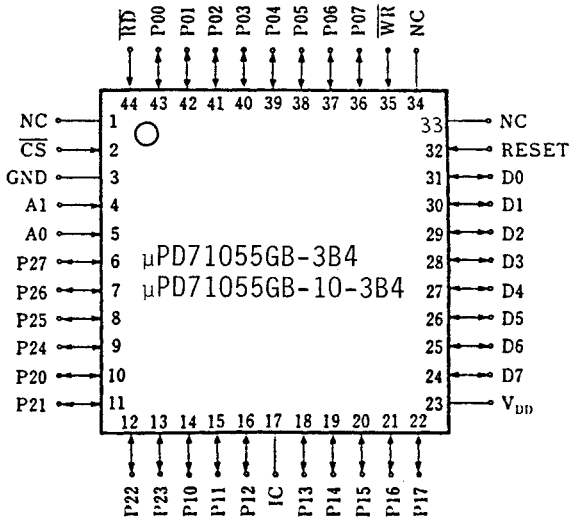
- Three 8-bit I/O ports
- Three programmable operation modes
- Bit manipulation command
- Microcomputer compatible
- No-wait operation with uPD70108-10 and uPD70116-10
- CMOS
- Single power supply

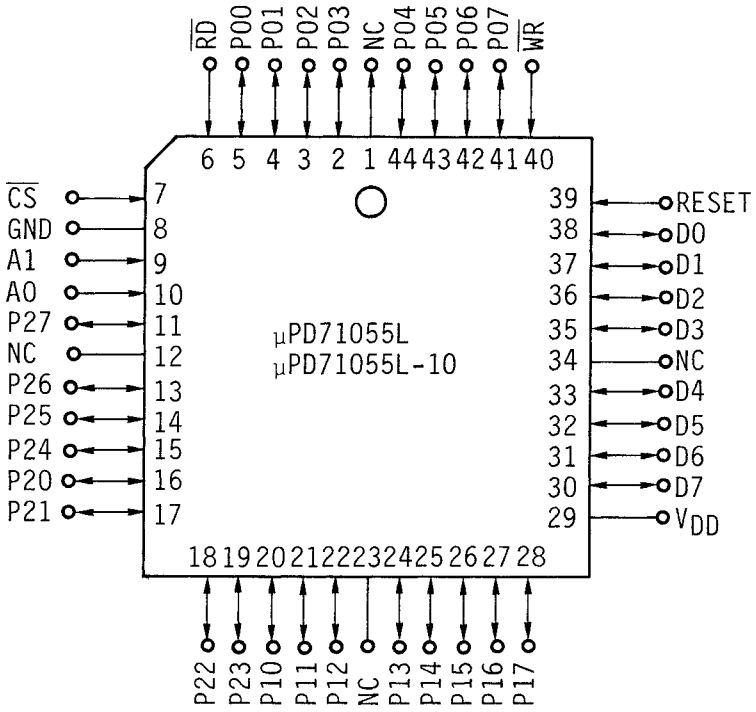
ORDERING INFORMATION

Part Number	Package	Recovery time [ns]
uPD71055C	40-pin plastic DIP	200
uPD71055C-10	40-pin plastic DIP	150
uPD71055GB-3B4	44-pin plastic QFP	200
uPD71055GB-10-3B4	44-pin plastic QFP	150
uPD71055L	44-pin PLCC	200
uPD71055L-10	44-pin PLCC	150

PIN CONFIGURATION (Top View)



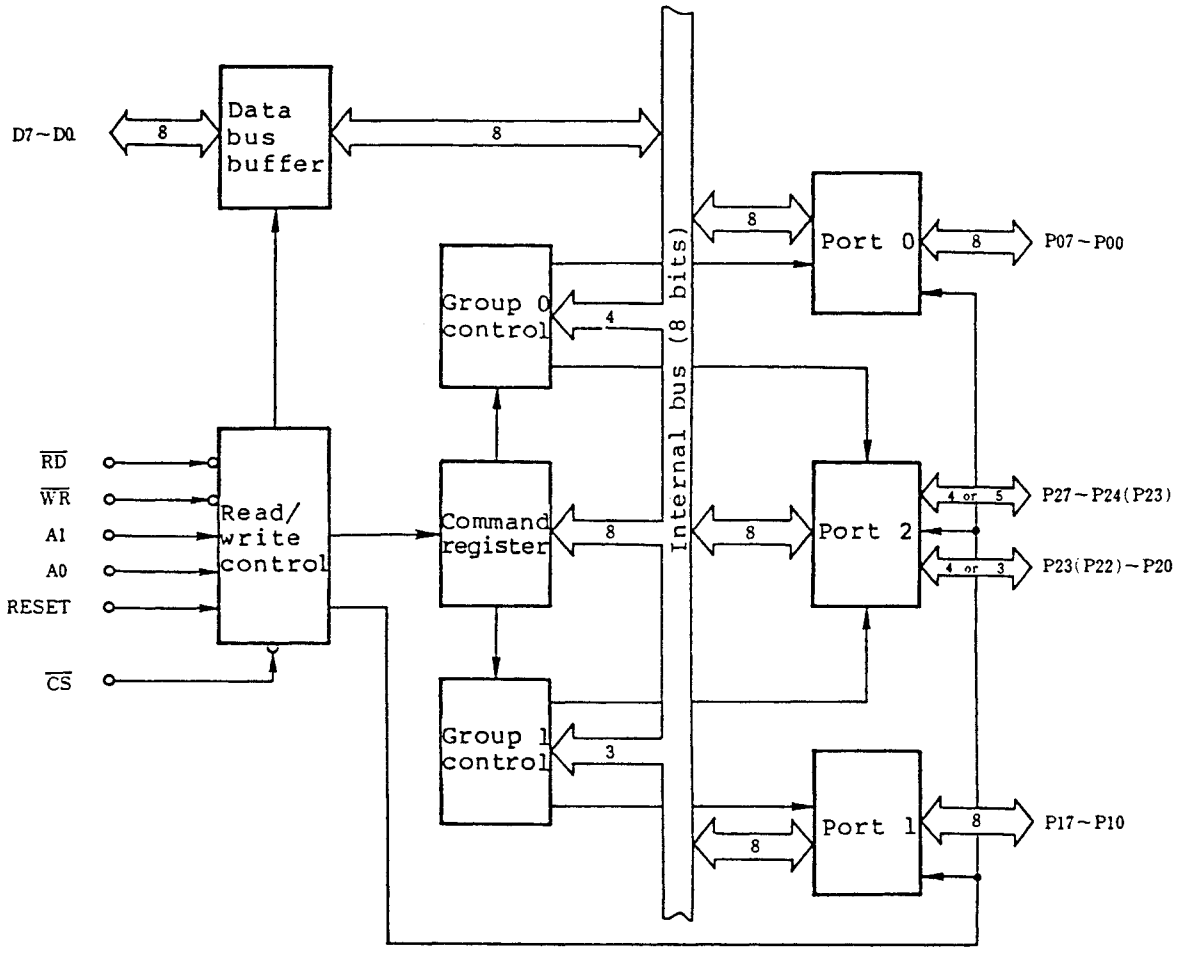




Pin Identification

D7 to D0	:	Data Bus	RESET	:	Reset
RD	:	Read Strobe	P07 to P00	:	Port 0
WR	:	Write Strobe	P17 to P10	:	Port 1
CS	:	Chip Select	P27 to P20	:	Port 2
A1, A0	:	Address	NC	:	Non-connection

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 D7 to D0 (data bus) - Three-state input/output

These pins form an 8-bit, three-state, bidirectional data bus. They are connected to the system data bus and are used for data communication. Active when $\overline{CS}$=0 and $\overline{RD}$=0 or $\overline{WR}$=0, otherwise these pins enter the high impedance.

1.2 $\overline{CS}$ (chip select) - Input

This signal is used to select the uPD71055. When $\overline{CS}$=0, the uPD71055 is selected. $\overline{CS}$=1 indicates nonselect and causes the lines of the data bus to become high impedance.

1.3 $\overline{RD}$ (read strobe) - Input

This signal is logic 0 when a read operation of data from the uPD71055 is being performed.

1.4 $\overline{WR}$ (write strobe) - Input

When data are to be written to the uPD71055, a logic 0 signal should be input to this pin. The contents of the data bus are then written to the uPD71055 at the rising edge (from 0 to 1) of the $\overline{WR}$ signal.

1.5 A1, A0 (address) - Input

These two inputs are used in combination with the $\overline{RD}$ and $\overline{WR}$ signals and select from among the three ports and the command register. These pins are normally connected to the lower 2 bits (A1, A0) of the system address bus.

1.6 RESET (reset) - Input

When the input to the RESET pin become high level, the group 0 and group 1 ports are set to mode 0 (basic I/O port mode) and all ports are set for input.

1.7 P07 to P00 (Port 0) - Three-state input/output

These are the port 0 input/output pins.

1.8 P17 to P10 (Port 1) - Three-state input/output

These are the port 1 input/output pins.

1.9 P27 to P20 (Port 2) - Three-state input/output

These are the port 2 input/output pins.

1.10 IC (Internally Connected)

This pin must be left unconnected.

2. BLOCK FUNCTIONS

The uPD71055 is designed to be used as a parallel interface between a microcomputer system and its peripheral devices. Because the uPD71055 can be controlled by the program of the microcomputer system, external logic circuits can be reduced to a minimum. The uPD71055 consists of these five blocks: the data bus buffer, the read/write control, the command register, group control, and three I/O ports.

2.1 Data Bus Buffer

This is an 8-bit, three-state, bidirectional buffer that serves as an interface between the uPD71055 and the system data bus. When the CPU executes IN or OUT instructions for the uPD71055, the data is sent or received via this buffer.

2.2 Read/Write Control

This block decodes the data input from the system bus and controls the data bus buffer data direction, the command register, and the three ports.

2.3 Command Register

Command words sent from the CPU are written to this register. Then, in accordance with the command, control signals are sent either to the group 0 control, the group 1 control, or to both. Note that the contents of this register cannot be read.

2.4 Group 0 Control, Group 1 Control

These blocks control the operation of the group 0 and group 1 ports in accordance with the mode set for each group.

2.5 Ports 0, 1, 2

The uPD71055 has three 8-bit I/O ports, referred to as port 0, port 1, and port 2. These ports are further divided into two groups with port 0 and the higher bits of port 2 belonging to group 0, and port 1 and the lower bits of port 2 belonging to group 1. Modes can be set independently for each group. There is also a bit manipulation instruction that can be used for bit-wise set/reset operations for port 2.

3. READ/WRITE TO THE uPD71055

To access the uPD71055, the $\overline{CS}$ signal should first be set to 0. Then the $\overline{WR}$ or $\overline{RD}$ signal should be set to 0 to specify a write or read operation. The input at the A1 and A0 pins specifies the port or command register to which the read or write operation is to be performed. When a write operation is performed to the command register, it is assumed that the data written is a command word.

Table 3-1 Control Signals and Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Operation	CPU Operation
0	0	1	0	0	Port 0 → Data bus	Input
0	0	1	0	1	Port 1 → Data bus	Input
0	0	1	1	0	Port 2 → Data bus	Input
0	0	1	1	1	Use prohibited	
0	0	0	x	x		
0	1	0	0	0	Data bus → Port 0	Output
0	1	0	0	1	Data bus → Port 1	Output
0	1	0	1	0	Data bus → Port 2	Output
0	1	0	1	1	Data bus → Command register	Output
0	1	1	x	x	Data bus high impedance	
1	x	x	x	x		

x: don't care

4. uPD71055 COMMANDS

The uPD71055 is provided with two commands that it uses to control its own operation. These are the mode select command that determines the operation of the group 0 and group 1 ports and the other is the bit manipulation command that sets/resets the bits of port 2. Both of these commands are executed by writing an 8-bit command word to the command register.

4.1 Mode Select

The uPD71055 has three modes that can be specified for the different groups. Mode 2, however, can only be specified for group 0.

(1) Mode 0

Specifies basic input/output port operation.

(2) Mode 1

Specifies operation controlled by a control/status signal (4 or 3 bits of port 2).

(3) Mode 2

This mode can only be specified for group 0 and specifies port operation in which the higher 5 bits of port 2 are used for control and status signals and port 0 is used as a bidirectional I/O port.

To specify the mode, set bit 7 of the command word to '1' and then write to the command register (A1A0=11) setting the value of each bit in accordance with the values shown in Fig. 4-1.

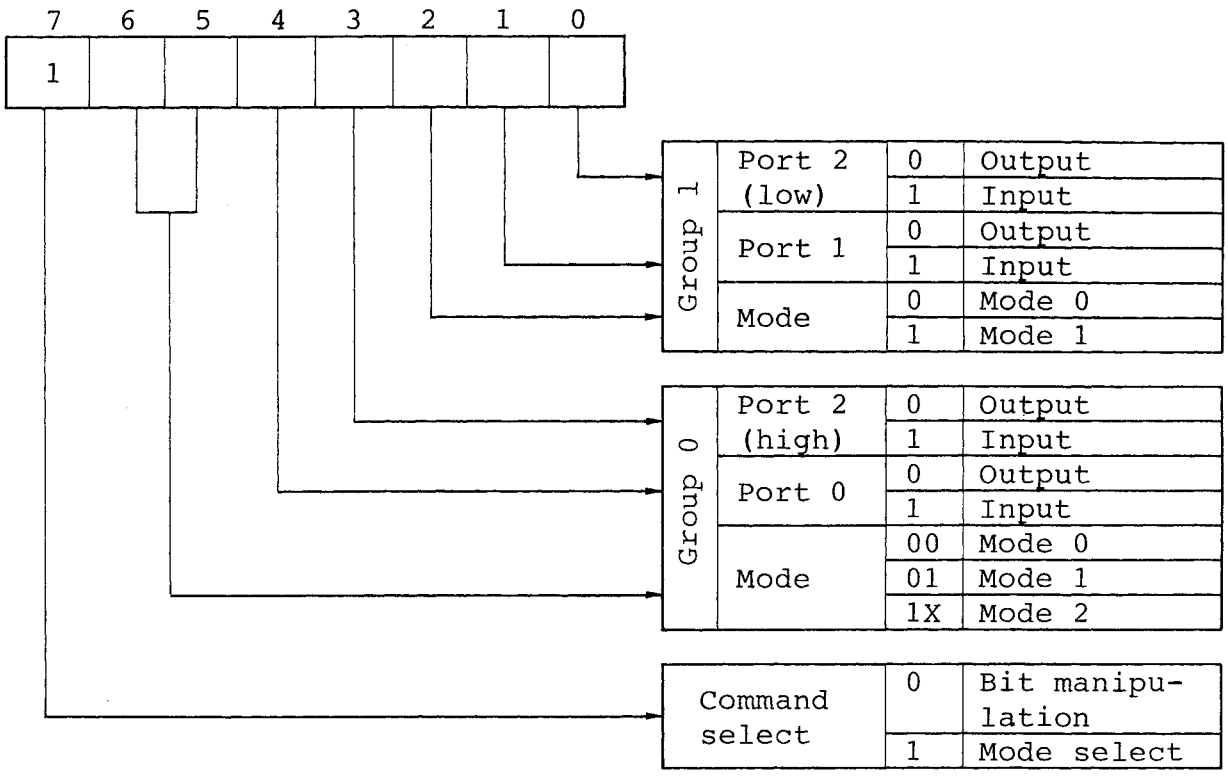


Fig. 4-1 Mode Select Command Word

4.2 Bit Manipulation Command

This command port 2. This type of operation is especially useful in mode 1 and mode 2 where the bits of port 2 are used as control/status signals. By executing this command, interrupts can be enabled and disabled from the CPU. Also, since direct write to port 2 (A1A0=10) is only possible in mode 0, this command can be used in mode 1 to directly write 1- or 2-bit output values.

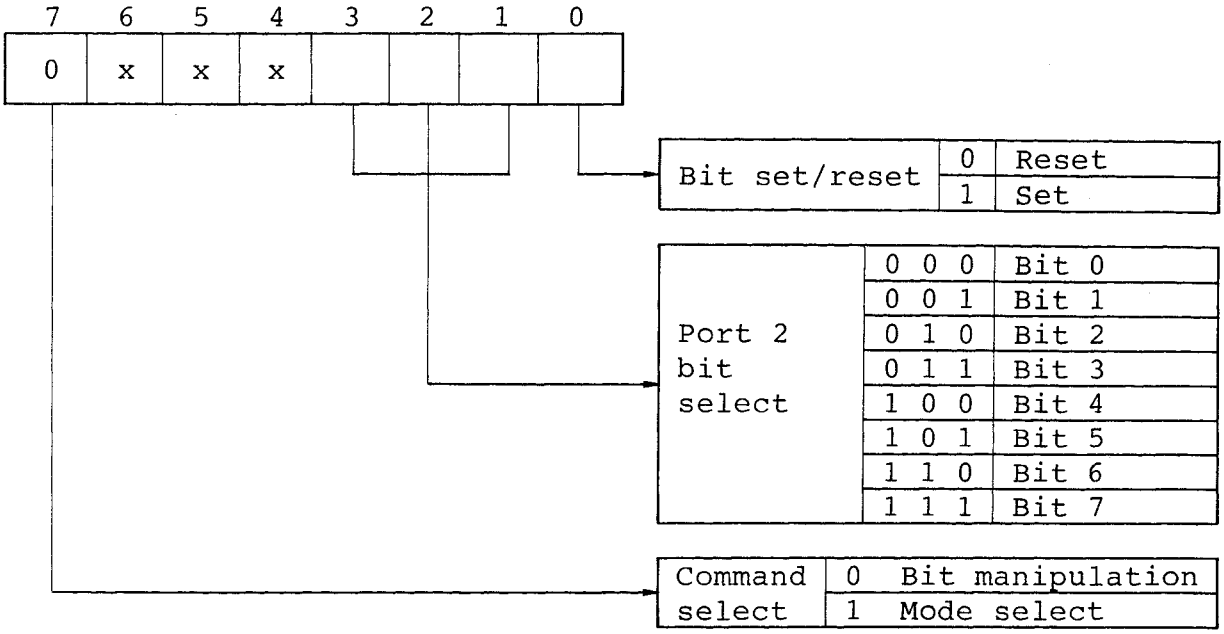


Fig. 4-2 Bit Manipulation Command Word

For example, to set bit 2 of port 2 to '1', the command word shown below (05H) should be set in the command register.

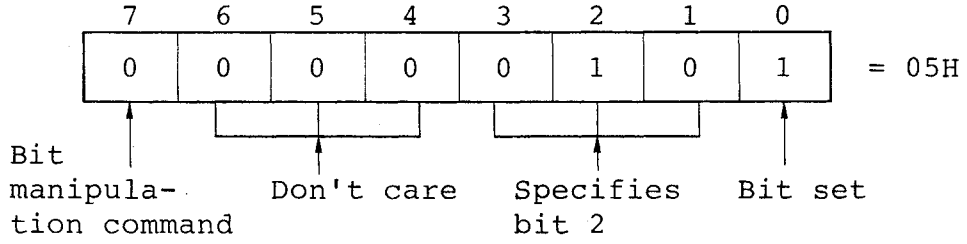


Fig. 4-3 Bit Manipulation Instruction Example

Note:
The bits of all ports are cleared when the PD71055 is reset, or when mode selection is performed.

5. OPERATION IN EACH MODE

In the uPD71055, the operation mode for each group can be set according to the application. The following mode setting combinations are possible:

(1) Group 0: mode 0; group 1: mode 0
(2) Group 0: mode 0; group 1: mode 1
(3) Group 0: mode 1; group 1: mode 0
(4) Group 0: mode 1; group 1: mode 1
(5) Group 0: mode 2; group 1: mode 0
(6) Group 0: mode 2; group 1: mode 1

The $\overline{RD}$ and $\overline{WR}$ signals that appear in the descriptions of each mode refer to the $\overline{RD}$ and $\overline{WR}$ signals of the port in question; these same signals for other ports are not affected.
Where the port in question is not clear, a numeric value in the range 0 to 2 is appended to the end of the signal name to indicate the port.

5.1 Mode 0

In this mode the ports of the uPD71055 are used to perform basic input/output operations. Each port operates with a bufferred input and a latched output.
According to the control word sent from the CPU, port 0, port 1, and the higher and lower 4 bits of port 2 can be independently specified for input or output.

(1) Input port operation

While the $\overline{RD}$ signal of a port specified for input is low level, data is taken into the port and the data of the port selected by the A0A1 signals is output to the data bus.

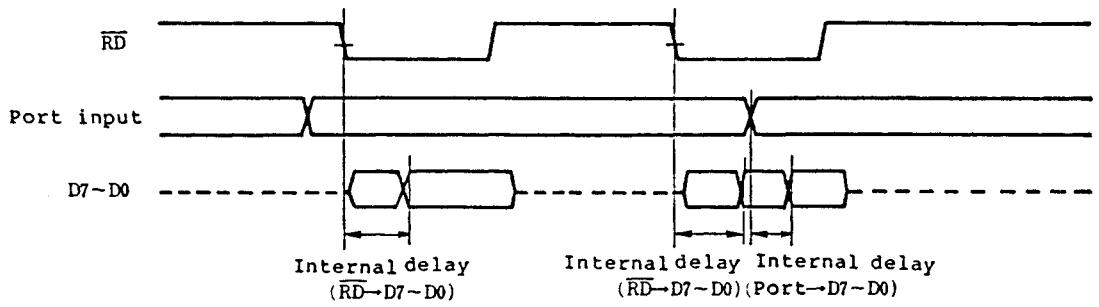


Fig. 5-1 Mode 0 Input Timing

(2) Output port operation

Ports specified for output constantly latch output values and output these to the port pins. When the CPU sets $\overline{WR}$ to low level and sends new data to the uPD71055, this data will be latched in the port selected by the A0A1 signals at the rising edge of $\overline{WR}$ and output to the port pins.
Low level is output immediately after the mode setting.

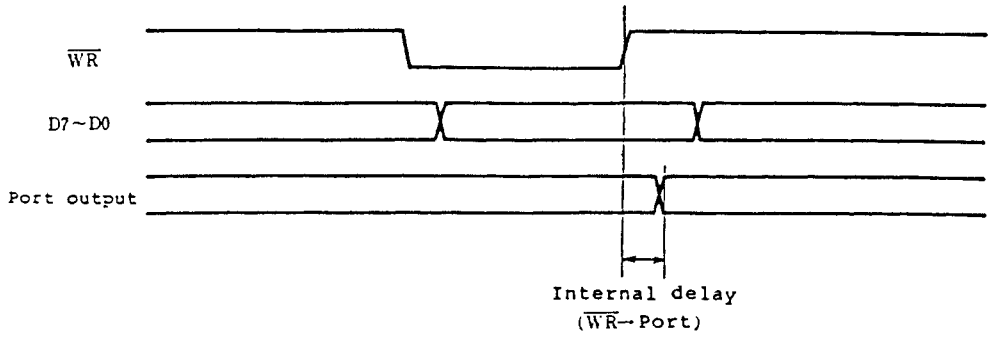


Fig. 5-2 Mode 0 Output Timing

By reading the contents of the ports set for output, the output value of the port can be ascertained.

(3) Group 0 mode 0

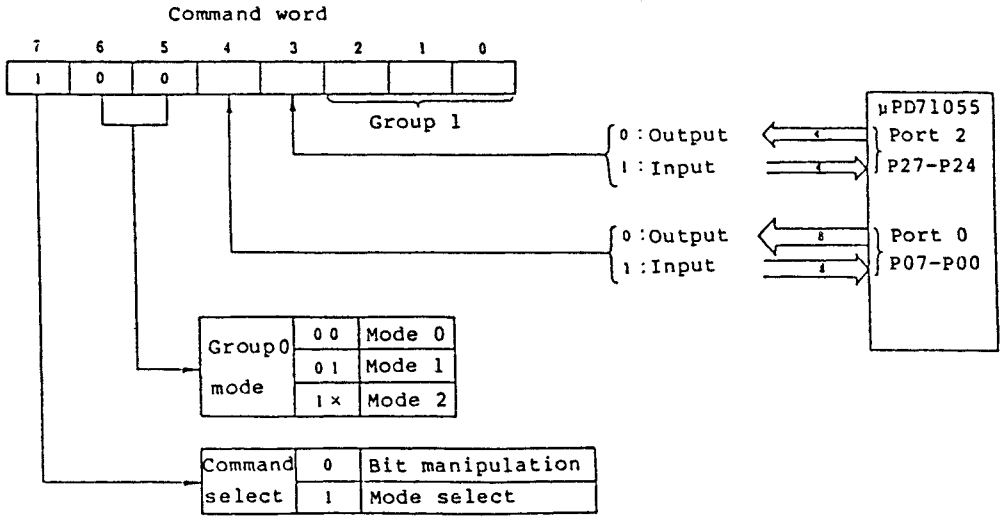


Fig. 5-3 Group 0 Mode 0

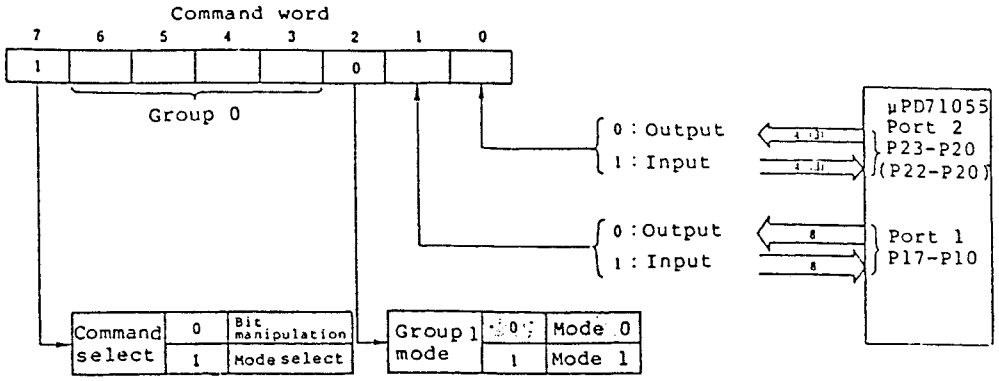


Fig. 5-4 Group 1 Mode 0

Note:
When group 0 is not set to mode 0, the bits of port 2 that can be used by group 1 are the 3 bits P22-P20.

(5) Mode 0 example

This is an example of connecting a CPU to an A/D converter. Here group 0 and group 1 are both set to mode 0 and port 2 is used to start conversion and detect termination of the conversion process.

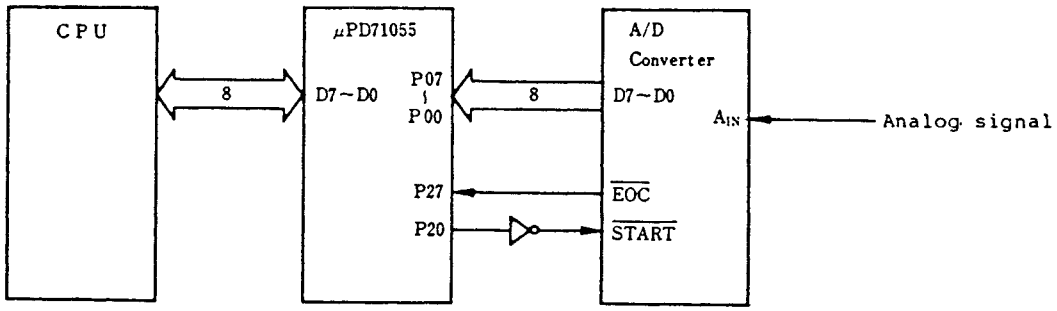


Fig. 5-5 A/D Converter Connection Example

This program is a subroutine that reads the converted data from an A/D converter.

```
READ_A/D:MOV     AL,10011000B  }   uPD71055 mode setting
         OUT     CTRLPORT,AL   }   o Group 0, group 1: mode 0
         MOV     AL,00000001B  |   o Port 0, port 2 (high): input
         OUT     CTRLPORT,AL   |   o Port 1, port 2 (low): output
         MOV     AL,00000000B  |   Conversion start
         OUT     CTRLPORT,AL   }
                                       ‾‾‾‾‾
                                       START  ‾‾\__/‾‾

WAIT_EOC:IN      AL,PORT2      }   End of conversion wait loop
         TEST1   AL,7          }
         BNZ     WAIT_EOC      }       ‾‾‾          Conversion
                                       EOC  ‾‾‾‾‾‾\_ ends
         IN      AL,PORT0          Read A/D converted values
         RET
```

5.2 Mode 1

In this mode, control and status signals are used to control data input/output. In group 0, the bits of port 0 function as the data port (for data input/output) and the higher 5 bits of port 2 as the control/status. In group 1, the bits of port 1 function as the data port and the lower 3 bits of port 2 as the control/status.
In mode 1, the bit manipulation instruction is used to write the bits of port 2.

Table 5-1 Functions of Port 2 in Mode 1

	Bit	During data input	During data output
	P20	INT1 (INTerrupt request)	INT1 (INTerrupt request)
	P21	IBF1 (Input Buffer Full F/F)	$\overline{\text{OBF1}}$ (Output Buffer Full F/F)
	P22	$\overline{\text{STB1}}$ (STroBe input) RIE1 (Read Interrupt Enable flag)	$\overline{\text{DAK1}}$ (Data AcKnowledge input) WIE1 (Write Interrupt Enable flag)
	P23*	Input/output	Input/output
	P23	INT0 (INTerrupt request)	INT0 (INTerrupt request)
	P24	$\overline{\text{STB0}}$ (STruBe input) RIE0 (Read Interrupt Enable flag)	Input/output
	P25	IBF0 (Input Buffer Full F/F)	Input/output
	P26	Input/output	$\overline{\text{DAK0}}$ (Data AcKnowledge input) WIE0 (Write Interrupt Enable flag)
	P27	Input/output	$\overline{\text{OBF0}}$ (Output Buffer Full F/F)

* Can only be used when group 0 is set to mode 0. At all other times, P23 belongs to group 0.

(1) Operation when data port is specified for input

When the data port (port 0 for group 0, and port 1 for group 1) is specified for input, the 8 bits of the data port are used for input. The bits of the control/status port (port 2) are used as follows:

(a) $\overline{STB}$ (strobe input) - input [$\overline{STB0}$ →P24, $\overline{STB1}$ →P22]

When this input is low level, the signals being sent form the peripheral to the data port are latched.

(b) IBF (input buffer full F/F) - output [$\overline{IBF0}$ →P25,
$\overline{STB1}$ →P21]

This output becomes high level to inform the peripheral that the input buffer has become full and to prohibit further data transfer. This signal becomes high level at the falling edge of the $\overline{STB}$ signal and becomes low level at the rising edge of the $\overline{RD}$ signal when $\overline{STB}$=1 (CPU completes read).
Initial value immediately after the mode setting is low level.

(c) INT (interrupt request) - output [INT0 →P23,
INT1 →P20]

This output becomes high level when the data from the peripheral is latched in the input port and functions as a data read request interrupt signal to the CPU. INT become high level when RIE (read interrupt enable flag) is 1 and $\overline{STB}$, IBF and $\overline{RD}$ are all high. INT becomes low level at the falling edge of the $\overline{RD}$ signal.
Initial value immediately after the mode setting is low level.

(d) RIE (read interrupt enable flag) [RIE0 →P24,
RIE1 →P22]

This is a read interrupt enable flag for read operation by the CPU. This bit controls interrupt request output to the CPU. Interrupts can be enabled by using the bit manipulation command to set this bit to '1' and disabled by resetting this bit to '0'.
Even if RIE is set/reset, the $\overline{STB}$ function of this bit is not affected.

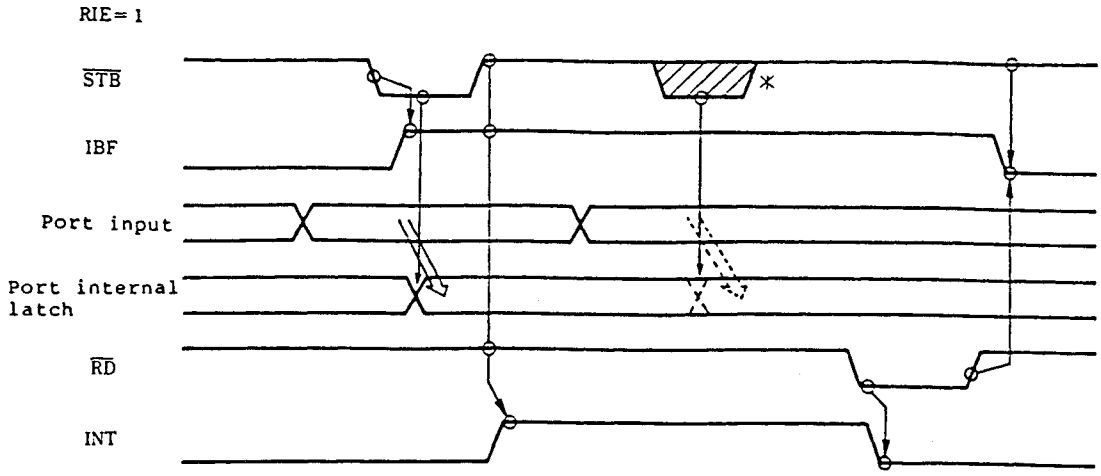


Fig. 5-6 Mode 1 Input Timing

* Here if $\overline{STB}$ becomes low level before IBF becomes low, the contents of the port latch will change. $\overline{STB}$ must therefore be kept high until IBF becomes low.

When input is specified in mode 1, the status of IBF, INT, and RIE can be ascertained by reading the contents of port 2.

(2) Operation when data port is specified for output

When the data port (Port 0 for group 0; Port 1 for group 1) is specified for output, the 8 bits of the data port are used for output (low level is output immediately after the mode setting) and the bits of the control/status port (port 2) function as follows:

(a) $\overline{OBF}$ (output buffer full F/F) - output [$\overline{OBF0}$ → P27, $\overline{OFB1}$ → P21]

This signal become low when data is received from the CPU and is latched in the output port. $\overline{OBF}$ therefore functions as a data receive request to the peripheral. $\overline{OBF}$ becomes low level at the rising edge of $\overline{WR}$ when $\overline{DAK}$=1 (CPU completes write) and becomes high at the falling edge of the $\overline{DAK}$ signal when the peripheral receives the data from the uPD71055.

Initial value immediately after the mode setting is high level.

(b) $\overline{DAK}$ (data acknowledge) - input [$\overline{DAK0}$ - P26, $\overline{DAK1}$ - P20]

This input is used to inform the uPD71055 that output port data has been received by the peripheral. The peripheral must be set so that it outputs a low level signal when it has received data.

(c) INT (interrupt request) - output [INT0 → P23,
INT1 → P20]

This output becomes high level when the output data from the uPD71055 has been received by the peripheral. INT therefore functions as a write request signal to the CPU indicating that it should send the next output data to the uPD71055. INT becomes high level when $\overline{WIE}$ ($\overline{write}$ interrupt enable flag) is set to '1' and $\overline{WR}$, $\overline{OBF}$, and $\overline{DAK}$ are all high and becomes low level at the falling edge of the $\overline{WR}$ signal.
Initial value immediately after the mode setting is low level.

(d) WIE (write interrupt enable flag) [WIE0 → P26,
WIE1 → P22]

This is a request interrupt enable flag for write operation by the CPU. This bit controls interrupt request output to the CPU. Interrupts can be enabled by using the bit manipulation command to set this bit to '1' and disabled by resetting this bit to '0'.
Even if RIE is set/reset, the $\overline{DAK}$ function of this bit is not affected.

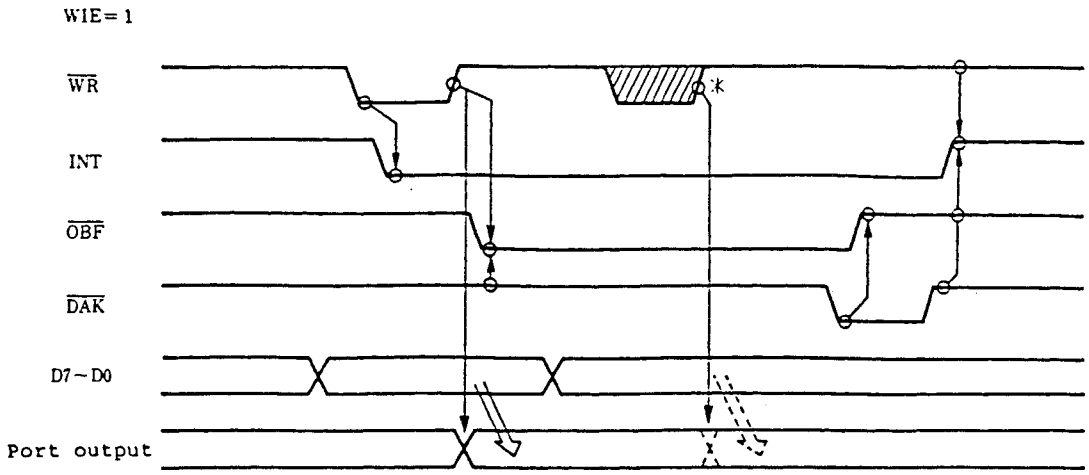


Fig. 5-7 Mode 1 Output Timing

* If data is written from the CPU before $\overline{OBF}$ becomes high, the contents of the port latch will change. Data write must therefore not be performed while $\overline{OBF}$ is low.

When output is specified in mode 1, the status of $\overline{OBF}$, INT, and WIE can be ascertained by reading the contents of port 2.

(3) Group 0 mode 1

When group 0 is used in mode 1, the higher 5 bits of port 2 become part of group 0. Of these 5 bits, 3 are used as control/status and the remaining 2 bits can be used by the user for input/output (bit manipulation instruction).

(a) To input from the data port (port 0)

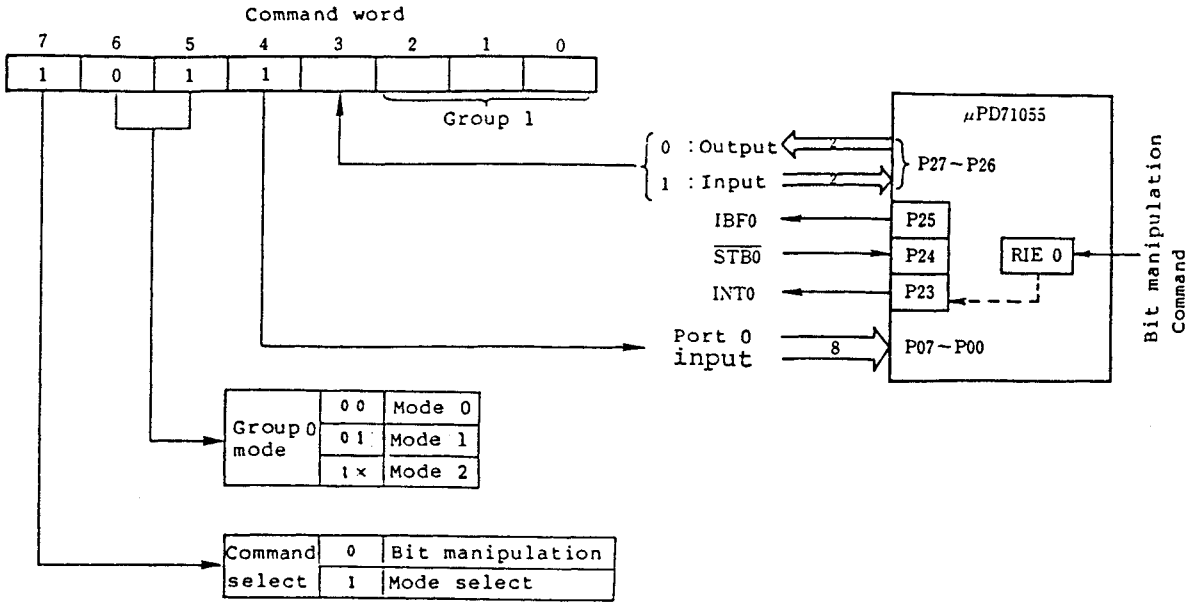


Fig. 5-8 Group 0 Mode 1 Input

(b) To output from the data port (port 0)

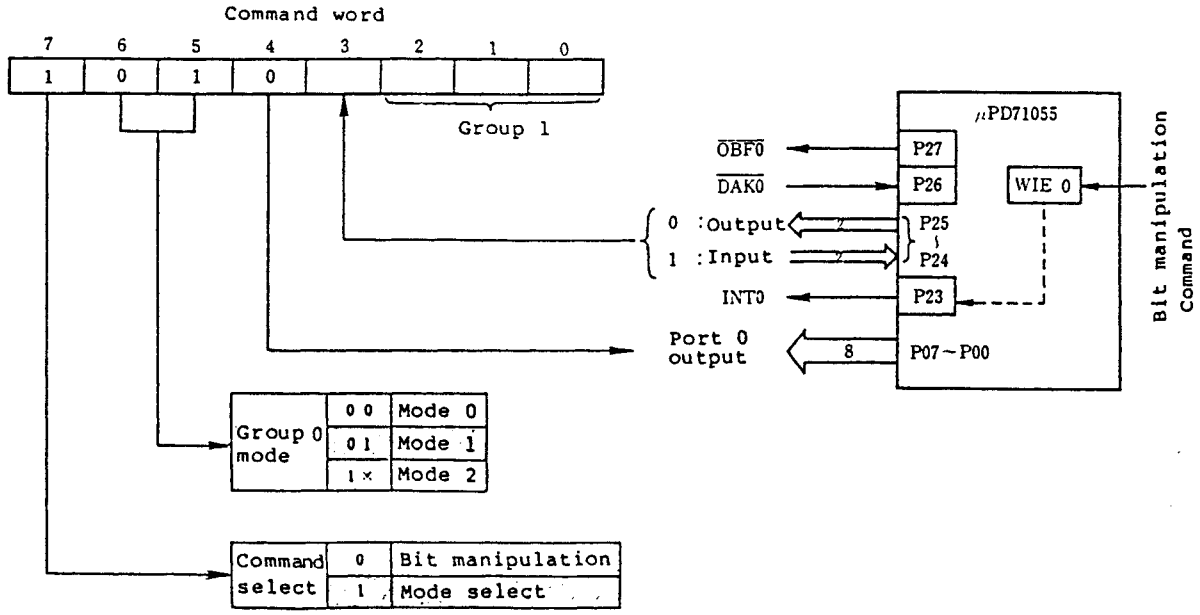


Fig. 5-9 Group 0 Mode 1 Input

(4) Group 1 mode 1

When group 1 is used in mode 1, the lower 4 bits of port 2 become part of group 1. Of these 4 bits, 3 are used as control/status and the remaining 1 bit* can be used by the user for input/output (bit manipulation command).

(a) To input from the data port (port 1)

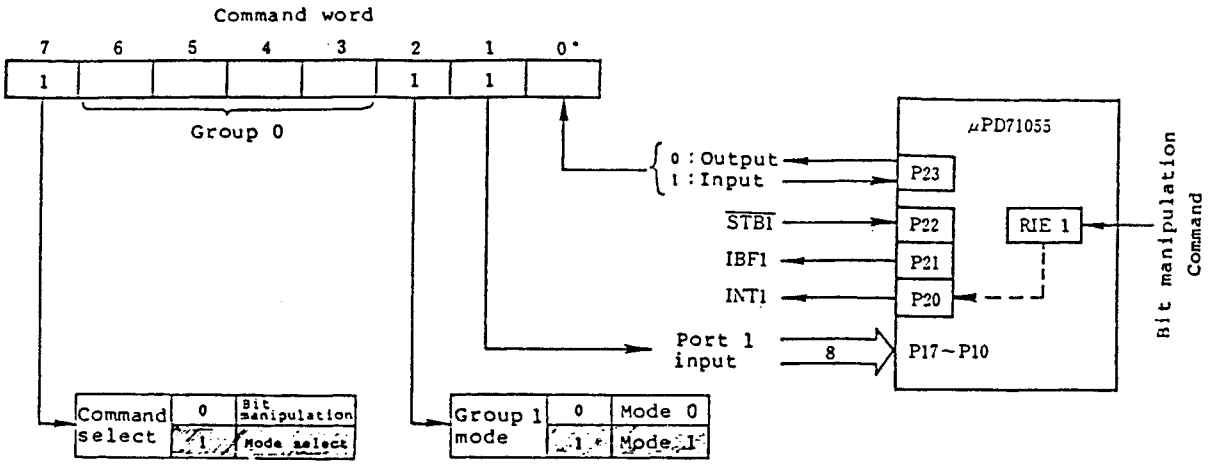


Fig. 5-10 Group 1 Mode 1 Input

(b) To output from the data port (port 1)

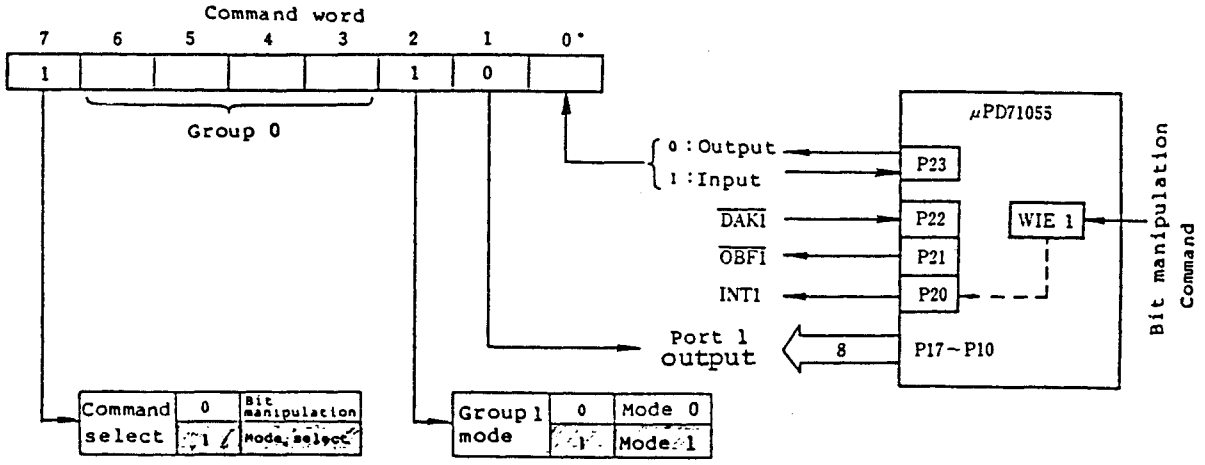


Fig. 5-11 Group 1 Mode 1 Input

* P23 belongs to group 1 only when group 0 is in mode 0, otherwise P23 belongs to group 0.

(5) Mode 1 examples

This is an example of connecting a printer with a Centronics interface. Group 0 is used in mode 1.
Group 1 can operate in any mode; in this example mode 0 is set.

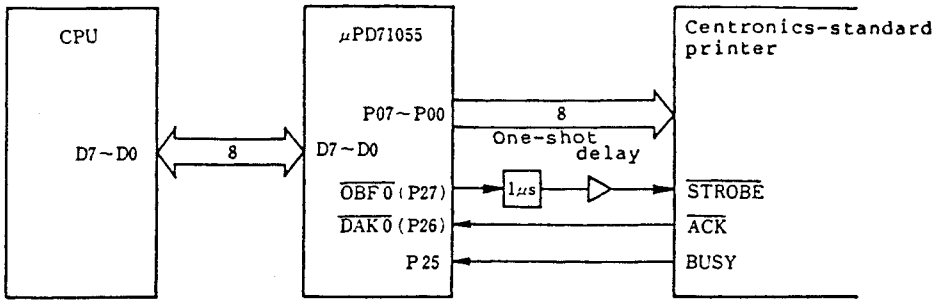


Fig. 5-12 Connection to a Printer

The program shown below is as subroutine that sends character strings to the printer.

```
                                    uPD71055 mode setting
INIT:    MOV     AL, 10101000B  }   o Group 0: mode 1
         OUT     CTRLPORT,AL    }   o Port 0: output
         RET                        o Port 2 (high): input
SENDPRN:MOV      BW,DATA            Output data address
PRNLOOP:MOVE     AL,[BW]        }
         CMP     AL,0FFH        }   End if data FFH
         BNZ     WAIT           }
         RET
WAIT:    IN      AL,PORT2
         TEST1   AL,7           }   Wait until output buffer is empty
         BZ      WAIT           }
         TEST1   AL,5           }   Wait until printer can
         BNZ     WAIT           }   accept data
         MOV     AL,[BW]        }   Send data to printer
         OUT     PORT0,AL       }
         INC     BW
         BR      PRNLOOP
```

5.3 Mode 2

This mode can only be used for group 0. In this mode port 0 functions as a bidirectional 8-bit data port operating under the control of the control/status signals (higher 5 bits of port 2). In this mode, port 0 combines the input and output operations of mode 1.

Table 5-2 Functions of Port 2 in Mode 2

Bit	Function
P23	INT0 (INTerrupt request)
P24	$\overline{\text{STB0}}$ (StroBe input) RIE0 (Read Interrupt Enable flag)
P25	IBF0 (Input Buffer Full F/F)
P26	$\overline{\text{DAK0}}$ (Data AcKnowledge input) WIE0 (Write Interrupt Enable flag)
P27	$\overline{\text{OBF0}}$ (Output Buffer Full F/F)

The $\overline{\text{DAK0}}$ and $\overline{\text{STB0}}$ signals are used to select input or output mode for port 0. By using these signals, bidirectional operation between the CPU and the peripheral can be realized.
In mode 2, the bit manipulation instruction is used to write to port 2.

(1) Operation of the control/status port

o Signals used when port 0 is used for output

(a) $\overline{\text{OBF0}}$ (output buffer full F/F) - output [P27]

This signal becomes low level when data is received from the CPU and is latched in the port 0 output buffer. $\overline{\text{OBF0}}$ therefore functions as a receive request signal to the peripheral. $\overline{\text{OBF0}}$ becomes low level at the rising edge of the $\overline{\text{WR0}}$ signal (indicates the end of CPU data write) and becomes high level at the falling edge of the $\overline{\text{DAK0}}$ signal (indicates that the peripheral has received the output data from port 0).

Initial value immediately after the mode setting is high level.

(b) $\overline{\text{DAK0}}$ (data acknowledge) - input [P26]

When this input becomes low level, the three-state output buffer is set for output mode. This signal is sent from the peripheral in response to the $\overline{\text{OBF0}}$ signal from the uPD71055 and should be set to become low level when data is received from port 0.

(c) WIE0 (write interrupt enable flag) [P26]

This is a write interrupt enable flag for write operation by the CPU. This bit controls interrupt request output to the CPU. This bit controls interrupt request output to the CPU. Interrupts can be enabled by using the bit manipulation command to set this bit to '1' and disabled by resetting this bit to '0'.
Even if WIE0 is set/reset, the $\overline{\text{DAK0}}$ function of this bit is not affected.

o Signals used when port 0 is used for input

(d) $\overline{\text{STB0}}$ (strobe input) - input [P24]

When this signal becomes low level, the data signals being sent from the peripheral to port 0 are latched.

(e) IBF0 (input buffer full F/F) - output [P25]

When this output becomes high level, it indicates that the input buffer is full and functions as a transfer prohibit signal to the peripheral. This signal becomes high level at the falling edge of the $\overline{\text{STB0}}$ signal and becomes low level at the rising edge of the $\overline{\text{RD0}}$ signal when $\overline{\text{STB0}}$=1 (CPU completes read).
Initial value immediately after the mode setting is low level.

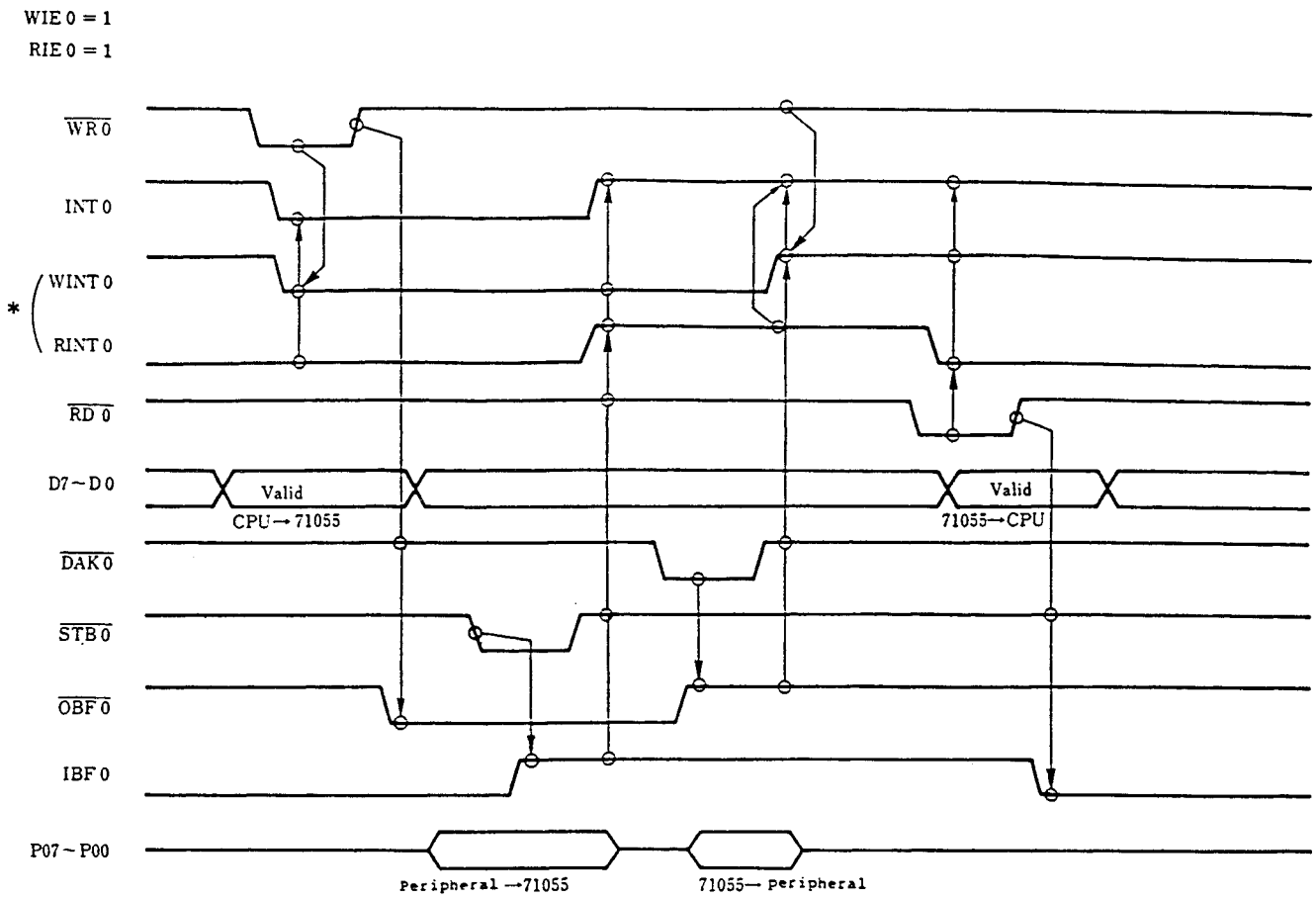
(f) RIE0 (read interrupt enable flag) - [P24]

This is a read interrupt enable flag for read operation by the CPU. This bit controls interrupt request output to the CPU. Interrupts can be enabled by using the bit manipulation command to set this bit to '1' and disabled by resetting this bit to '0'.
Even if RIE0 is set/reset, the $\overline{\text{STB0}}$ function of this bit is not affected.

o Signal used for both input and output

(g) INT0 (interrupt request) - output [P23]

This signal is used for both input and output operations of port 0. During input operation, it functions as a read request interrupt signal to the CPU and during output as a write request interrupt signal. The output of this signal is the logical sum (OR) of the INT signal during input operation and the INT signal during output operation in mode 1. Initial value immediately after the mode setting is low level.



* WINT0 and RINT0 are internal signals and are write and read interrupt request signals to the CPU, respectively.

$$WINT0 = \overline{OBF0} \cdot \overline{WIE0} \cdot \overline{DAK0} \cdot \overline{WR0}$$

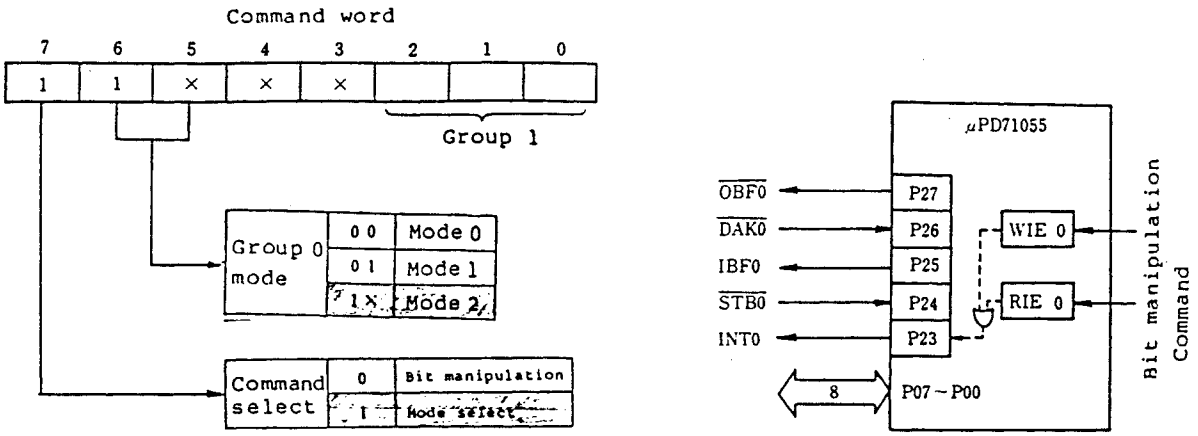
$$RINT0 = IBF0 \cdot REI0 \cdot \overline{STB0} \cdot \overline{RD0}$$

Also note that

$$INT0 = WINT0 + RINT0$$

Fig. 5-13 Mode 2 Timing

(2) Mode 2 specification



In this mode, the status of the following signals can be ascertained by reading port 2: $\overline{OBF0}$, IBF0, INT0, WIE0, and RIE0.

Fig. 5-14 Group 0 Mode 2

(3) Mode 2 example

This is an example of transferring data between two CPUs.

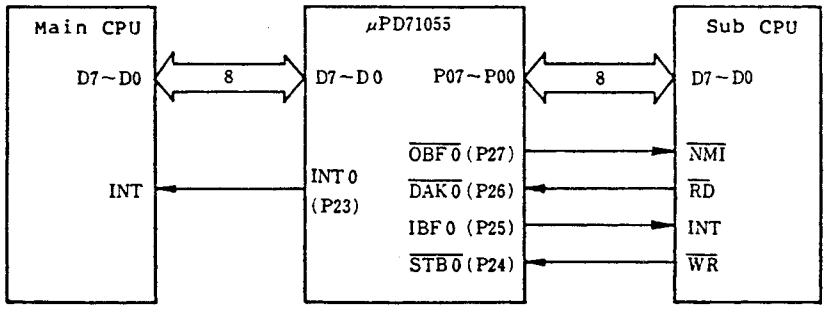
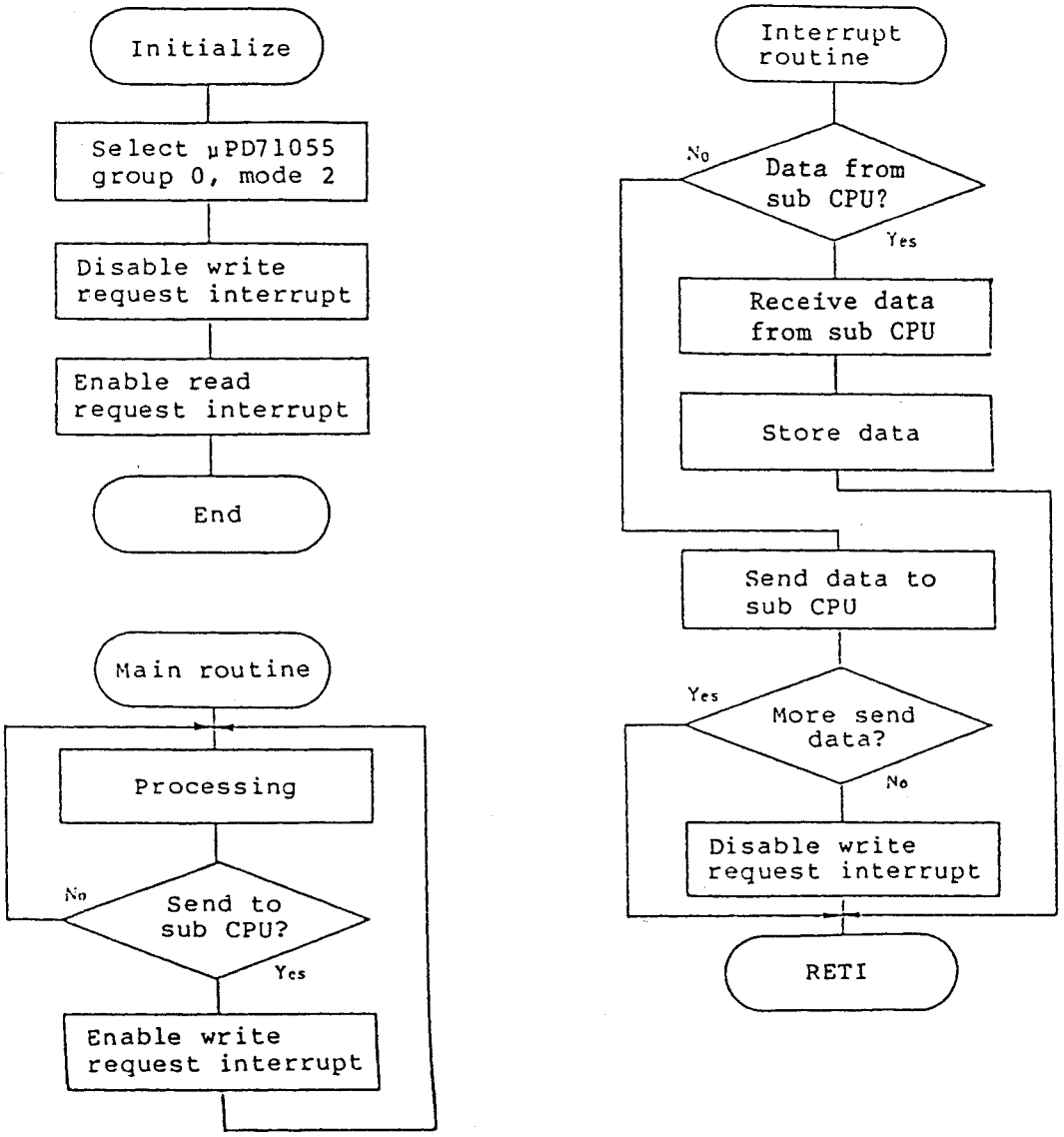


Fig. 5-15 Connecting Two CPUs

Main CPU Flowchart



Sub CPU Flowchart

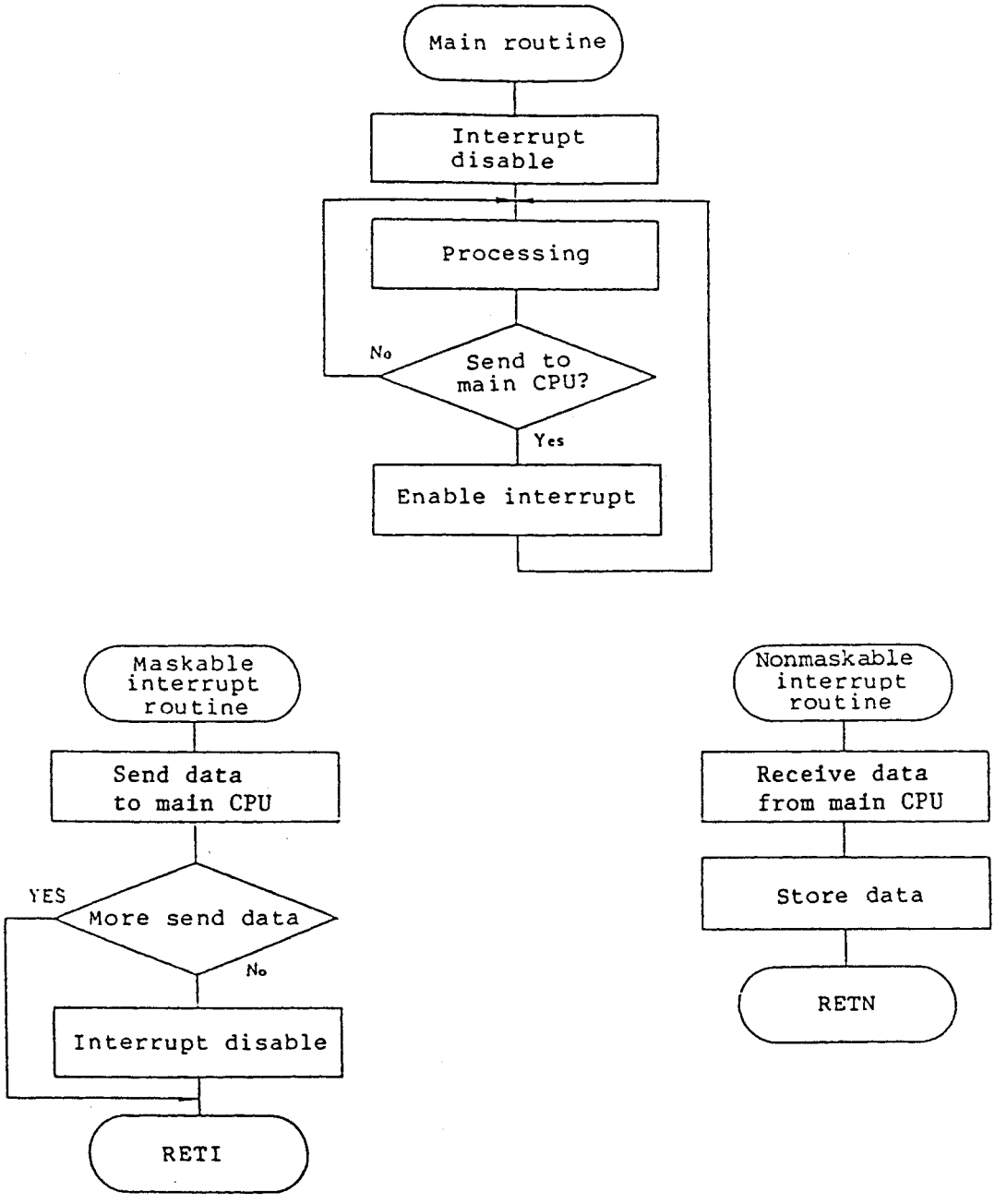


Table 6-1 Mode Combinations and Bit Functions of Port 2

Mode Combinations and Port 2 Bit Functions

Group 0							Group 1					
Mode	PO_7-PO_0	$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	Mode	$P1_7$-$P1_0$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
0	In	D	D	D	D	NA	0	In	D	D	D	D
0	In	D	D	D	D	NA	0	Out	D	D	D	D
0	In	D	D	D	D	NA	1	In	B	$\overline{STB1}$ (RIE1)	IBF1	INT1
0	In	D	D	D	D	NA	1	Out	B	$\overline{DAK1}$ (WIE1)	$\overline{OBF1}$	INT1
0	Out	D	D	D	D	NA	0	In	D	D	D	D
0	Out	D	D	D	D	NA	0	Out	D	D	D	D
0	Out	D	D	D	D	NA	1	In	B	$\overline{STB1}$ (RIE1)	IBF1	INT1
0	Out	D	D	D	D	NA	1	Out	B	$\overline{DAK1}$ (WIE1)	$\overline{OBF1}$	INT1
1	In	B	B	IBF0	$\overline{STB0}$ (RIE0)	INT0	0	In	NA	D	D	D
1	In	B	B	IBF0	$\overline{STB0}$ (RIE0)	INT0	0	Out	NA	D	D	D
1	In	B	B	IBF0	$\overline{STB0}$ (RIE0)	INT0	1	In	NA	$\overline{STB1}$ (RIE1)	IBF1	INT1
1	In	B	B	IBF0	$\overline{STB0}$ (RIE0)	INT0	1	Out	NA	$\overline{DAK1}$ (WIE1)	$\overline{OBF1}$	INT1
1	Out	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	B	B	INT0	0	In	NA	D	D	D
1	Out	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	B	B	INT0	0	Out	NA	D	D	D
1	Out	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	B	B	INT0	1	In	NA	$\overline{STB1}$ (RIE1)	IBF1	INT1
1	Out	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	B	B	INT0	1	Out	NA	$\overline{DAK1}$ (WIE1)	$\overline{OBF1}$	INT1
2	I/O	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	IBF0	$\overline{STB0}$ (RIE0)	INT0	0	In	NA	D	D	D
2	I/O	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	IBF0	$\overline{STB0}$ (RIE0)	INT0	0	Out	NA	D	D	D
2	I/O	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	IBF0	$\overline{STB0}$ (RIE0)	INT0	1	In	NA	$\overline{STB1}$ (RIE1)	IBF1	INT1
2	I/O	$\overline{OBF0}$	$\overline{DAK0}$ (WIE0)	IBF0	$\overline{STB0}$ (RIE0)	INT0	1	Out	NA	$\overline{DAK1}$ (WIE1)	$\overline{OBF1}$	INT1

Note:

(1) In this chart, "NA" indicates that the bit cannot be used by this group.

(2) The symbol "B" indicates bits that can only be rewritten by the bit manipulation command.

(3) In this chart, "D" indicates that is used by the user.

(4) Symbols in parentheses are internal flags.

(5) In indicates Input, Out indicates Output, and I/O indicates Input/Output.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
Input Voltage	V_I		-0.5 to V_{DD}+0.3	V
Output Voltage	V_O		-0.5 to V_{DD}+0.3	V
Operating Temperature	T_{opt}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

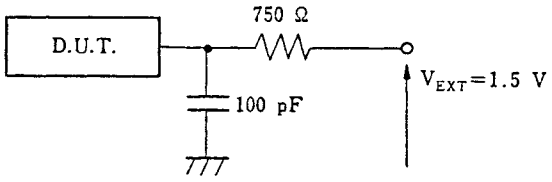
DC CHARACTERISTICS (Ta = -40 to +85°C, V_{DD} = 5V $\pm$10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage High	V_{IH}		2.2		V_{DD} +0.3	V
Input Voltage Low	V_{IL}		-0.5		0.8	V
Output Voltage High	V_{OH}	I_{OH} = -400uA	0.7 V_{DD}			V
Output Voltage Low	V_{OL}	I_{OL} = 2.5mA			0.4	V
Darlington Drive Current	I_{DAR}	*	-1.0		-4.0	mA
Input Leakage Current High	I_{LIH}	V_I=V_{DD}			10	uA
Input Leakage Current Low	I_{LIL}	V_I=0V			-10	uA
Output Leakage Current High	I_{LOH}	V_I=V_{DD}			10	uA
Output Leakage Current Low	I_{LOH}	V_I=0V			-10	uA
Supply Current	I_{DD1}	Operation mode		5	10	mA

DC CHARACTERISTICS (Ta = -40 to +85°C, V_{DD} = 5V ±10%) (Cont'd)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{DD2}	Standby mode Inputs: RESET=0.1V Others=V_{DD}-0.1V Outputs: Open		2	50	uA

* For up to 8 lines arbitrarily chosen from ports B and C.



CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	fc = 1 MHz Unmeasured pins returned to 0V			10	pF
I/O Capacitance	C_{IO}				20	pF

AC CHARACTERISTICS (Ta = -40 to +85°C, V_{DD} = 5V ±10%)

READ CYCLE:

PARAMETER	SYMBOL	TEST CONDITIONS	uPD71055		uPD71055-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
*Address Set-up to $\overline{RD}\downarrow$	t_{SAR}		0		0		ns
*Address Hold from $\overline{RD}\uparrow$	t_{HRA}		0		0		ns
$\overline{RD}$ Pulse Width	t_{RRL}		160		150		ns
Data Delay Time from $\overline{RD}\downarrow$	t_{DRD}	C_L=150pF		120		100	ns
Data Float Time from $\overline{RD}\uparrow$	t_{FRD}	C_L= 20pF R_L= 2K ohm	10	85	10	60	ns
Read out Recovery Time	t_{RV}		200		150		ns

WRITE CYCLE:

PARAMETER	SYMBOL	TEST CONDITIONS	uPD71055		uPD71055-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
*Address Set-up to $\overline{WR}\downarrow$	t_{SAW}		0		0		ns
*Address Hold from $\overline{WR}\uparrow$	t_{HWA}		0		0		ns
$\overline{WR}$ Pulse Width	t_{WWL}		120		100		ns
Data Set-up Time to $\overline{WR}\downarrow$	t_{SDW}		100		100		ns
Data Hold Time from $\overline{WR}\uparrow$	t_{HWD}		0		0		ns
Write Recovery Time	t_{RV}		200		150		ns

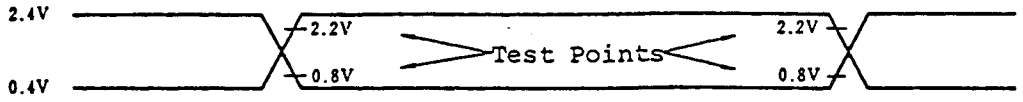
*: $\overline{CS}$, A1 and A0

AC CHARACTERISTICS (Ta = -40 to +85°C, V_{DD} = 5V ±10%) (Cont'd)
OTHERS:

PARAMETER	SYMBOL	TEST CONDITIONS	uPD71055		uPD71055-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Port Setup Time to $\overline{RD}\downarrow$	t_{SPR}		0		0		ns
Port Hold Time from $\overline{RD}\uparrow$	t_{HRP}		0		0		ns
Port Setup Time to $\overline{STB}\downarrow$	t_{SPS}		0		0		ns
Port Hold Time from $\overline{STB}\uparrow$	t_{HSP}		150		150		ns
Port Delay Time from $\overline{WR}\uparrow$	t_{DWP}	C_L = 150pF		350		200	ns
$\overline{STB}$ Pulse Width	t_{SSL}		350		100		ns
$\overline{DAK}$ Pulse Width	t_{DADAL}		300		100		ns
Port Delay Time from $\overline{DAK}\downarrow$ (Mode 2)	t_{DDAP}	C_L = 150pF		300		150	ns
Port Float Time from $\overline{DAK}\uparrow$ (Mote 2)	t_{FDAP}	C_L = 20pF R_L = 2K ohm	20	250	20	250	ns
$\overline{OBF}$ Set Delay from $\overline{WR}\uparrow$	t_{DWOB}	C_L = 150pF		300		150	ns
$\overline{OBF}$ Clear Delay from $\overline{DAK}\downarrow$	t_{DDAOB}			350		150	ns
IBF Set Delay from $\overline{STB}\downarrow$	t_{DSIB}			300		150	ns
IBF Clear Delay from $\overline{RD}\uparrow$	t_{DRIB}			300		150	ns
INT Set Delay from $\overline{DAK}\uparrow$	t_{DDAI}			350		150	ns
INT Clear Delay from $\overline{WR}\downarrow$	t_{DWI}			450		200	ns
INT Set Delay from $\overline{STB}\uparrow$	t_{DSI}			300		150	ns
INT Clear Delay from $\overline{RD}\downarrow$	t_{DRI}			400		200	ns
RESET Pulse Width	t_{RESET1}	*1	50		50		us
	t_{RESET2}	*2	500		500		ns

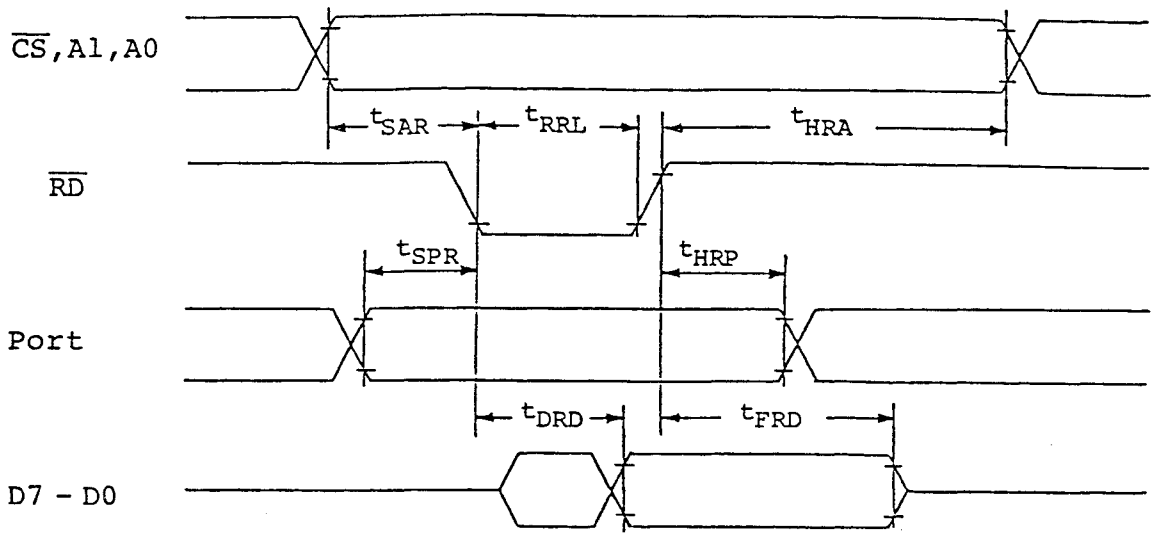
*1: During power-on or right after power-on
*2: During operation

AC TEST INPUT WAVEFORM

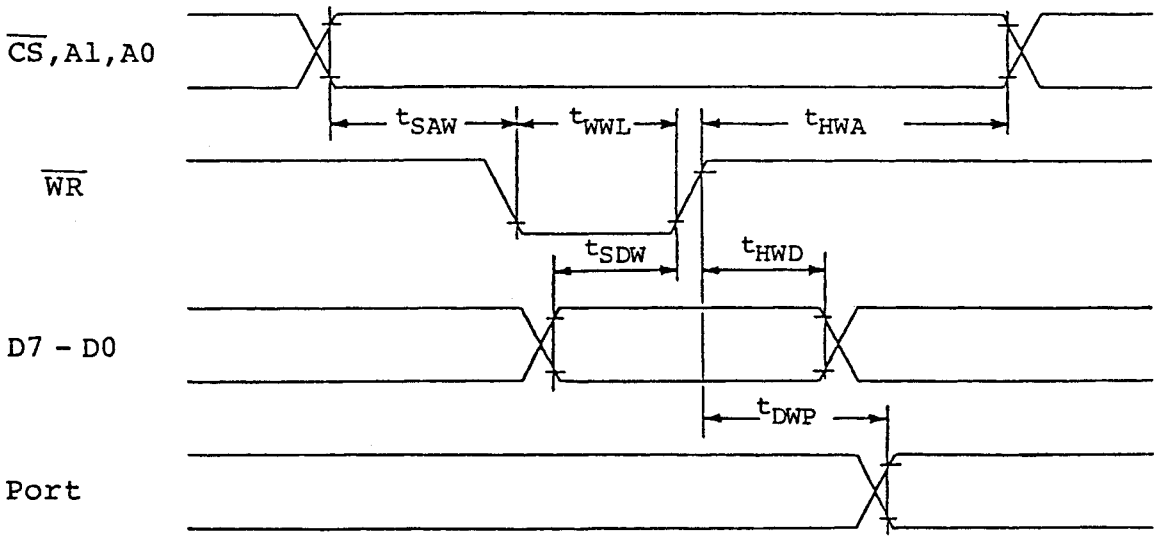


TIMING

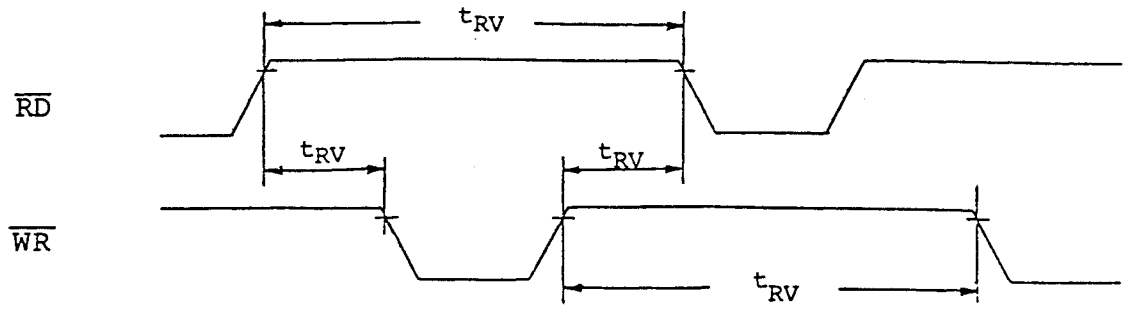
MODE 0: Input



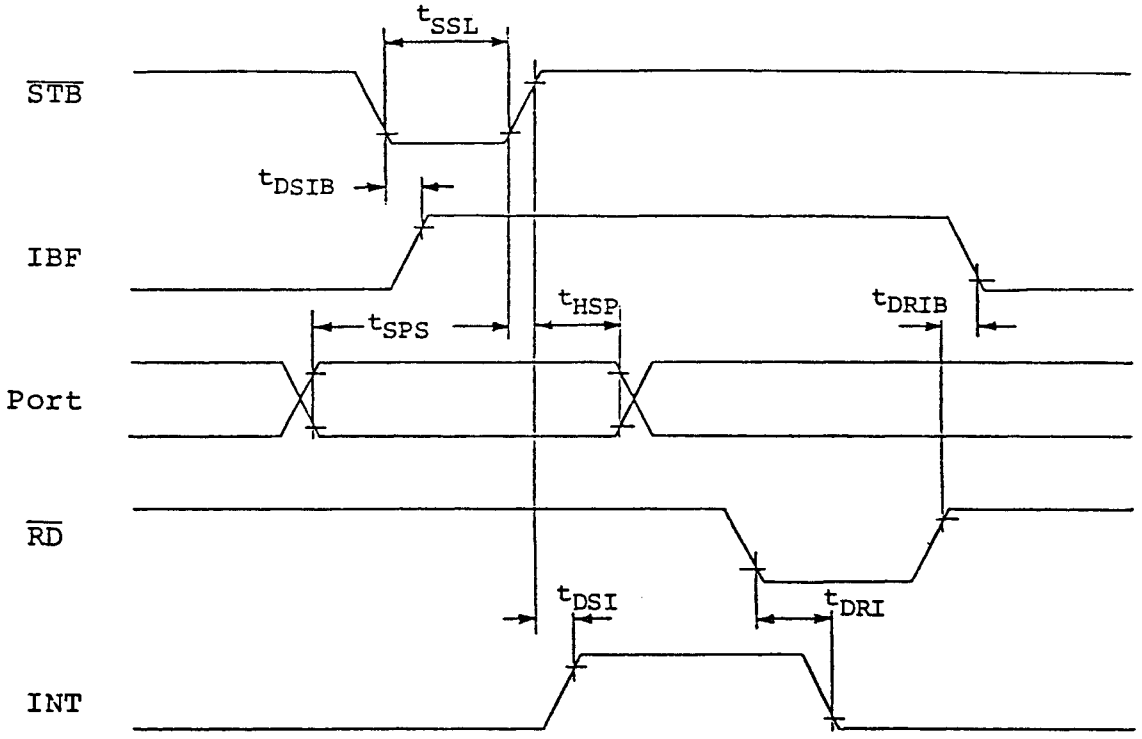
MODE 0: Output



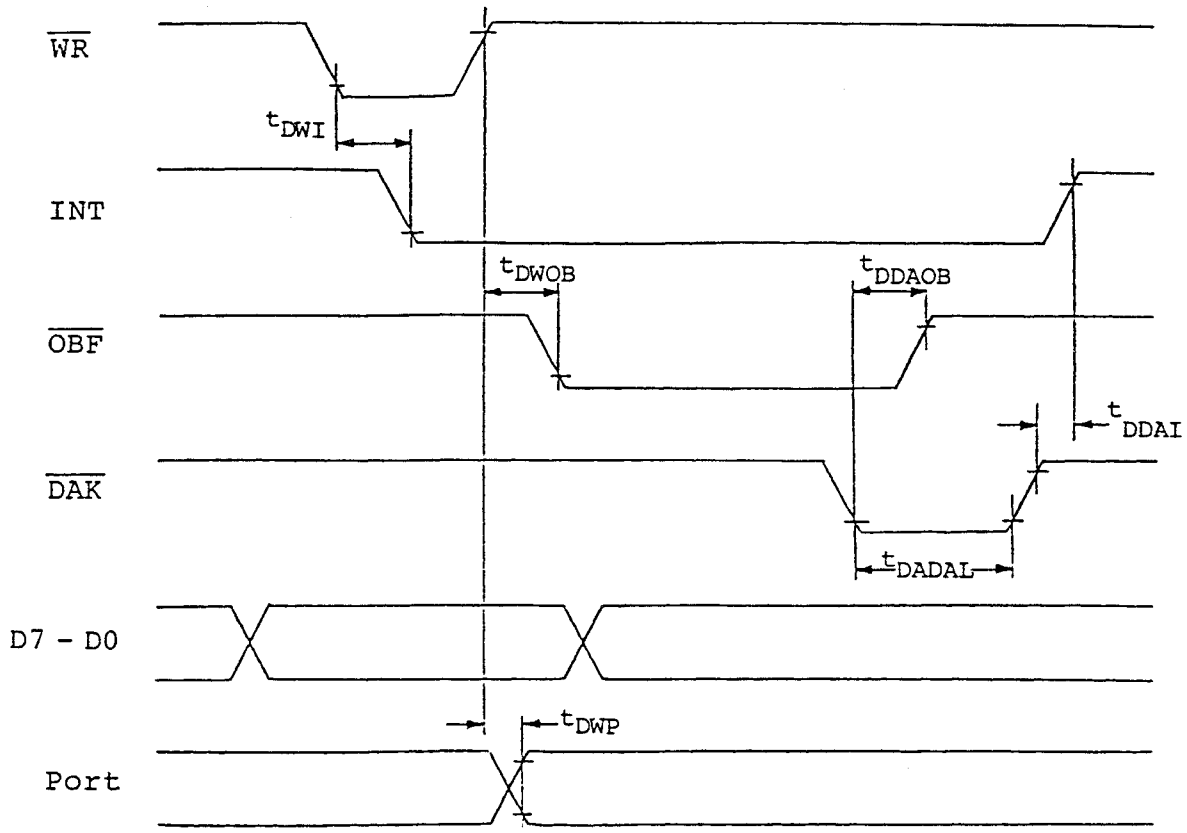
RECOVERY TIME



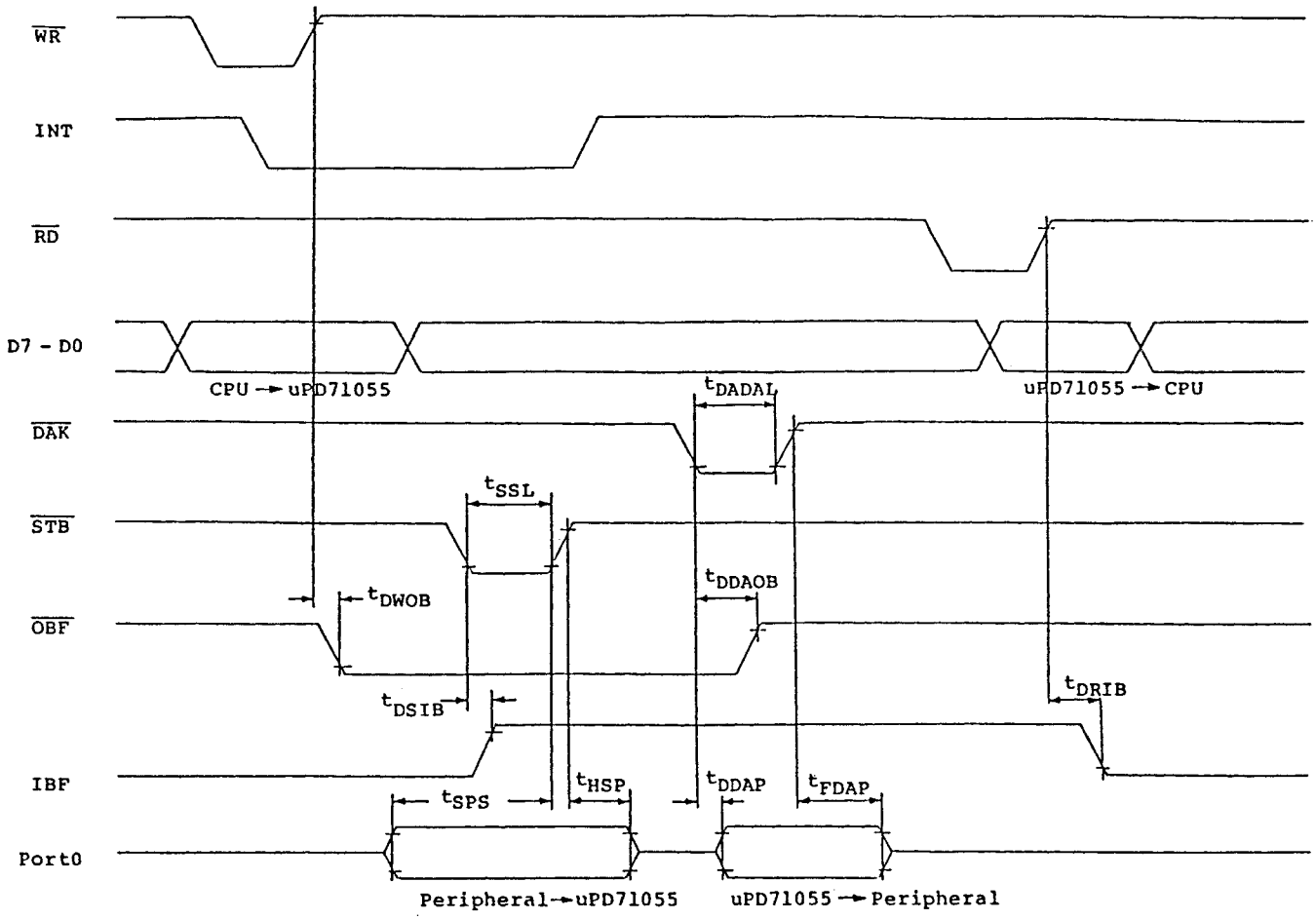
MODE 1: Input



MODE 1: Output

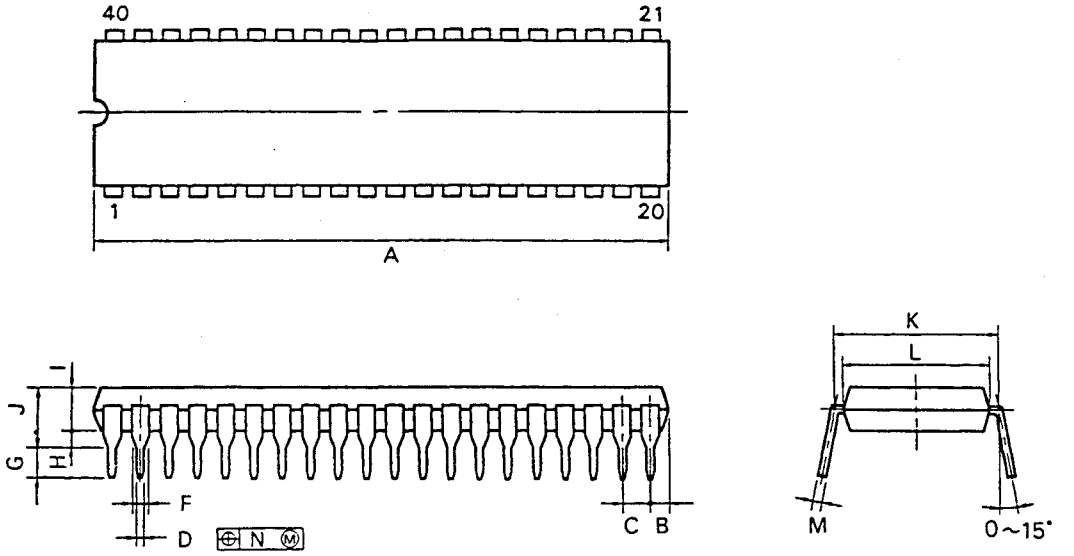


MODE 2:


WR
INT
RD
D7 - D0
CPU → uPD71055
uPD71055 → CPU
DAK
STB
OBF
IBF
Port0
tDADAL
tSSL
tDWOB
tDDAOB
tDSIB
tDRIB
tSPS
tHSP
tDDAP
tFDAP
Peripheral → uPD71055
uPD71055 → Peripheral

PACKAGE OUTLINES

40-pin Plastic



P40C-100-600A

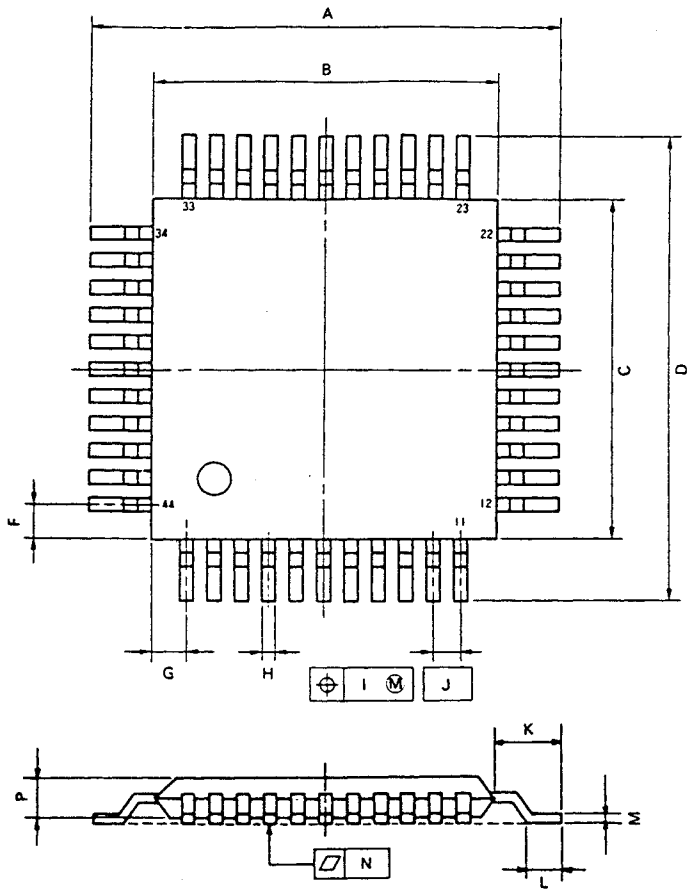
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

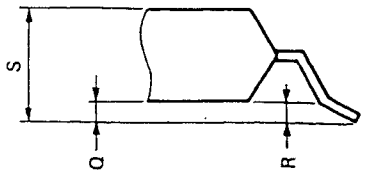
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.6^{-0.3}$	$0.142^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

44-pin Plastic QFP (bent lead)



detail of lead end



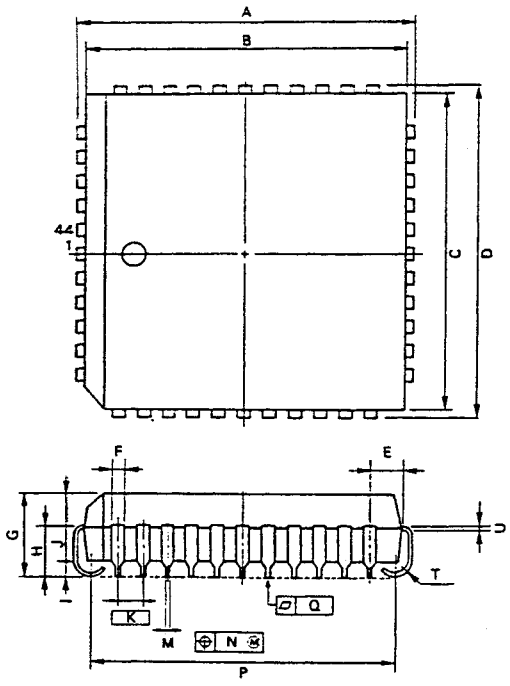
P44GB-80-3B4

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$13.6^{+0.4}$	$0.535^{+0.017}_{-0.016}$
B	$10^{+0.2}$	$0.394^{+0.008}_{-0.009}$
C	$10^{+0.2}$	$0.394^{+0.008}_{-0.009}$
D	$13.6^{+0.4}$	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.35^{+0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.8^{+0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{+0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

44-pin PLCC



P44L-50A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.5^{\pm 0.2}$	$0.689^{\pm 0.008}$
B	16.58	0.653
C	16.58	0.653
D	$17.5^{\pm 0.2}$	$0.689^{\pm 0.008}$
E	$1.94^{\pm 0.15}$	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	$4.4^{\pm 0.2}$	$0.173^{+0.009}_{-0.008}$
H	$2.8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$15.50^{\pm 0.20}$	$0.610^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

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